RENESAS **1:12 LVDS Output 1.8V Fanout Buffer**

8P34S1212I Datasheet

Description

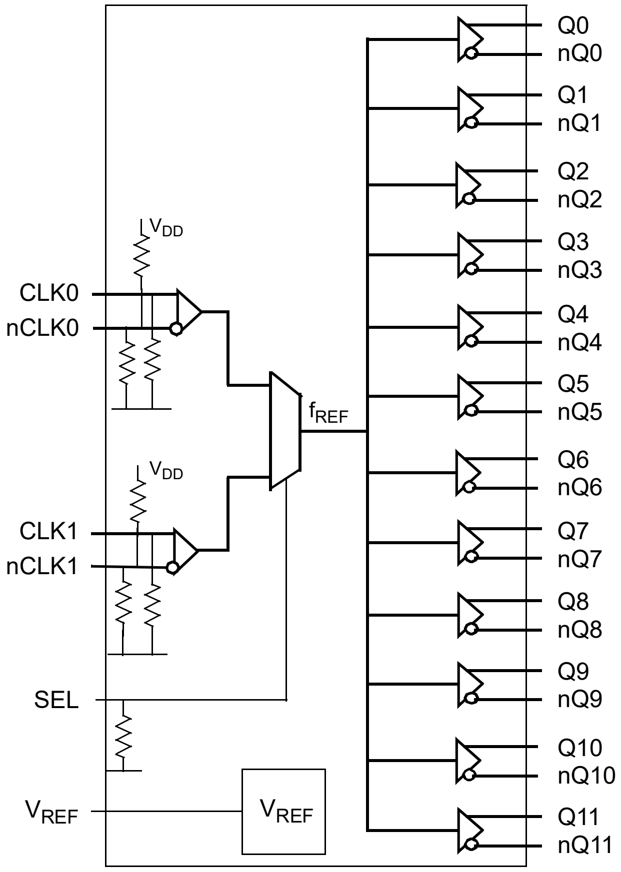
The 8P34S1212I is a high-performance differential LVDS fanout buffer. The device is designed for the fanout of high-frequency, very low additive phase-noise clock and data signals. The 8P34S1212I is characterized to operate from a 1.8V power supply. Guaranteed output-to-output and part-to-part skew characteristics make the 8P34S1212I ideal for those clock distribution applications that demand well-defined performance and repeatability.

Two selectable differential inputs and 12 low skew outputs are available. The integrated bias voltage reference enables easy interfacing of single-ended signals to the device inputs. The device is optimized for low power consumption and low additive phase noise.

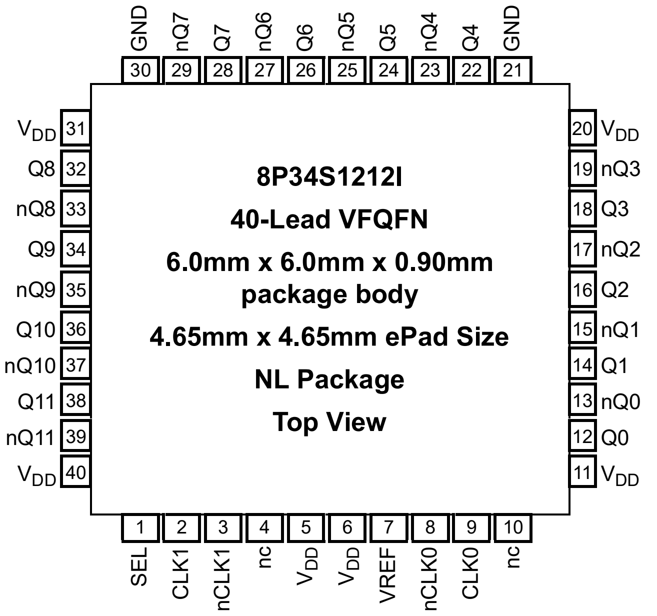
Features

- 12 low skew, low additive jitter LVDS output pairs
- Two selectable, differential clock input pairs
- Differential CLK0, CLK1 pairs can accept the following differential input levels: LVDS, CML
- Maximum input clock frequency: 1.2GHz (maximum)
- LVCMOS/LVTTL interface levels for the control input select pin
- Output skew: 10ps (typical)
- Propagation delay: 340ps (typical)
- Low additive phase jitter, RMS; f_{REF} = 156.25MHz, V_{PP} = 1V, 12kHz- 20MHz: 41fs (typical)
- Maximum device current consumption (I_{DD}): 227mA (maximum) at 1.89V
- Full 1.8V supply voltage
- Lead-free (RoHS 6), 40-Lead VFQFN packaging
- -40°C to 85°C ambient operating temperature

Block Diagram



Pin Assignment



Pin Descriptions and Characteristics

Table 1. Pin Descriptions[a]

Number	Name	Type		Description
1	SEL	Input	Pulldown	Reference select control. See Table 3 for function. LVCMOS/LVTTL interface levels.
2	CLK1	Input	Pulldown	Non-inverting differential clock/data input.
3	nCLK1	Input	Pulldown/ Pullup	Inverting differential clock/data input.
4, 10	nc	Unused		Do not connect.
5, 6, 11, 20, 31, 40	V_{DD}	Power		Power supply pins.
7	V_{REF}			Bias voltage reference. Provides an input bias voltage for the CLKx, nCLKx input pairs in AC-coupled applications. Refer to *Figures 2B and 2C* for applicable AC-coupled input interfaces.
8	nCLK0	Input	Pulldown/ Pullup	Inverting differential clock/data input.
9	CLK0	Input	Pulldown	Non-inverting differential clock/data input.
12, 13	Q0, nQ0	Output		Differential output pair 0. LVDS interface levels.
14, 15	Q1, nQ1	Output		Differential output pair 1. LVDS interface levels.
16, 17	Q2, nQ2	Output		Differential output pair 2. LVDS interface levels.
18, 19	Q3, nQ3	Output		Differential output pair 3. LVDS interface levels.
21, 30	GND	Power		Power supply ground.
22, 23	Q4, nQ4	Output		Differential output pair 4. LVDS interface levels.
24, 25	Q5, nQ5	Output		Differential output pair 5. LVDS interface levels.
26, 27	Q6, nQ6	Output		Differential output pair 6. LVDS interface levels.
28, 29	Q7, nQ7	Output		Differential output pair 7. LVDS interface levels.
32, 33	Q8, nQ8	Output		Differential output pair 8. LVDS interface levels.
34, 35	Q9, nQ9	Output		Differential output pair 9. LVDS interface levels.
36, 37	Q10, nQ10	Output		Differential output pair 10. LVDS interface levels.
38, 39	Q11, nQ11	Output		Differential output pair 11. LVDS interface levels.

[a] *Pulldown* and *Pullup* refers to an internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Table 3. SEL Input Function Table[a]

Input	
SEL	**Operation**
0 (Default)	CLK0, nCLK0 is the selected differential clock input.
1	CLK1, nCLK1 is the selected differential clock input.

[a] SEL is an asynchronous control.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 10mA 15mA
Input Sink/Source, I_{REF}	±2mA
Maximum Junction Temperature, $T_{J,MAX}$	125°C
Storage Temperature, T_{STG}	-65°C to 150°C
ESD - Human Body Model[a]	2000V
ESD - Charged Device Model$^{\text{Note 1.}}$	1500V

[a] According to JEDEC JS-001-2012/JESD11-C101E.

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 1.8V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		1.71	1.8	1.89	V
I_{DD}	Power Supply Current	Q0 to Q11 terminated 100Ω between nQx, Qx		185	227	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 1.8V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			0.65 * V_{DD}		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.35 * V_{DD}	V
I_{IH}	Input High Current	SEL	$V_{DD} = V_{IN}$ = 1.89V			150	µA
I_{IL}	Input Low Current	SEL	V_{DD} = 1.89V, V_{IN} = 0V	-10			µA

Table 4C. Differential Inputs Characteristics, V_{DD} = 1.8V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0, CLK1, nCLK0, nCLK1	V_{IN} = V_{DD} = 1.89V			150	µA
I_{IL}	Input Low Current	CLK0, CLK1	V_{IN} = 0V, V_{DD} = 1.89V	-10			µA
		nCLK0, nCLK1	V_{IN} = 0V, V_{DD} = 1.89V	-150			µA
V_{REF}	Reference Voltage for Input Bias[a]		I_{REF} = +100µA, V_{DD} = 1.8V	0.9		1.30	V
V_{PP}	Peak-to-Peak VoltageNote3.		V_{DD} = 1.89V	0.2		1.0	V
V_{CMR}	Common Mode Input Voltage[b] [c]			0.9		V_{DD} – (V_{PP}/2)	V

[a] V_{REF} specification is applicable to the AC-coupled input interfaces shown in *Figures 2B and 2C.*

[b] Common mode input voltage is defined as crosspoint voltage.

[c] V_{IL} should not be less than -0.3V and V_{IH} should not be higher than V_{DD}.

Table 4D. LVDS DC Characteristics, V_{DD} = 1.8V ± 5%, T_A = -40°C to 85°C **[a]**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage	outputs loaded with 100Ω	247		454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.00		1.40	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

[a] Output drive current must be sufficient to drive up to 30cm of PCB trace (assume nominal 50Ω impedance).

AC Electrical Characteristics

Table 5. AC Electrical Characteristics, V_{DD} = 1.8V ± 5%, T_A = -40°C to 85°C[a]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Frequency	CLK[0:1], nCLK[0:1]				1.2	GHz
$\Delta V/\Delta t$	Input Edge Rate	CLK[0:1], nCLK[0:1]		1.5			V/ns
t_{PD}	Propagation Delay[b] [c]		CLK[0:1]; nCLK[0:1] to any Qx, nQx	200	340	450	ps
*t*sk(o)	Output Skew[d] [e]				10	45	ps
*t*sk(i)	Input SkewNote 5.				5	45	ps
*t*sk(p)	Pulse Skew		f_{REF} = 100MHz		3	20	ps
*t*sk(pp)	Part-to-Part Skew[f]					250	ps
t_{JIT}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section		f_{REF} = 122.88MHz Square Wave, V_{PP} = 1V, Integration Range: 1kHz – 40MHz		89	200	fs
			f_{REF} = 122.88MHz Square Wave, V_{PP} = 1V, Integration Range: 10kHz – 20MHz		74	150	fs
			f_{REF} = 122.88MHz Square Wave, V_{PP} = 1V, Integration Range: 12kHz – 20MHz		74	150	fs
			f_{REF} = 156.25MHz Square Wave, V_{PP} = 1V, Integration Range: 1kHz – 40MHz		58	81	fs
			f_{REF} = 156.25MHz Square Wave, V_{PP} = 1V, Integration Range: 10kHz – 20MHz		41	60	fs
			f_{REF} = 156.25MHz Square Wave, V_{PP} = 1V, Integration Range: 12kHz – 20MHz		41	60	fs
			f_{REF} = 156.25MHz Square Wave, V_{PP} = 0.5V, Integration Range: 1kHz – 40MHz		85	123	fs
			f_{REF} = 156.25MHz Square Wave, V_{PP} = 0.5V, Integration Range: 10kHz – 20MHz		61	87	fs
			f_{REF} = 156.25MHz Square Wave, V_{PP} = 0.5V, Integration Range: 12kHz – 20MHz		61	87	fs
t_R / t_F	Output Rise/ Fall Time		10% to 90%, outputs loaded with 100 Ω		225	400	ps
			20% to 80%, outputs loaded with 100 Ω		110	260	ps
$MUX_{ISOLATION}$	Mux Isolation[g]		f_{REF} = 100MHz		72.6		dB

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] Measured from the differential input crossing point to the differential output crossing point

[c] Input V_{PP} = 400mV

[d] Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

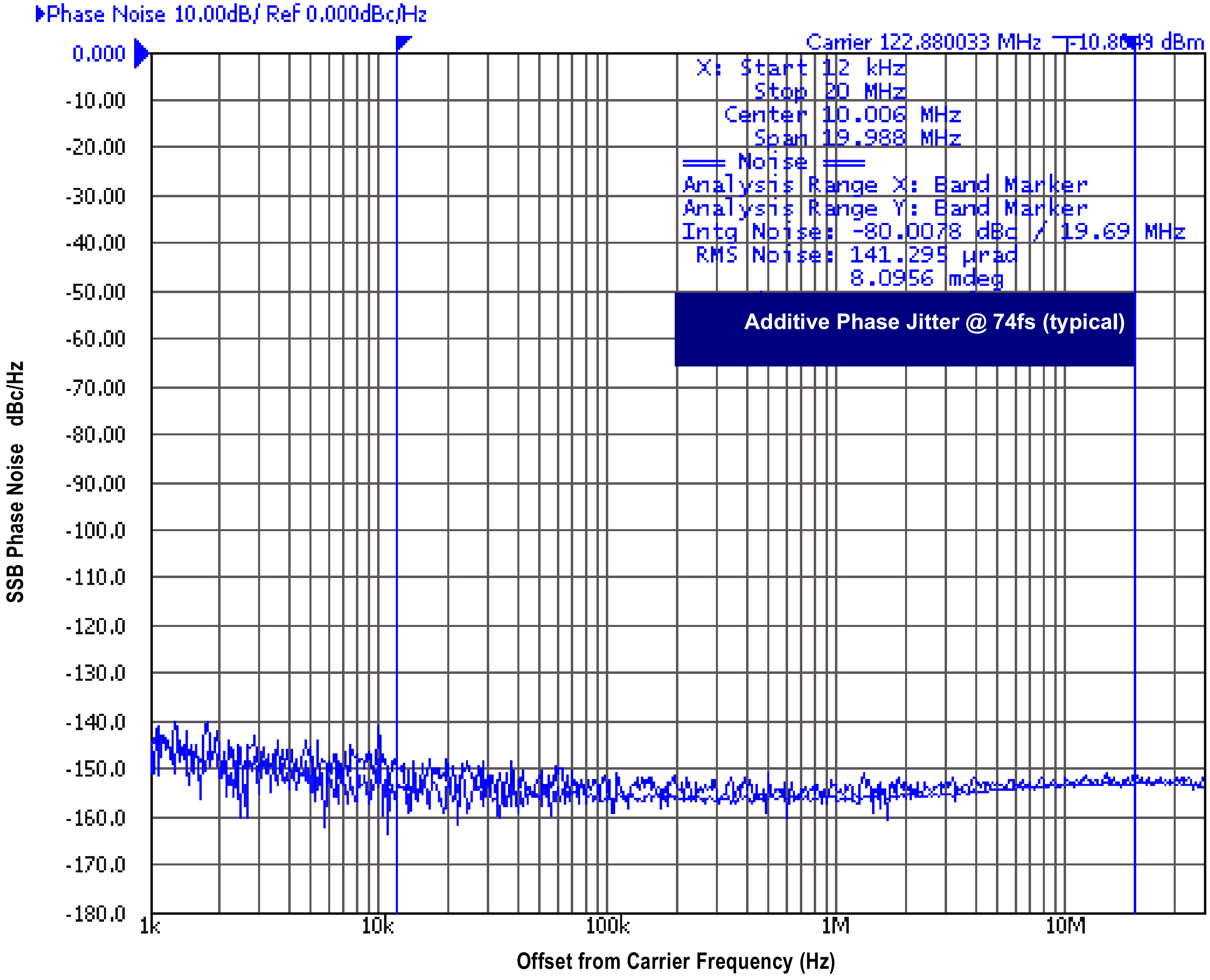
[e] This parameter is defined in accordance with JEDEC Standard 65.

[f] Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

[g] Qx, nQx outputs measured differentially. See *MUX Isolation diagram* in the *Parameter Measurement Information section.*

Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment.

Measured using a Wenzel Oscillator as the input source.

Additive Phase Jitter

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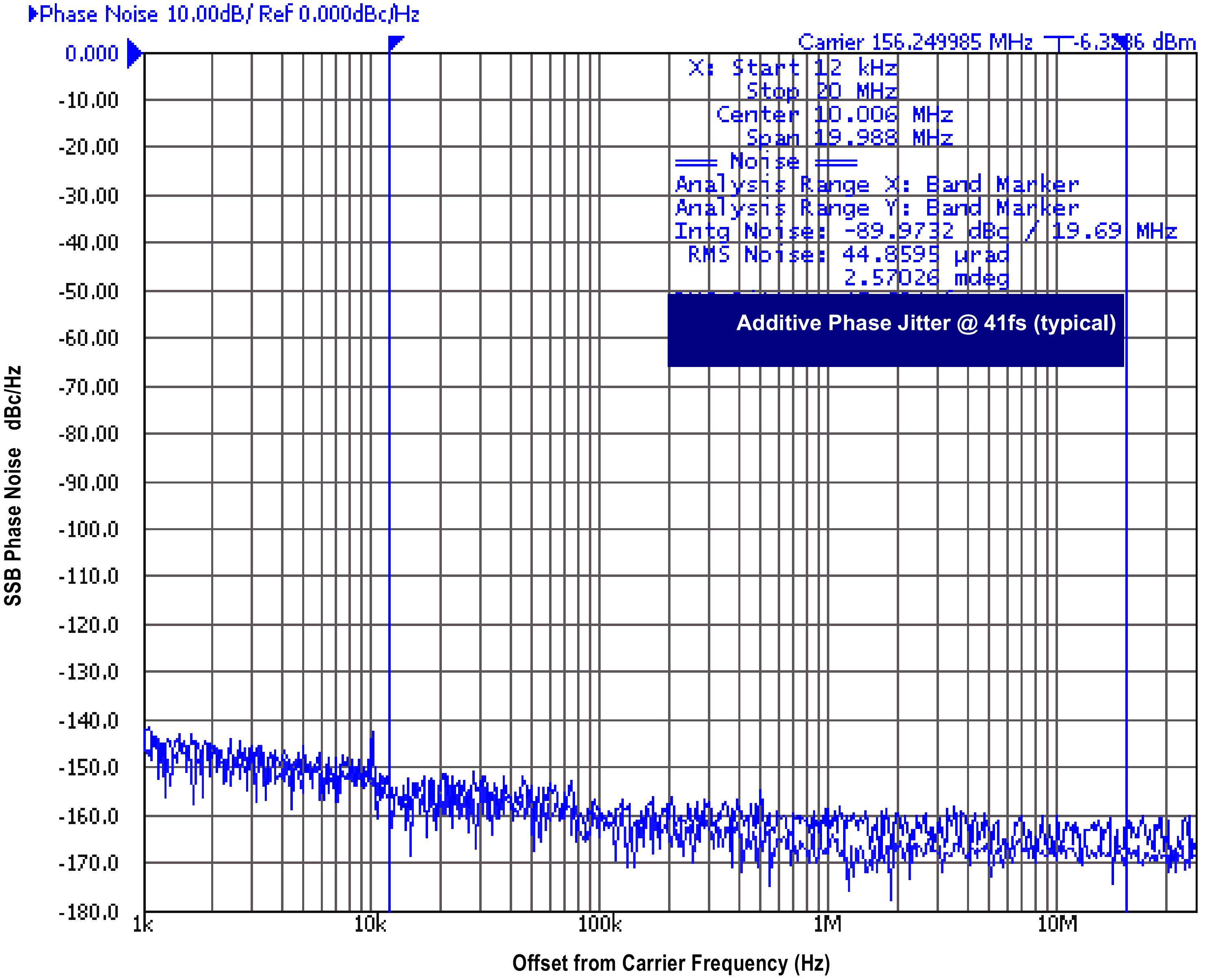

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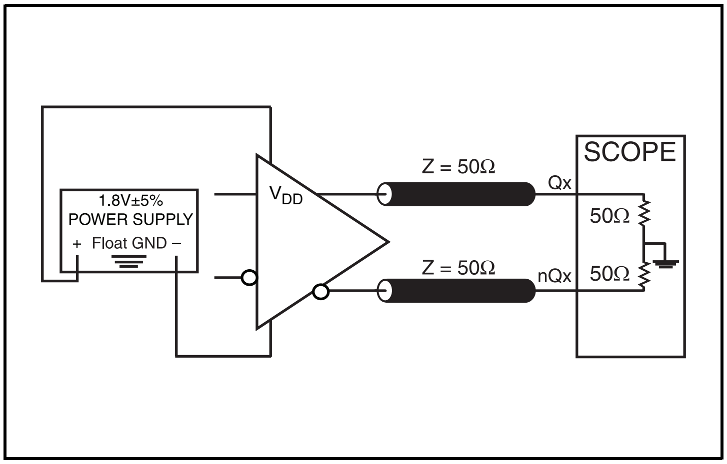
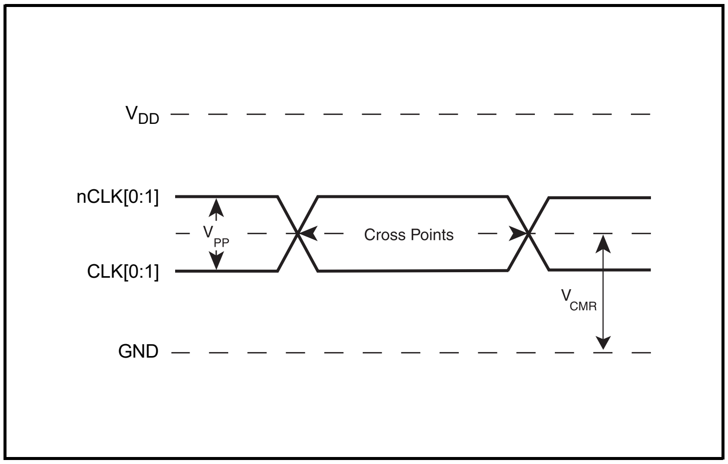
Measured using a Wenzel Oscillator as the input source.

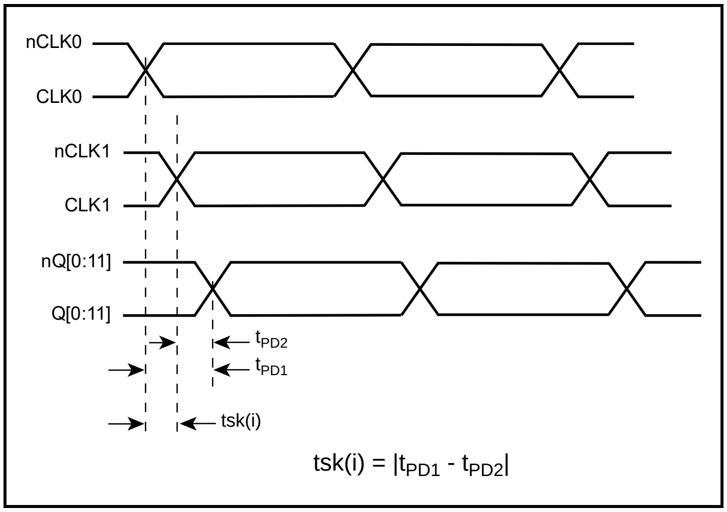
Parameter Measurement Information



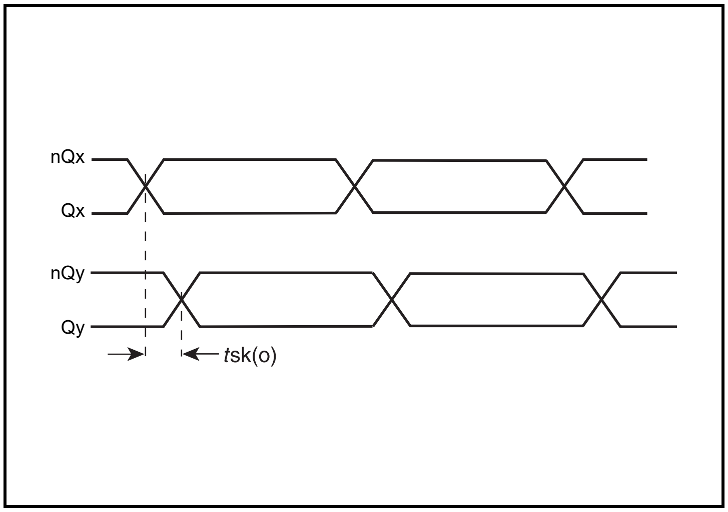
1.8V ±5% LVDS Output Load Test Circuit



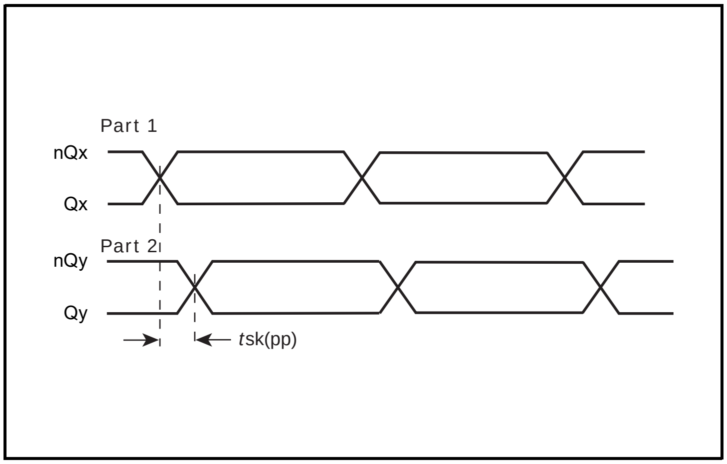
Differential Input Level



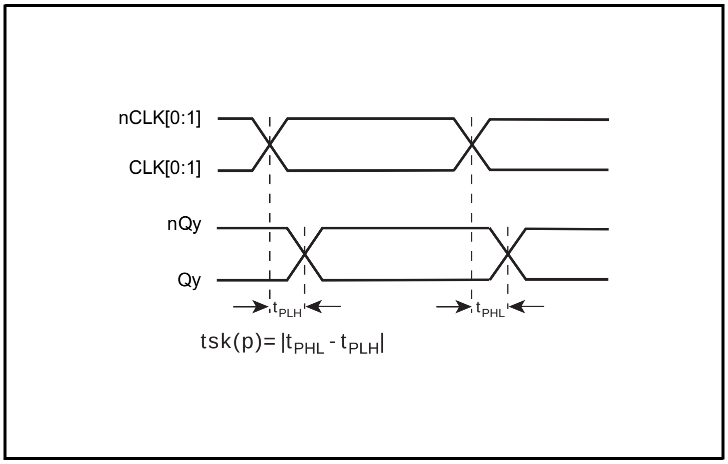
Input Skew



Output Skew

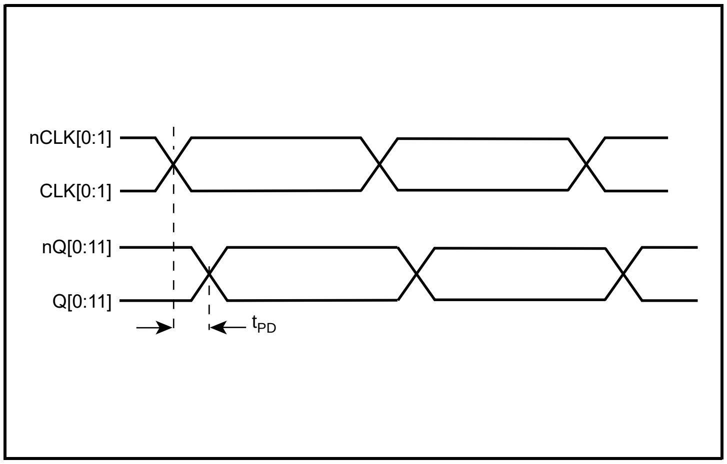


Part-to-Part Skew

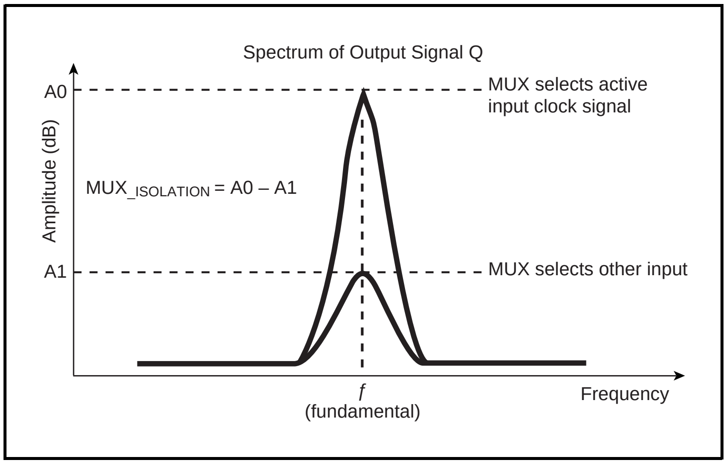


Pulse Skew

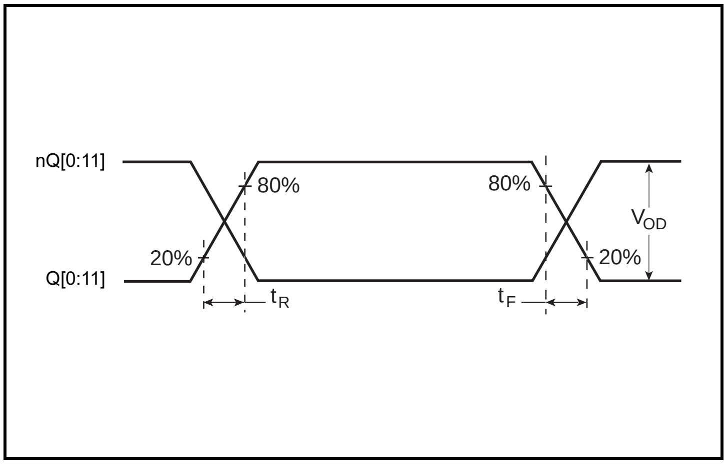
Parameter Measurement Information, continued



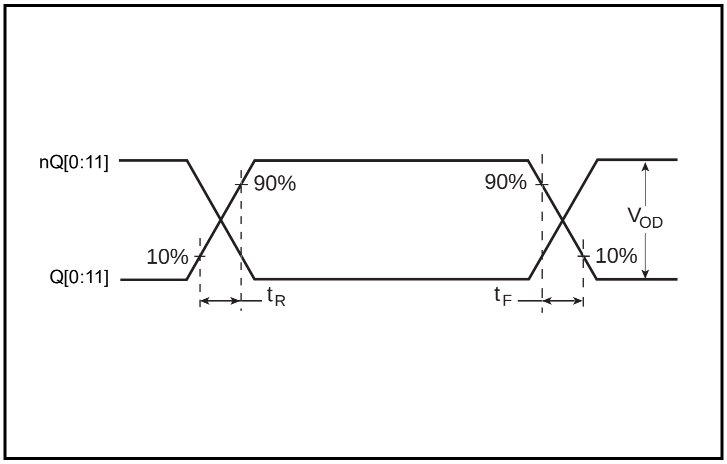
Propagation Delay



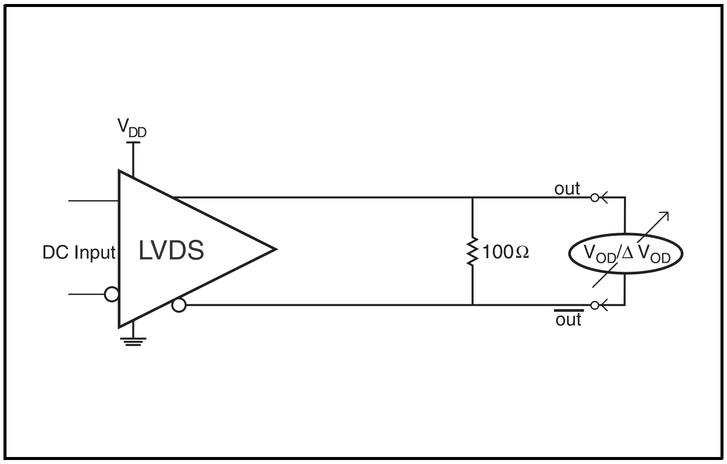
MUX Isolation



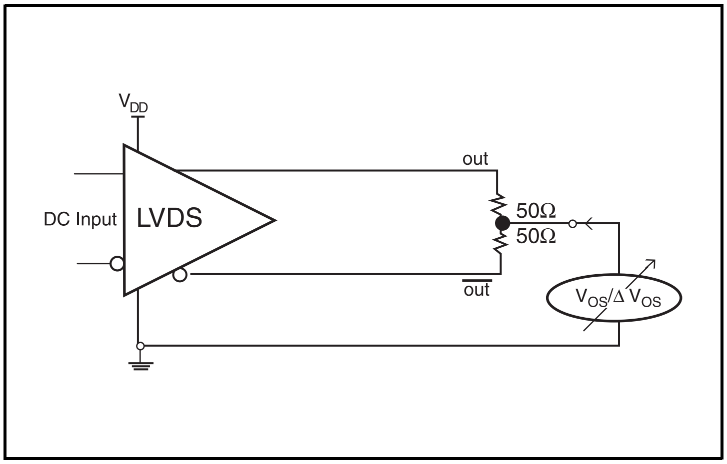
Output Rise/Fall Time, 20% – 80%



Output Rise/Fall Time, 10% – 90%



Differential Output Voltage Setup



Offset Voltage Setup

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1A and Figure 1B show examples of how a differential input can be wired to accept single-ended levels. The values below are for when both the single ended swing and VDD are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance and the signal DC offset after AC coupling should be equal to V1. For most Zo = 50Ω applications, R3 = 100Ω and R4 can be 100Ω.

By keeping the same R3/R4 ratio, the values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the input can handle larger amplitude signaling, it is recommended that the amplitude be reduced. For single-ended applications, the swing can be larger. Make sure the single-ended logic high and logic low signal operates within specification limit. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

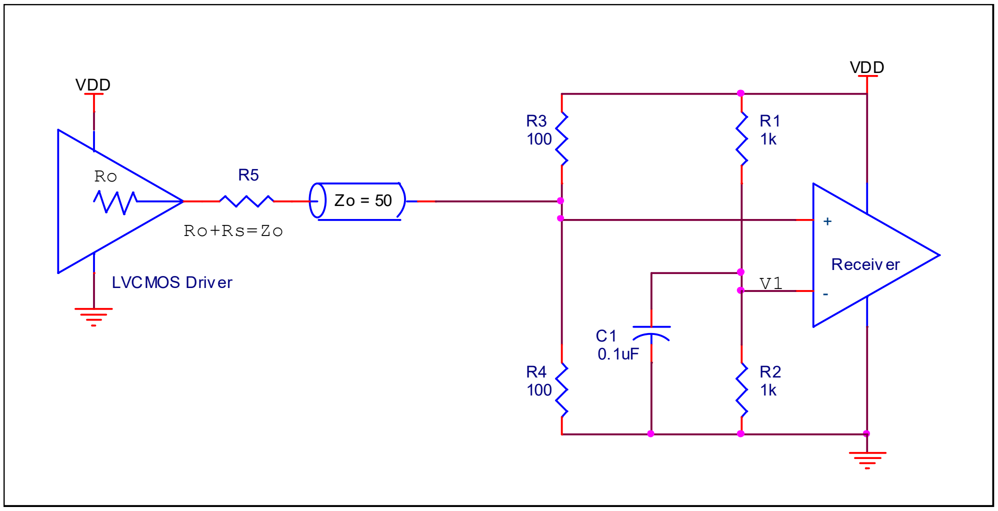


Figure 1A. DC Coupling Example for Wiring a Differential Input to Accept Single-ended Levels

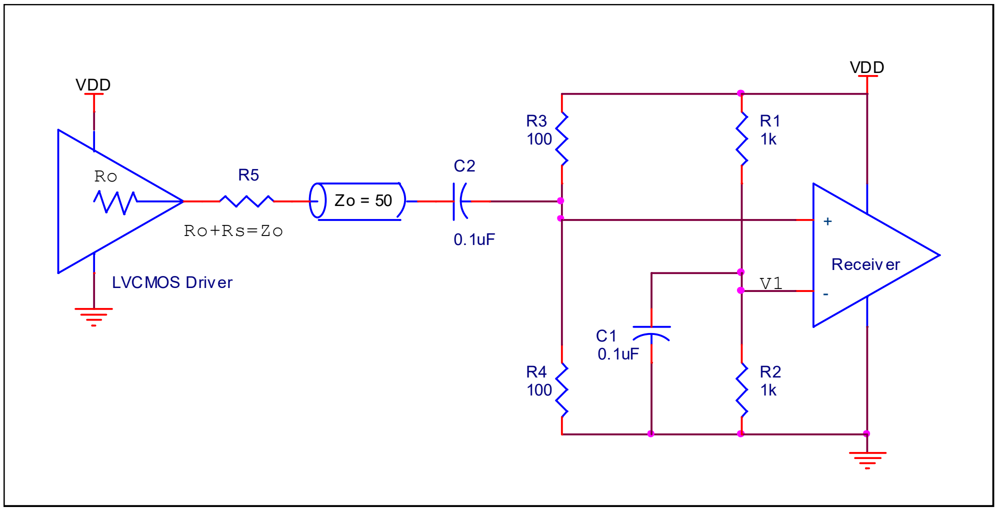


Figure 1B. AC Coupling Example for Wiring a Differential Input to Accept Single-ended Levels

Recommendations for Unused Input and Output Pins

Inputs

CLK/nCLK Inputs

For applications not requiring the use of a differential input, both the CLK and nCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Outputs

LVDS Outputs

Unused LVDS outputs must either have a 100Ω differential termination or have a 100Ω pull-up resistor to V_{DD} in order to ensure proper device operation.

1.8V Differential Clock Input Interface

The CLK /nCLK accepts LVDS and other differential signals. The differential input signal must meet both the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2D* show interface examples for the CLK /nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

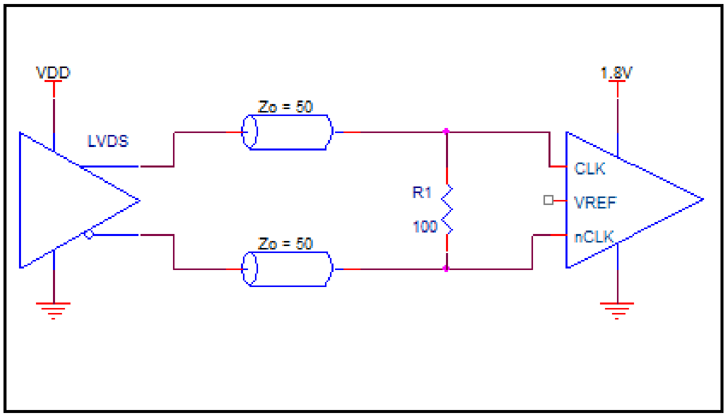


Figure 2A. Differential Input Driven by an LVDS Driver - DC Coupling

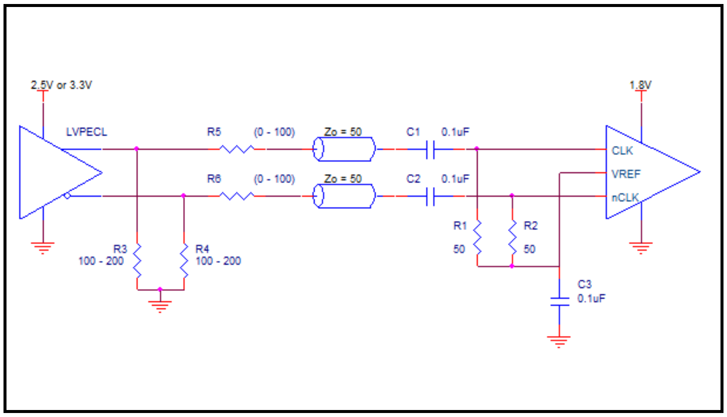


Figure 2B. Differential Input Driven by an LVPECL Driver - AC Coupling

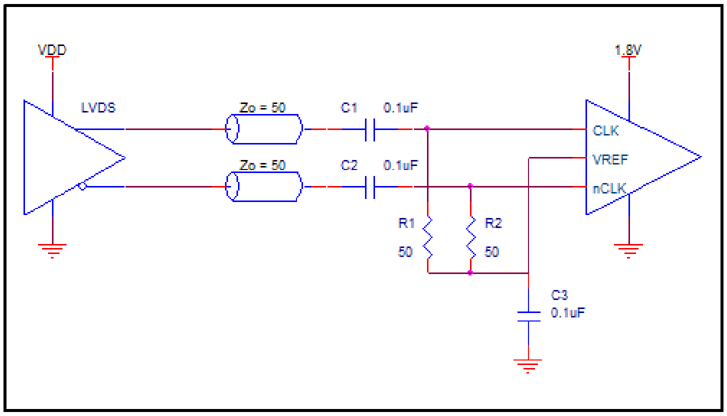


Figure 2C. Differential Input Driven by an LVDS Driver - AC Coupling

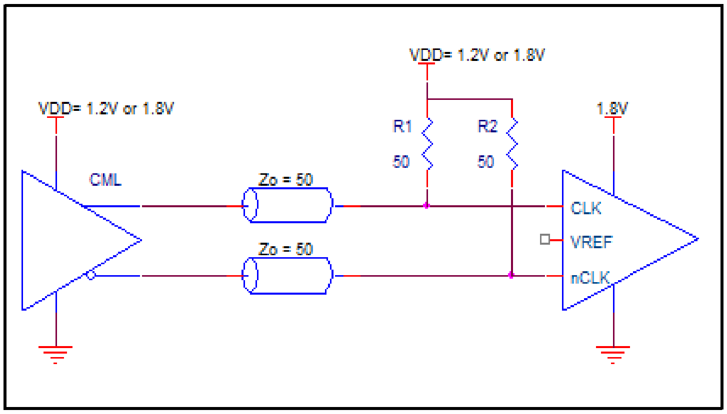


Figure 2D. Differential Input Driven by a CML Driver

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 3A* can be used with either type of output structure. *Figure 3B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

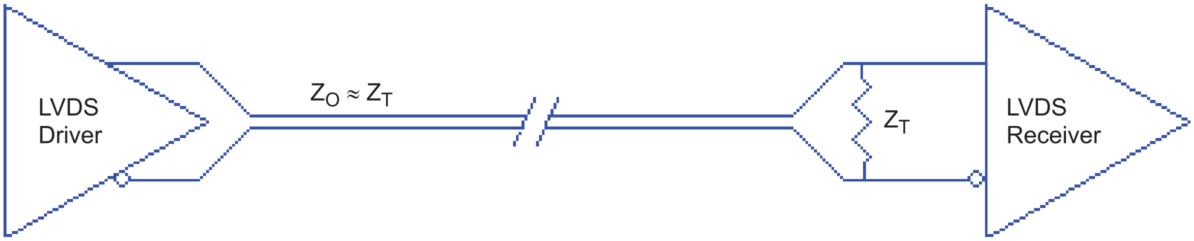


Figure 3A. Standard LVDS Termination

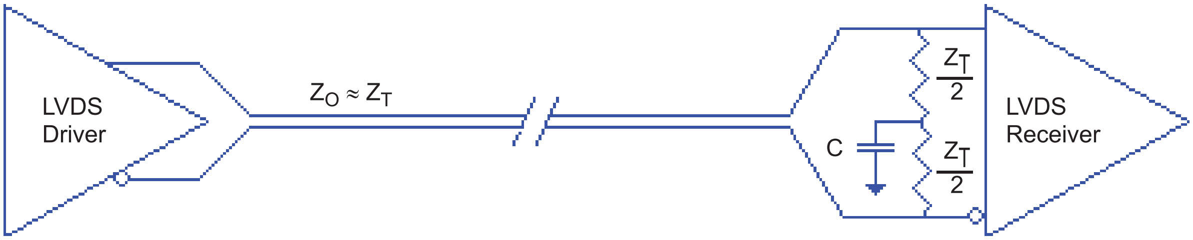


Figure 3B. Optional LVDS Termination

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

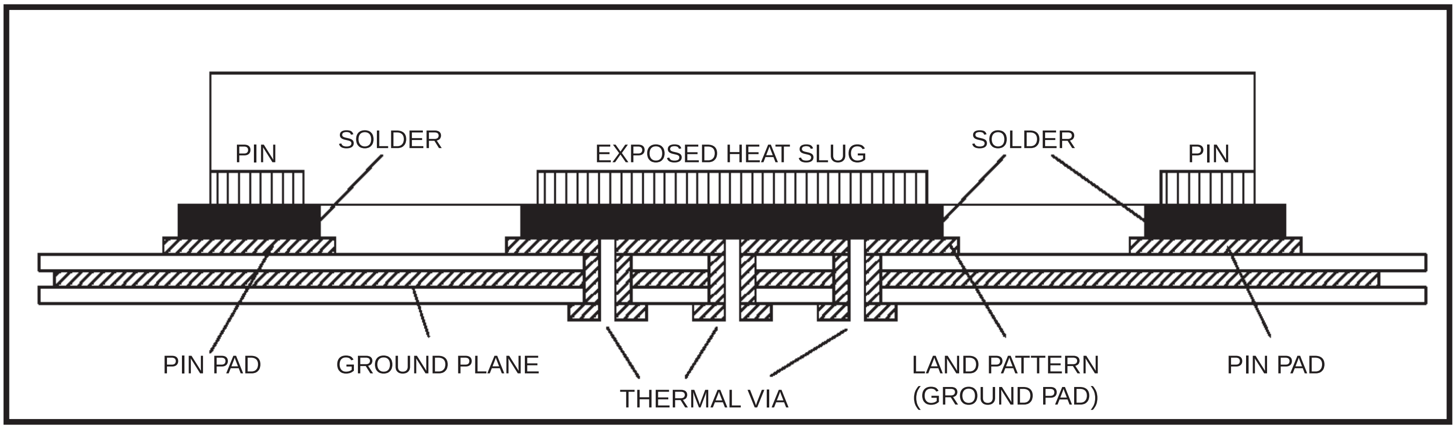


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8P34S1212I. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8P34S1212I is the sum of the core power plus the output power dissipation into the load. The following is the power dissipation for V_{DD} = 1.8V + 5% = 1.89V, which gives worst case results.

The maximum current at 85°C is as follows:

I_{DD_MAX} = 227mA

Power $_{(core)MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 1.89V * 227mA = **429.03mW**

Total Power$_{\_MAX}$ = 429.03mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + TA

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 33°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.429W * 33°C/W = 99.16°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. θ_{JA} vs. Air Flow Table for a 40-Lead VFQFN

θ_{JA} vs. Air Flow (m/s)			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	33.0°C/W	26.3C/W	24.0°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 40-Lead VFQFN

θ_{JA} **vs. Air Flow (m/s)**			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	33.0°C/W	26.3C/W	24.0°C/W

Transistor Count

The transistor count for the 8P34S1212I is: 8438

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/us/en/document/psc/nlnlg-40-package-outline-60-x-60-mm-body-epad-465-x-465-mm-qfn

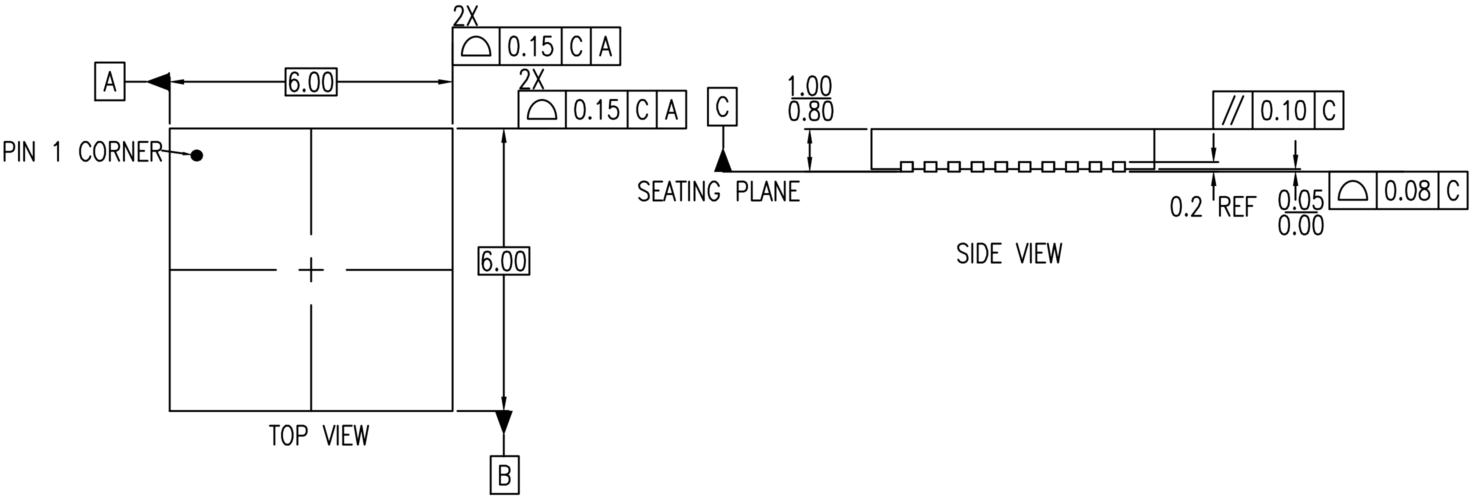
Ordering Information

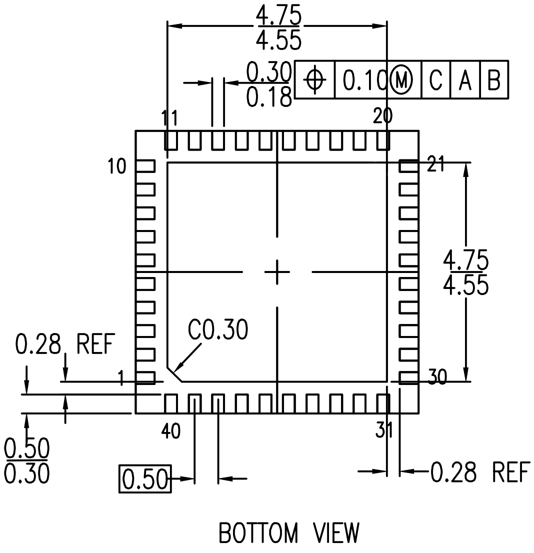
Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8P34S1212NLGI	IDT8P34S1212NLGI	“Lead-Free” 40-Lead VFQFN	Tray	-40°C to 85°C
8P34S1212NLGI8	IDT8P34S1212NLGI	“Lead-Free” 40-Lead VFQFN	Tape & Reel	-40°C to 85°C

Revision History

Revision Date	Description
September 4, 2020	Updated the section “Wiring the Differential Input to Accept Single-Ended Levels”.
November 24, 2017	Updated the description of pins 3, 8, and 9 in Table 1 Updated the package drawings; however, no technical changes Completed other minor changes
January 20, 2014	Initial release.





NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES