LVPECL Frequency-Programmable Crystal Oscillator

IDT8N3S270EC-1103

DATA SHEET

General Description

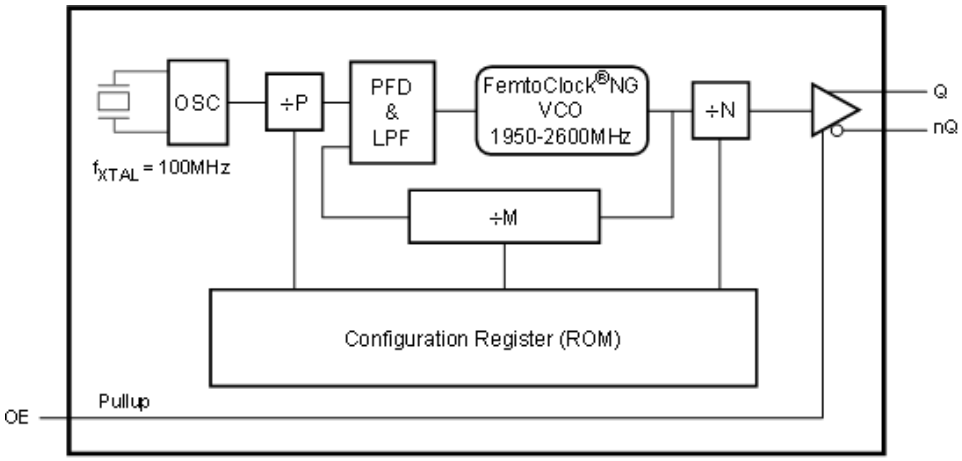
The ICS8N3S270EC-1103 is a Frequency-Programmable Crystal Oscillator with very flexible frequency programming capabilities. The device uses IDT's fourth generation FemtoClock® NG technology for an optimum of high clock frequency and low phase noise performance (<0.25ps RMS 12kHz - 20MHz, typical). The device accepts a 3.3V supply and is packaged in a small, lead-free (RoHS 6) 6-lead ceramic 5mm x 7mm x 1.55mm package.

The device is programmed for an output frequency of 240MHz. The extended temperature range supports wireless infrastructure, telecommunication and networking end equipment requirements.

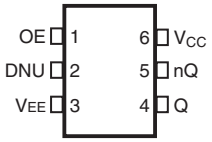
Features

- Fourth Generation FemtoClock® NG technology
- Factory-programmable clock output frequency of 240MHz
- One 3.3V LVPECL clock output
- Output enable control (positive polarity), LVCMOS/LVTTL compatible
- RMS phase jitter @ 240MHz (12kHz - 20MHz): 0.23ps (typical)
- RMS phase jitter @ 240MHz (1kHz - 40MHz): 0.26ps (typical)
- 3.3V supply
- -40°C to 85°C ambient operating temperature
- Available in a lead-free (RoHS 6) 6-pin ceramic package

Block Diagram



Pin Assignment



IDT8N3S270EC-1103
6-lead ceramic 5mm x 7mm x 1.55mm package body
CD Package
Top View

Pin Description and Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1	OE	Input	Pullup	Output enable pin. See Table 3A for function. LVCMOS/LVTTL interface levels.
2	DNU			Do not use (factory use only).
3	V_{EE}	Power		Negative power supply.
4, 5	Q, nQ	Output		Differential clock output. LVPECL interface levels.
6	V_{CC}	Power		Positive power supply.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	OE			5.5		pF
R_{PULLUP}	Input Pullup Resistor				50		kΩ

Function Tables

Table 3. OE Configuration

Input	
OE	Output Enable
0	Outputs Q, nQ are in high-impedance state.
1 (default)	Outputs are enabled.

NOTE: OE is an asynchronous control.

Principles of Operation

The ICS8N3S270EC-1103 uses a fractional feedback-divider synthesizer core with a Delta-Sigma modulator for noise shaping and is very robust in its frequency synthesis capability. Output frequencies are synthesized from an internal 100MHz third overtone crystal (f_{XTAL})in order to minimize phase noise generation by frequency multiplication. The higher frequency reference crystal also allows more efficient “shaping” of noise by the Delta-Sigma modulator.

The device supports a factory-programmed output frequency of 240MHz.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	3.63V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	49.4°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				148	mA

Table 4B. LVPECL DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} – 1.3		V_{CC} – 0.8	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} – 2.0		V_{CC} – 1.6	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} – 2V.

Table 4C. LVCMOS/LVTTL DC Characteristic, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.3V	2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = V_{IN} = 3.465V	-0.3		0.8	V
I_{IH}	Input High Current	OE	V_{CC} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	OE	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA

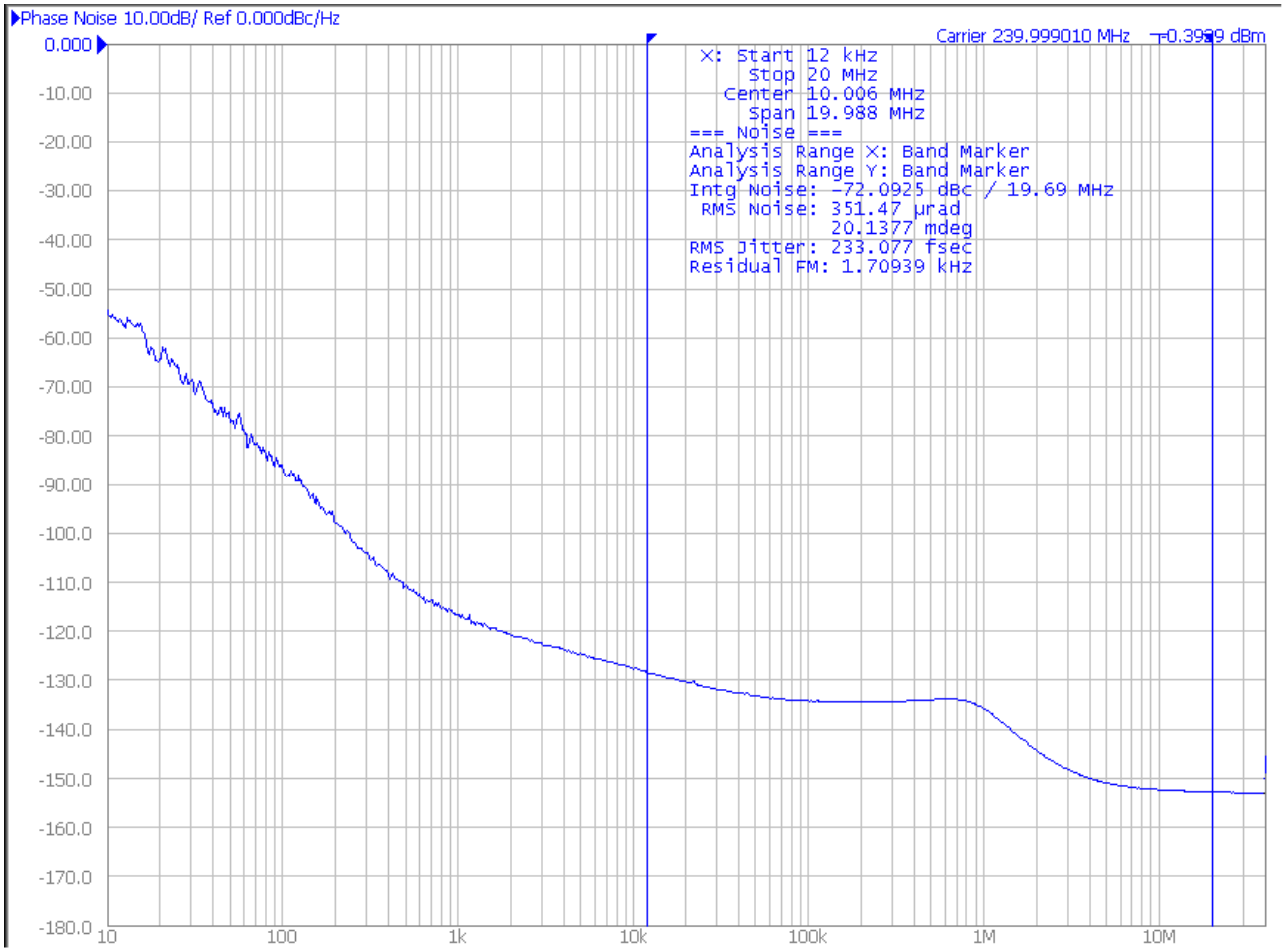
AC Electrical Characteristics

Table 5. AC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency Q, nQ				240	MHz
f_I	Initial Accuracy	Measured @ 25°C			±5	ppm
f_S	Temperature Stability				±50	ppm
f_A	Aging	Frequency drift over 10 year life			±3	ppm
		Frequency drift over 15 year life			±5	ppm
f_T	Total Stability	Over 10 year life			±58	ppm
t_{jit}(cc)	Cycle-to-Cycle Jitter; NOTE 1				15	ps
t_{jit}(per)	Period Jitter (RMS); NOTE 1			2	3	ps
t_{jit}(Ø)	RMS Phase Jitter (Random); NOTE 2	240MHz, Integration Range: 12kHz - 20MHz		0.23	0.28	ps
t_{jit}(Ø)	RMS Phase Jitter (Random); NOTE 2	240MHz, Integration Range: 1kHz - 40MHz		0.26	0.32	ps
Φ_N(100)	Single-side band phase noise, 100Hz from Carrier	240MHz		-89		dBc/Hz
Φ_N(1k)	Single-side band phase noise, 1kHz from Carrier	240MHz		-117		dBc/Hz
Φ_N(10k)	Single-side band phase noise, 10kHz from Carrier	240MHz		-127		dBc/Hz
Φ_N(100k)	Single-side band phase noise, 100kHz from Carrier	240MHz		-134		dBc/Hz
Φ_N(1M)	Single-side band phase noise, 1MHz from Carrier	240MHz		-136		dBc/Hz
Φ_N(10M)	Single-side band phase noise, 10MHz from Carrier	240MHz		-153		dBc/Hz
t_R / t_F	Output Rise/Fall Time	20% to 80%	150		300	ps
odc	Output Duty Cycle		48		52	%
$t_{STARTUP}$	Device startup time after power up				20	ms

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: This parameter is defined in accordance with JEDEC standard 65.
NOTE 2: Refer to the phase noise plot.

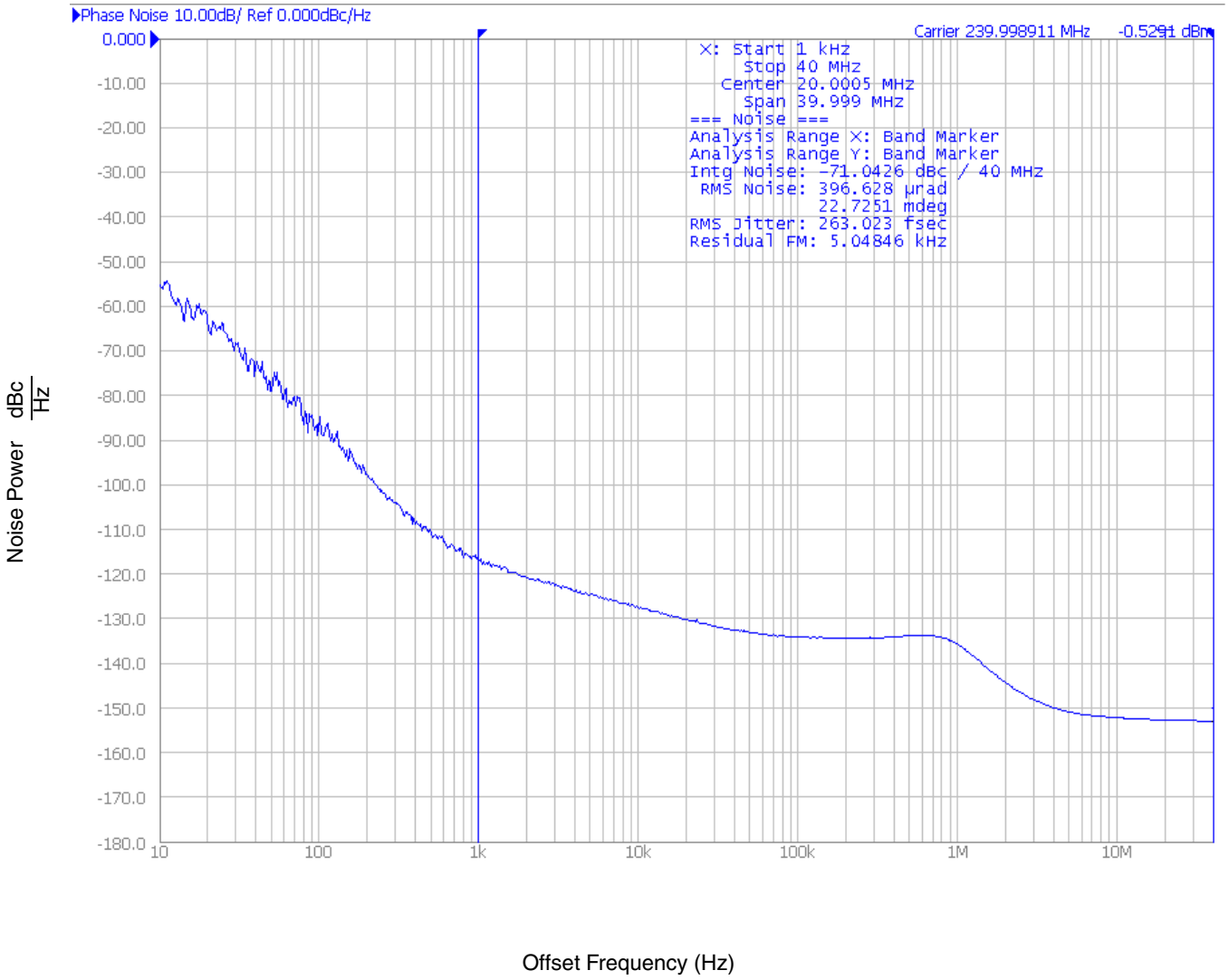
Typical Phase Noise at 240MHz



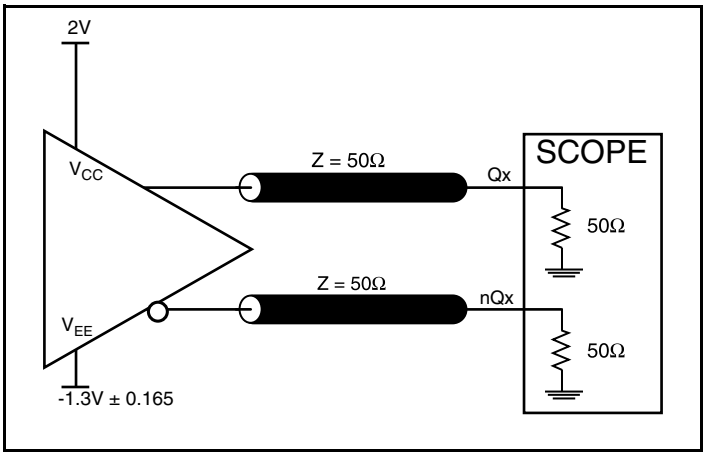
Noise Power dBc

Offset Frequency (Hz)

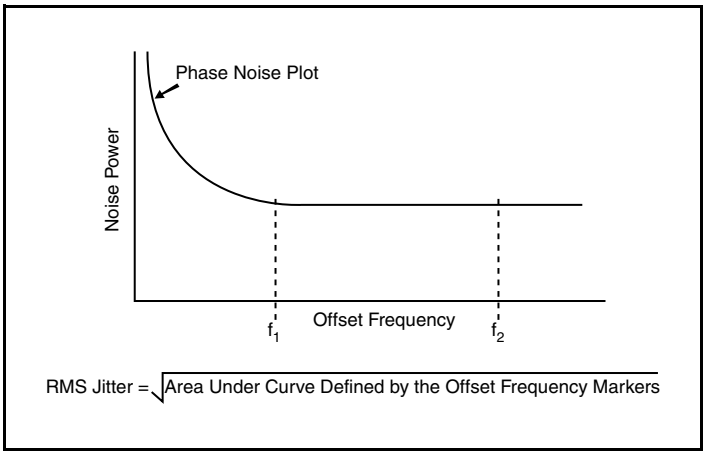
Typical Phase Noise at 240MHz continued



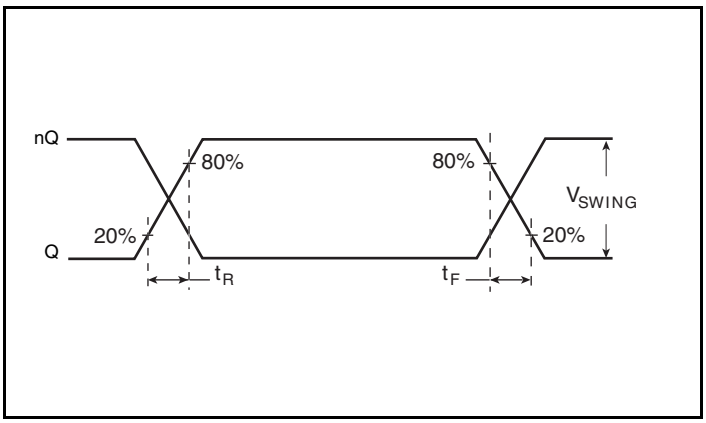
Parameter Measurement Information



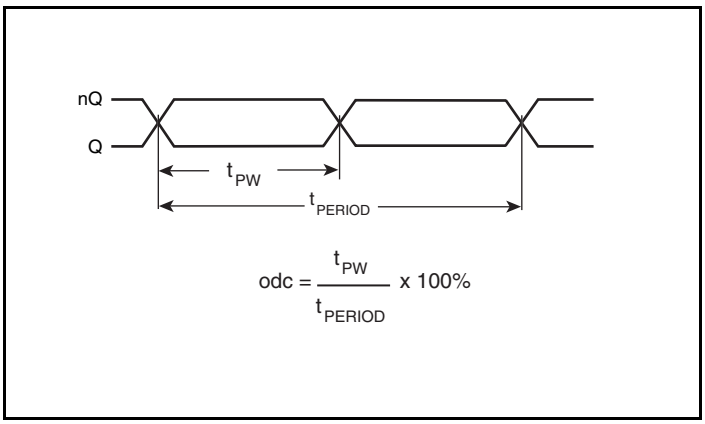
3.3V LVPECL Output Load AC Test Circuit



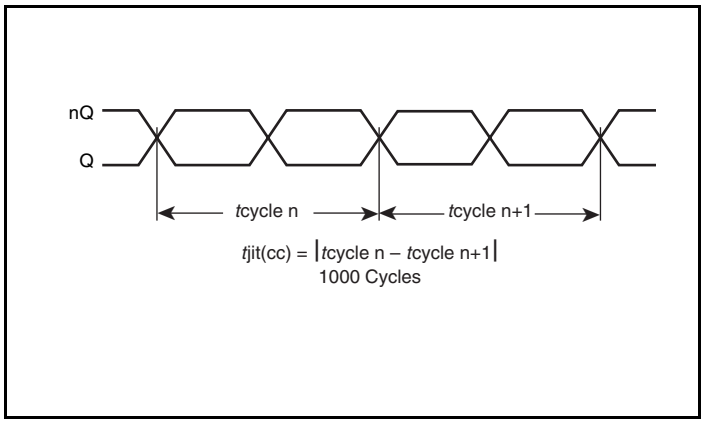
RMS Phase Jitter



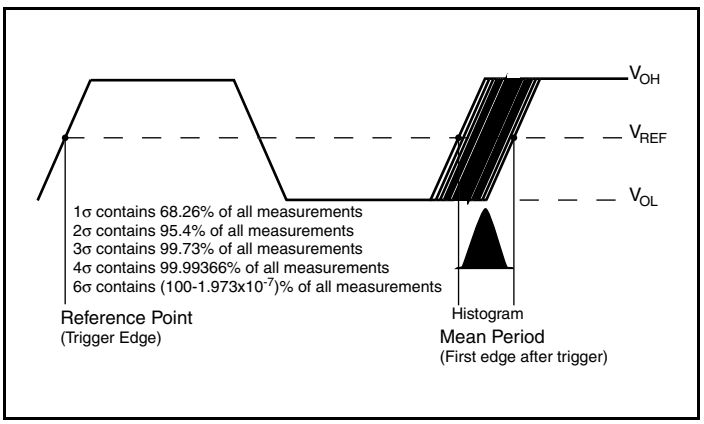
Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period



Cycle-to-Cycle Jitter



Period Jitter

Applications Information

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 1A and 1B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

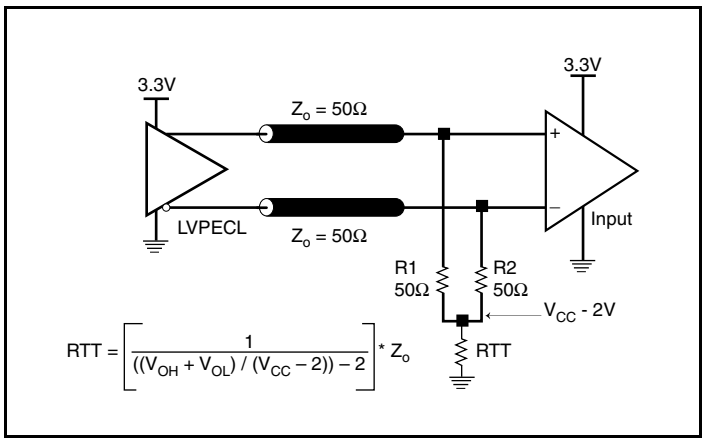


Figure 1A. 3.3V LVPECL Output Termination

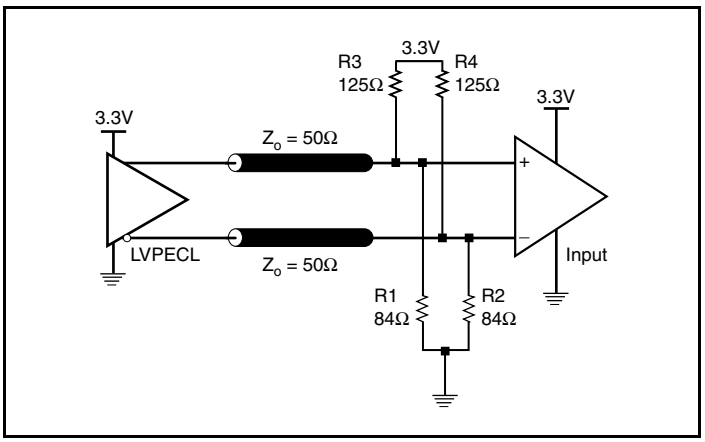


Figure 1B. 3.3V LVPECL Output Termination

Schematic Layout

Figure 2 shows an example of IDT8N3S270EC-1103 application schematic. In this example, the device is operated at V_{CC} = 3.3V. As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1µF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set.

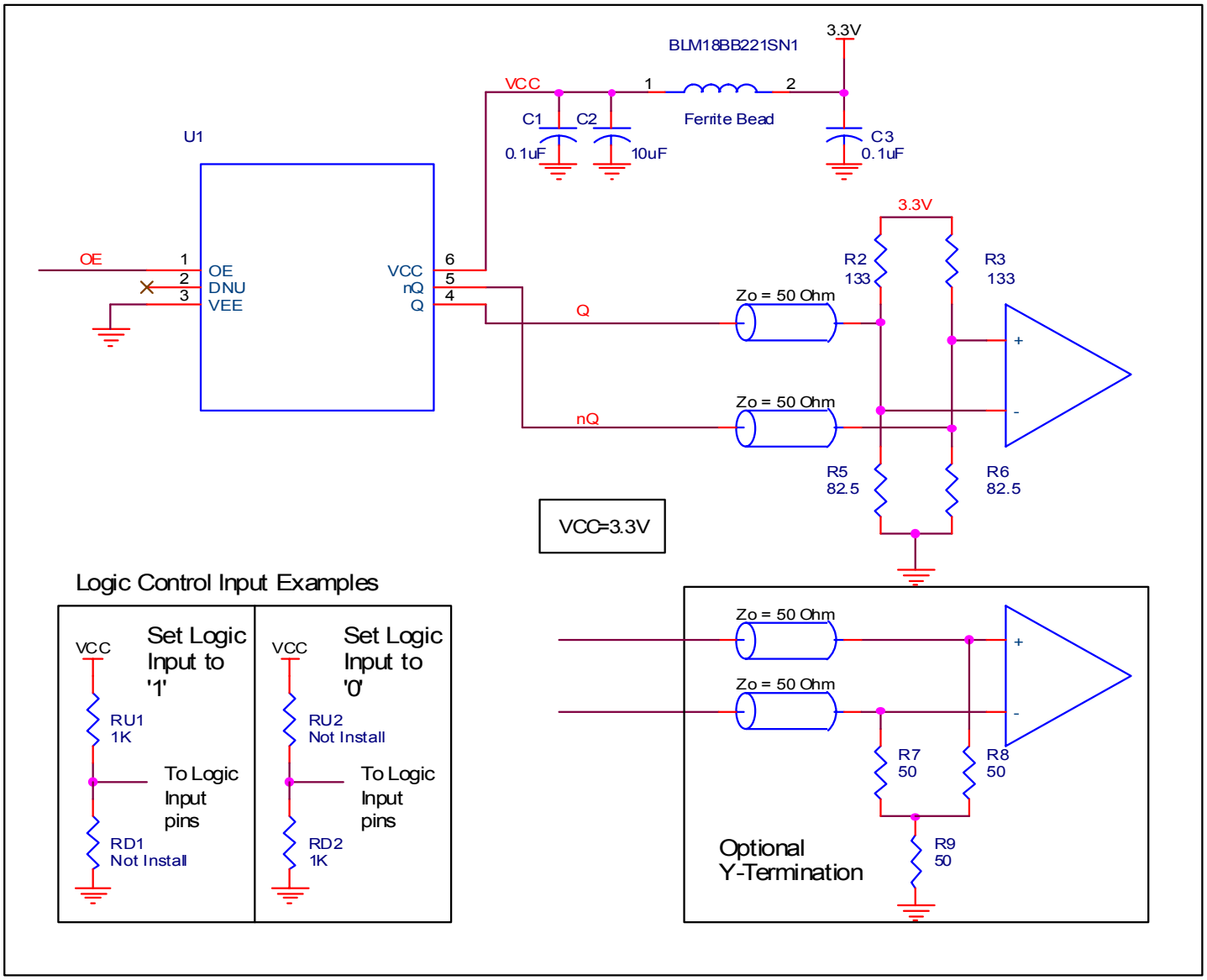


Figure 2. IDT8N3S270EC-1103 Application Schematic

Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8N3S270EC-1103. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8N3S270EC-1103 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{CC} = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 148mA = **512.82mW**
- Power (outputs)$_{MAX}$ = **32mW/Loaded Output pair**

  Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 512.82mW + 32mW = 544.82mW

2. Junction Temperature.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 49.4°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.545W * 49.4°C/W = 111.9°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 6 Lead Ceramic VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	49.4°C/W	44.2°C/W	42.1°C/W

3. Calculations and Equations.

LVPECL output driver circuit and termination are shown in *Figure 3.*

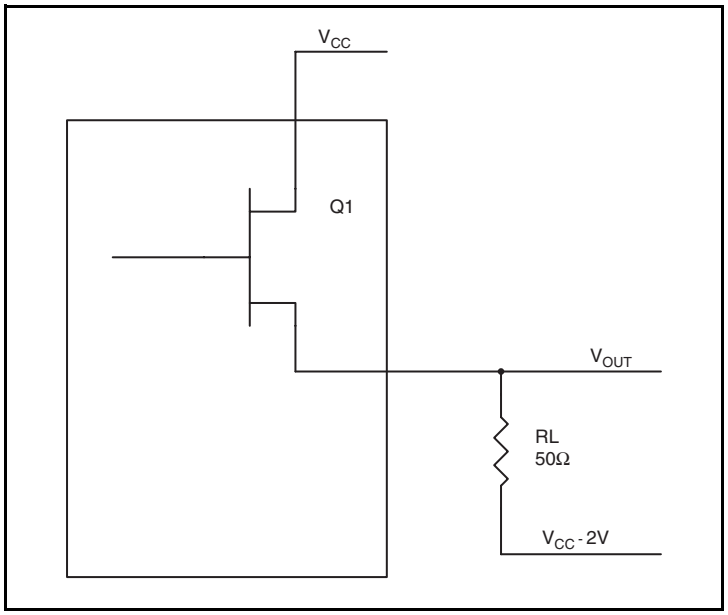


Figure 3. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 0.8V}$
  $(V_{CC\_MAX} – V_{OH\_MAX}) = \mathbf{0.8V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.6V}$
  $(V_{CC\_MAX} – V_{OL\_MAX}) = \mathbf{1.6V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.8V)/50\Omega] * 0.8V =$ **19.2mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.6V)/50\Omega] * 1.6V =$ **12.8mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **32mW**

Reliability Information

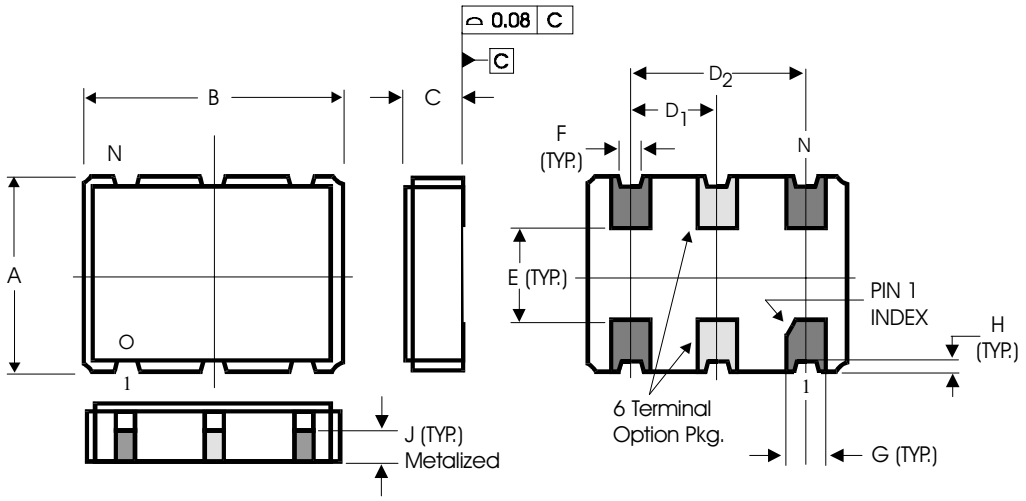
Table 7. θ_{JA} vs. Air Flow Table for a 6-lead Ceramic 5mm x 7mm Package

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	49.4°C/W	44.2°C/W	42.1°C/W

Transistor Count

The transistor count for IDT8N3S270EC-1103 is: 47,511

Package Outline and Package Dimensions



SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	4.85	5.00	5.15
B	6.85	7.00	7.15
C	1.35	1.50	1.65
D_1	2.41	2.54	2.67
D_2	4.95	5.08	5.21
E	2.47	2.6	2.73
F	0.47	0.60	0.73
G	1.27	1.40	1.53
H	-	0.15 Ref.	-
J	-	0.65 Ref.	-

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8N3S270EC-1103CDI	IDT8N3S270EC-1103CDI	“Lead-Free” 6 lead Ceramic DIP	Tray	-40°C to 85°C
8N3S270EC-1103CDI8	IDT8N3S270EC-1103CDI	“Lead-Free” 6 lead Ceramic DIP	2500 Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		4	Absolute Maximum Rating - corrected Package Thermal Impedance.	4/27/12
	T6	11	Power Considerations - corrected Thermal Resistance table, updated Junction Temperture calculation.	
	T7	13	Corrected Air Flow table.	

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