

### General Description

The ICS8N3PGDAMBKI-025 is a very versatile programmable LVPECL synthesizer that can be used for OTN/SONET to Ethernet or 10 GB Ethernet to OTN/SONET rate conversions. The conversion rate is pin-selectable and one of the four rates is supported at a time. In the default configuration, an input clock of 161.1328MHz is converted to 25MHz output.

The device uses IDT's fourth generation FemtoClock NG technology to deliver low phase noise clocks combined with low power consumption. The RMS phase jitter at 25MHz output frequency is 0.66ps (12kHz - 5MHz integration range).

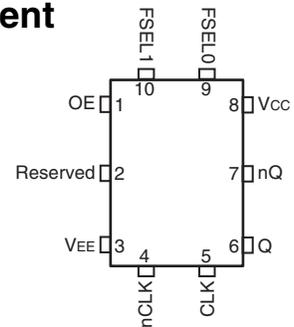
### Features

- Fourth Generation FemtoClock® Next Generation (NG) technology
- Footprint compatible with 5mm x 7mm differential oscillators
- One differential LVPECL output pair
- CLK, nCLK input pair can accept the following levels: HCSL, LVDS, LVPECL, LVHSTL and SSTL
- Output frequencies: 19.44MHz and 25MHz
- VCO range: 2.0GHz – 2.5GHz
- Cycle-to-cycle jitter: 30ps (maximum)
- RMS phase jitter, 12kHz – 5MHz: 0.66ps (typical)
- Full 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

### Frequency Select Table

FSEL[1:0]	Input (MHz)	Output Frequency (MHz)
00	161.1328	25
01	156.25	25
10	161.1328	19.44
11	156.25	19.44 (default)

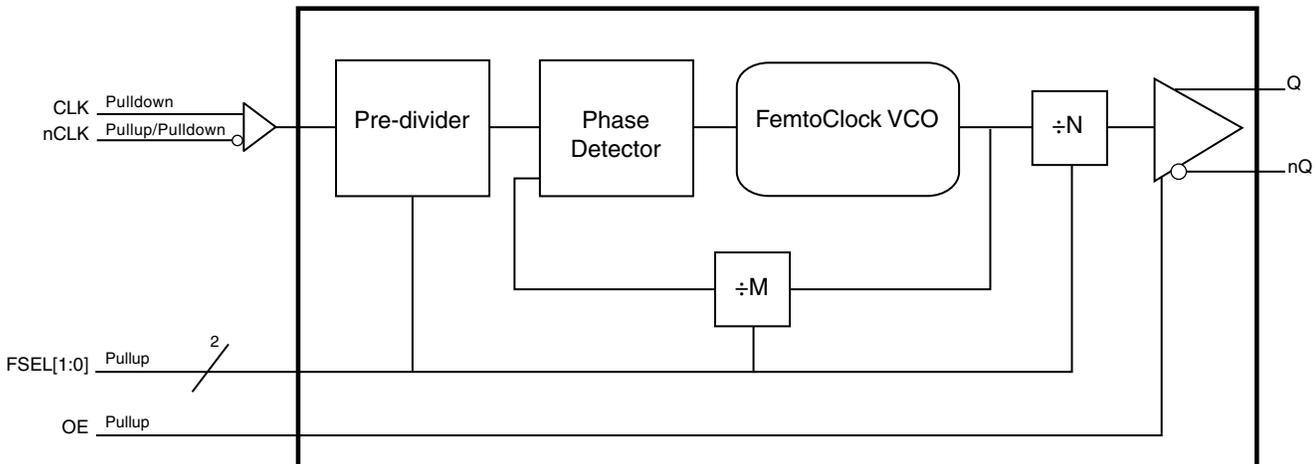
### Pin Assignment



ICS8N3PGDAMBKI-025

10-Lead VFQFN  
5mm x 7mm x 1mm package body  
K Package  
Top View

### Block Diagram



### Table 1. Pin Descriptions

Number	Name	Type		Description
1	OE		Pullup	Output enable. External pullup required for normal operation. LVCMOS/LVTTL interface levels.
2	Reserved	Reserve		Reserved pin.
3	V <sub>EE</sub>	Power		Negative supply pin.
4	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. V <sub>CC</sub> /2 default when left floating
5	CLK	Input	Pulldown	Non-inverting differential clock input.
6, 7	Q, nQ	Output		Differential output pair. LVPECL interface levels.
8	V <sub>CC</sub>	Power		Power supply pin.
9	FSEL0	Input	Pullup	Feedback control input. Sets the output divider value to one of four values. LVCMOS/LVTTL interface levels. See <i>Frequency Select Table</i> on page 1.
10	FSEL1	Input	Pullup	Feedback control input. Sets the output divider value to one of four values. LVCMOS/LVTTL interface levels. See <i>Frequency Select Table</i> on page 1.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

### Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			3.5		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

## Function Table

### Table 3. P, M, N Divider Function Table

FSEL[1:0]	P	M	N	Input Frequency (MHz)	Output Frequency (MHz)
0 0	÷2	26.0653	÷84	161.1328	25
0 1	÷2	27.5200	÷86	156.25	25
1 0	÷2	27.5071	÷114	161.1328	19.44
1 1 (default)	÷2	28.3668	÷114	156.25	19.44

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{CC}$	3.63V
Inputs, $V_I$	-0.5V to $V_{CC} + 0.5V$
Outputs, $I_O$ Continuous Current Surge Current	50mA 100mA
Package Thermal Impedance, $\theta_{JA}$	39.2°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Power Supply Voltage		3.135	3.3	3.465	V
$I_{EE}$	Power Supply Current				189	mA

**Table 4B. Power Supply DC Characteristics,  $V_{CC} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Power Supply Voltage		2.375	2.5	2.625	V
$I_{EE}$	Power Supply Current				182	mA

**Table 4C. LVCMOS/LVTTL DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	$V_{CC} = 3.465V$	2		$V_{CC} + 0.3$	V
		$V_{CC} = 2.625V$	1.7		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage	$V_{CC} = 3.465V$	-0.3		0.8	V
		$V_{CC} = 2.625V$	-0.3		0.7	V
$I_{IH}$	Input High Current	FSEL[1:0] $V_{CC} = V_{IN} = 3.465V$ or $2.625V$			5	$\mu A$
$I_{IL}$	Input Low Current	FSEL[1:0] $V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-150			$\mu A$

**Table 4D. Differential DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	CLK, nCLK	$V_{CC} = V_{IN} = 3.465V$ or $2.625V$			150	$\mu A$
$I_{IL}$	Input Low Current	CLK	$V_{IN} = 0V$ , $V_{CC} = 3.465V$ or $2.625V$	-5			$\mu A$
		nCLK	$V_{IN} = 0V$ , $V_{CC} = 3.465V$ or $2.625V$	-150			$\mu A$
$V_{PP}$	Peak-to-Peak Voltage			0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1			$V_{EE}$		$V_{CC} - 0.85$	V

NOTE 1: Common mode input voltage is defined as the crossing point.

**Table 4E. LVPECL DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CC} - 1.4$		$V_{CC} - 0.9$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$		$V_{CC} - 1.7$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs termination with  $50\Omega$  to  $V_{CC} - 2V$ .

## AC Electrical Characteristics

**Table 5A. AC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency		19.44		25	MHz
$f_{jit(cc)}$	Cycle-to-Cycle Jitter; NOTE 1			18	30	ps
$f_{jit(\emptyset)}$	RMS Phase Jitter (Random); NOTE 2, 3	Integration Range: 12kHz – 5MHz		0.66	0.83	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	100		500	ps
odc	Output Duty Cycle		49		51	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 2: Refer to the Phase Noise plots.

NOTE 3: Characterized using Rhode Schwartz SMA100A for input clocks.

**Table 5B. AC Characteristics,  $V_{CC} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency		19.44		25	MHz
$f_{jit(cc)}$	Cycle-to-Cycle Jitter; NOTE 1			18	30	ps
$f_{jit(\emptyset)}$	RMS Phase Jitter (Random); NOTE 2, 3	Integration Range: 12kHz – 5MHz		0.66	0.83	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	100		500	ps
odc	Output Duty Cycle		49		51	%

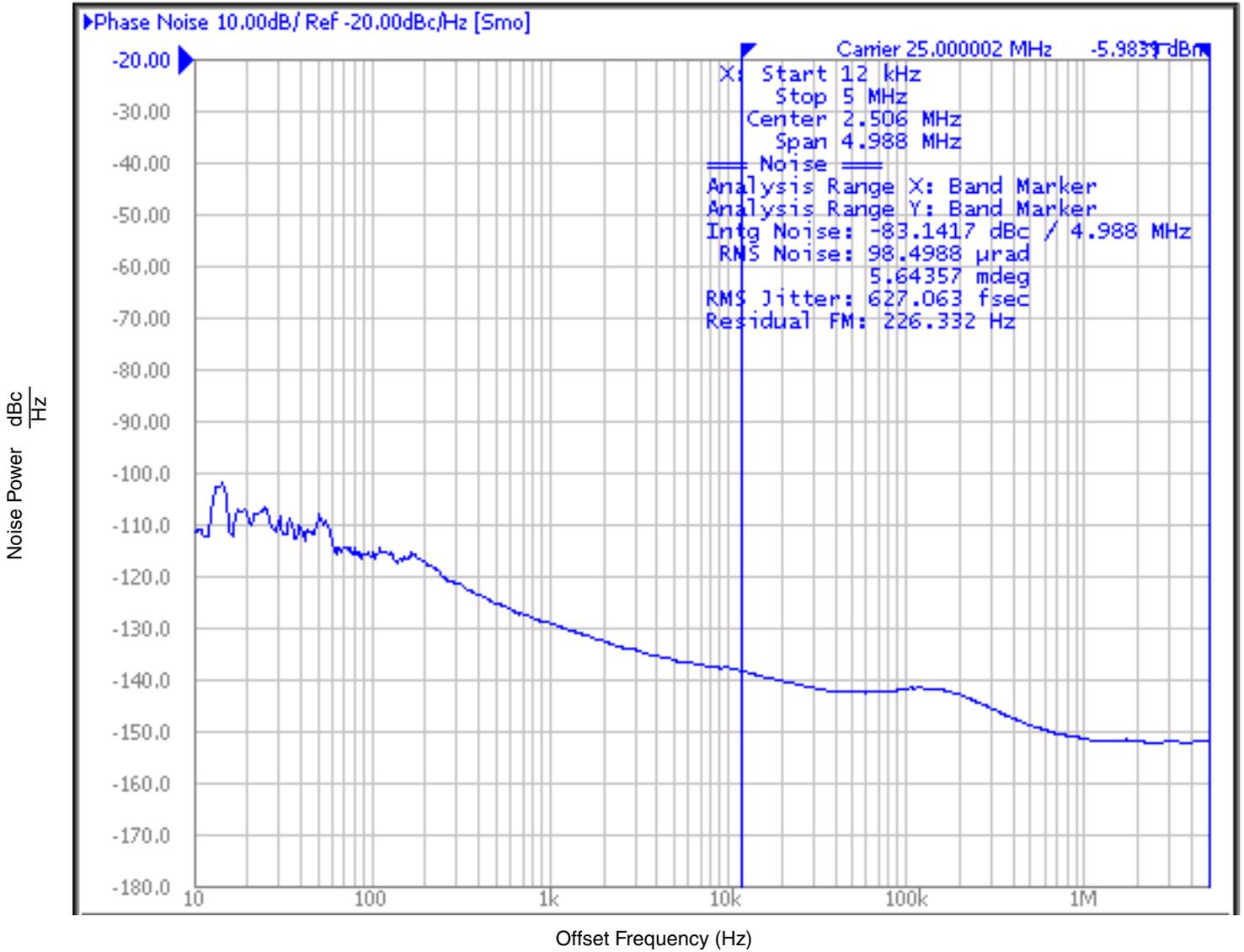
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

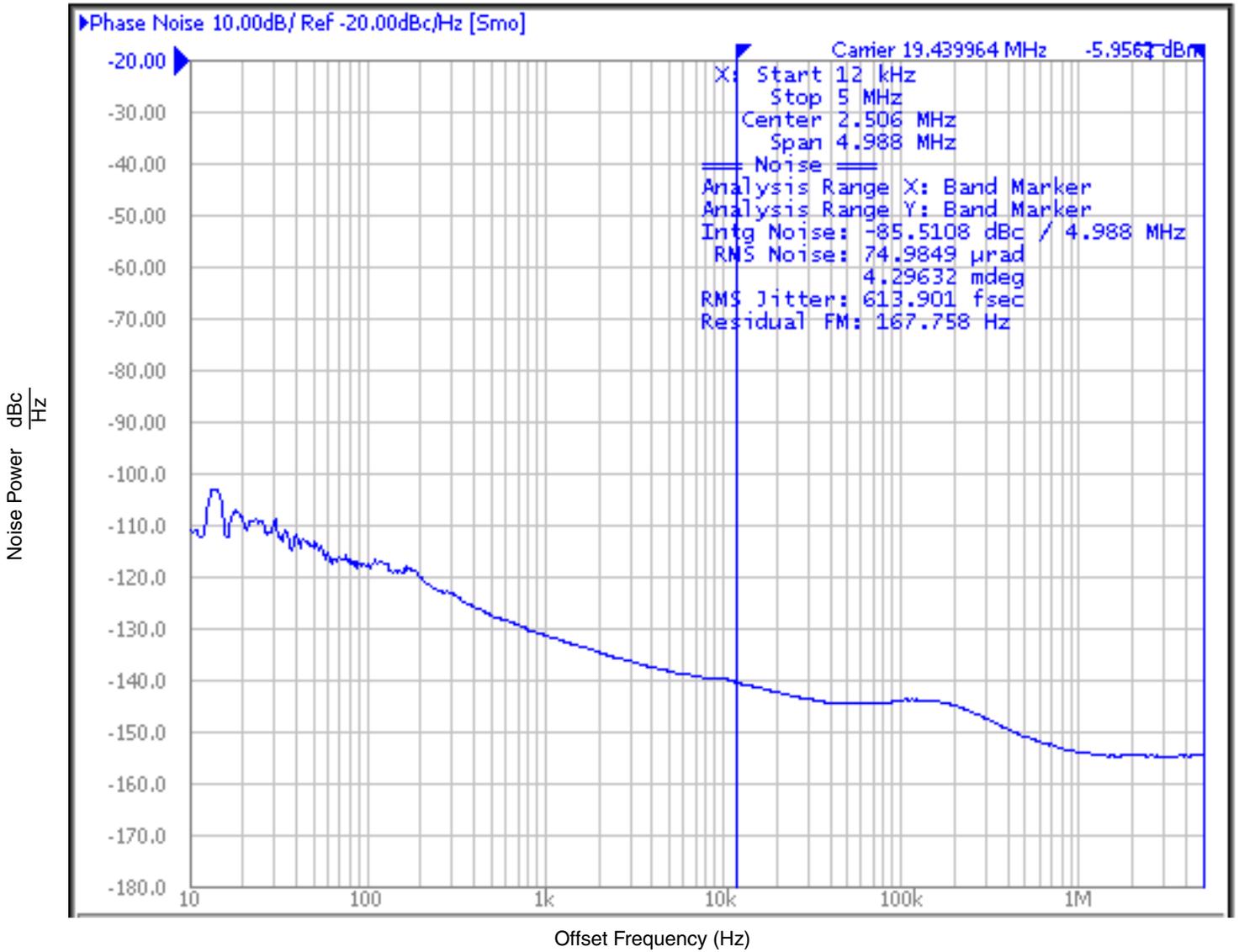
NOTE 2: Refer to the Phase Noise plots.

NOTE 3: Characterized using Rhode Schwartz SMA100A for input clocks.

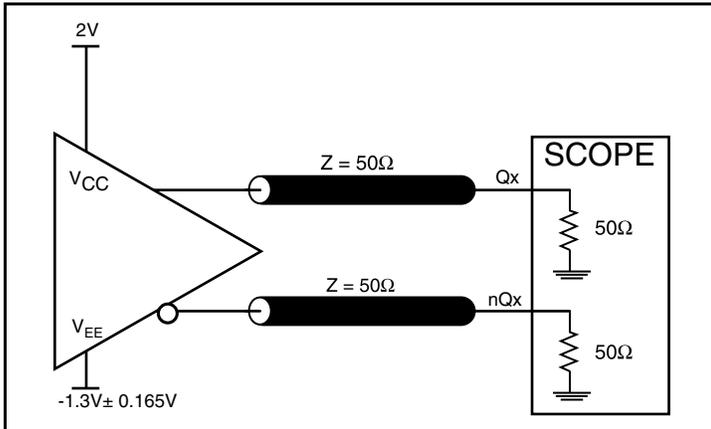
Typical Phase Noise at 25MHz



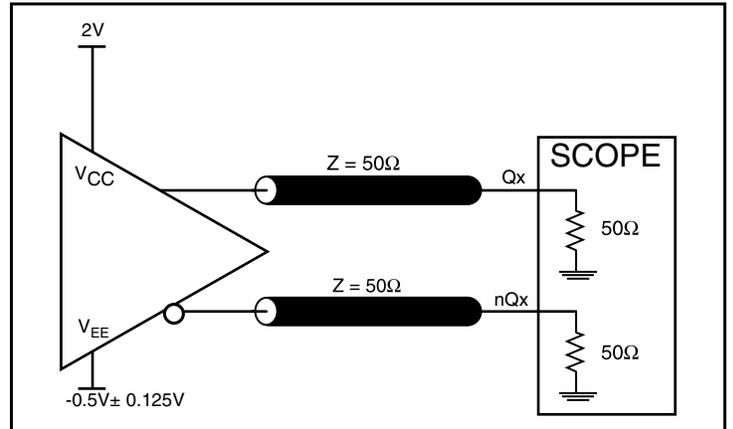
Typical Phase Noise at 19.44MHz



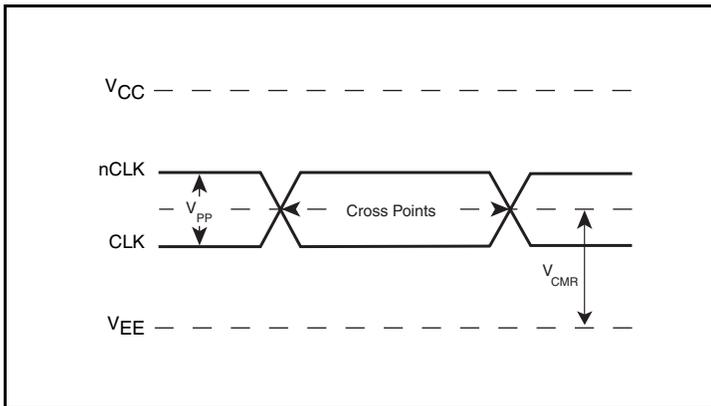
## Parameter Measurement Information



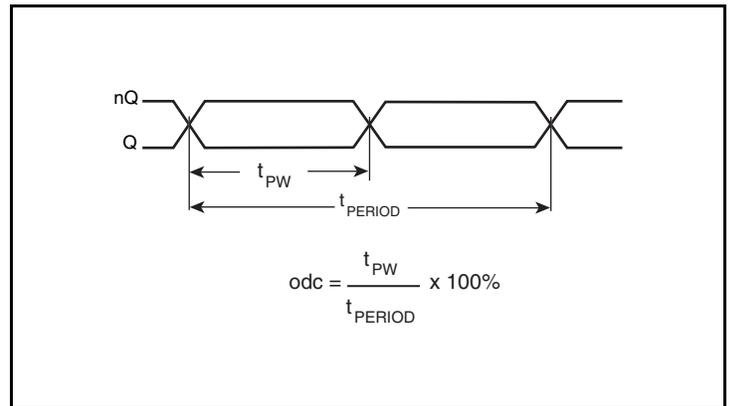
3.3V LVPECL Output Load AC Test Circuit



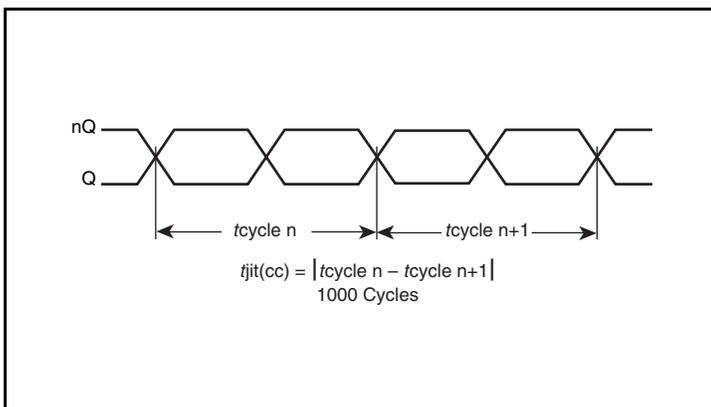
2.5V LVPECL Output Load AC Test Circuit



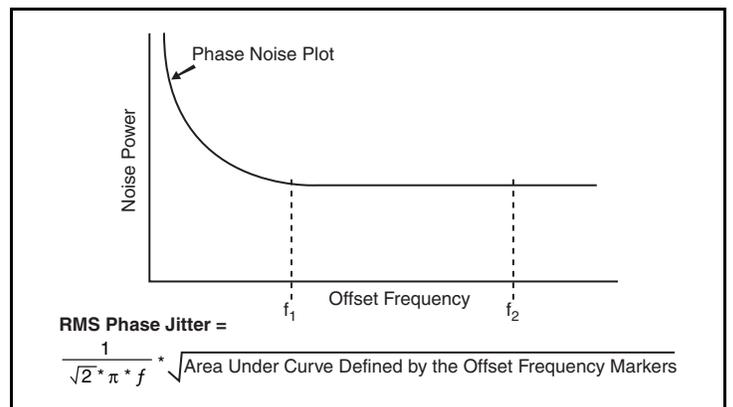
Differential Input Level



Output Duty Cycle/Pulse Width/Period

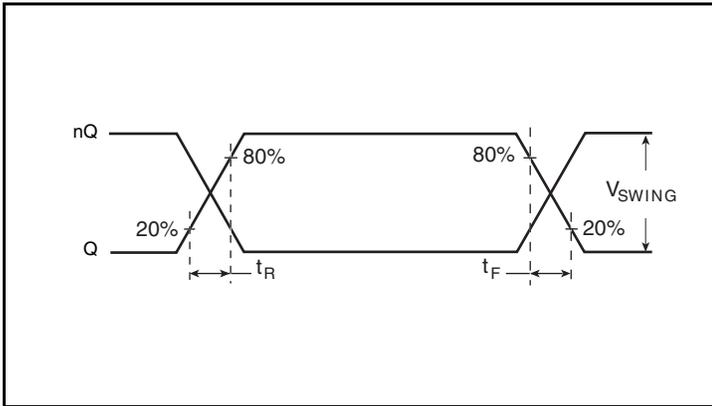


Cycle-to-Cycle Jitter



RMS Phase Jitter

## Parameter Measurement Information, continued



Output Rise/Fall Time

## Application Information

### Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{CC}/2$  is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is 2.5V and  $V_{CC} = 3.3V$ , R1 and R2 value should be adjusted to set  $V_{REF}$  at 1.25V. The values below are for when both the single ended swing and  $V_{CC}$  are at the same voltage. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission

line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however  $V_{IL}$  cannot be less than -0.3V and  $V_{IH}$  cannot be more than  $V_{CC} + 0.3V$ . Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

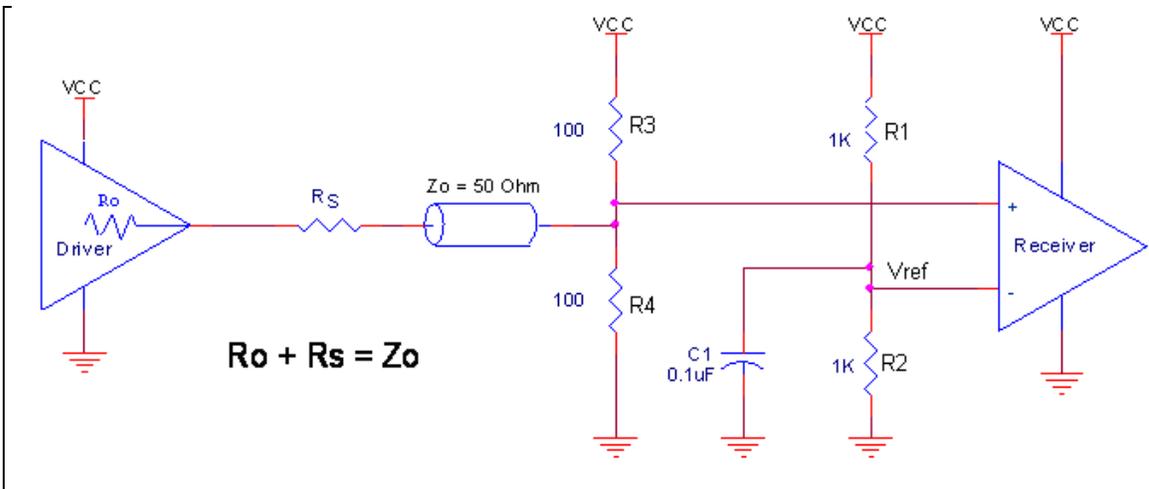
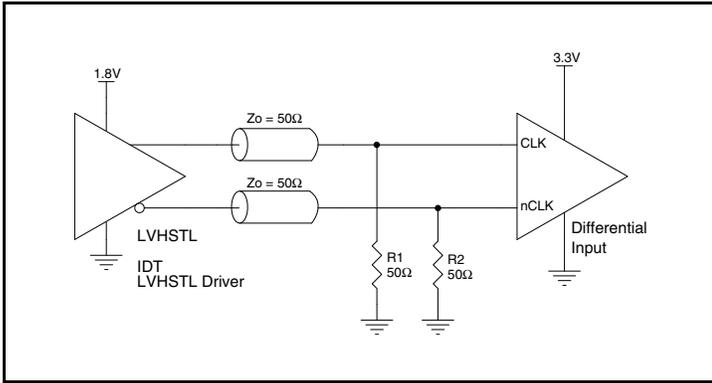


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

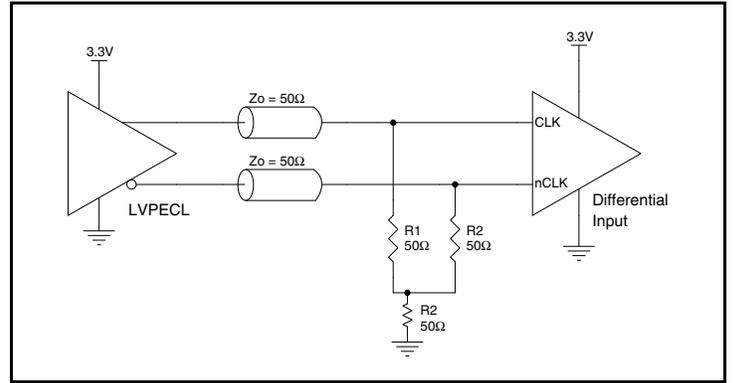
## Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. *Figures 2A to 2F* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the

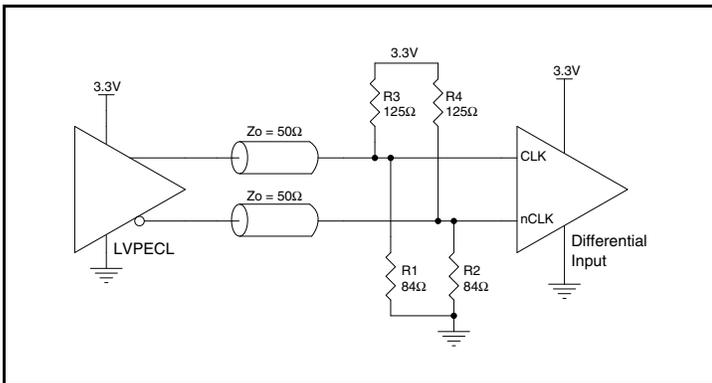
vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



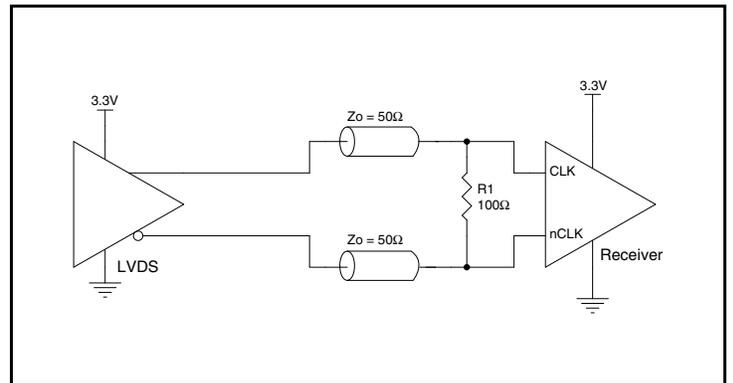
**Figure 2A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver**



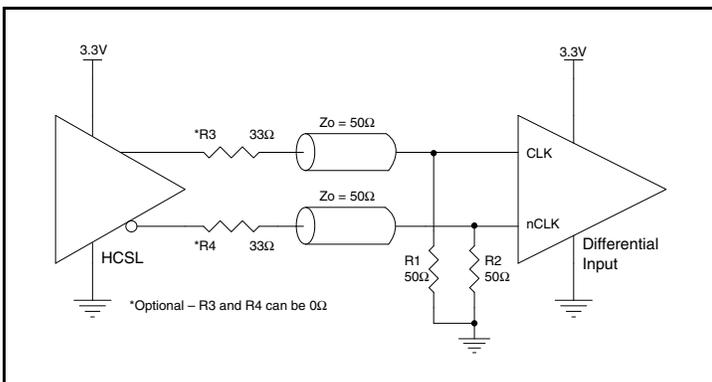
**Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



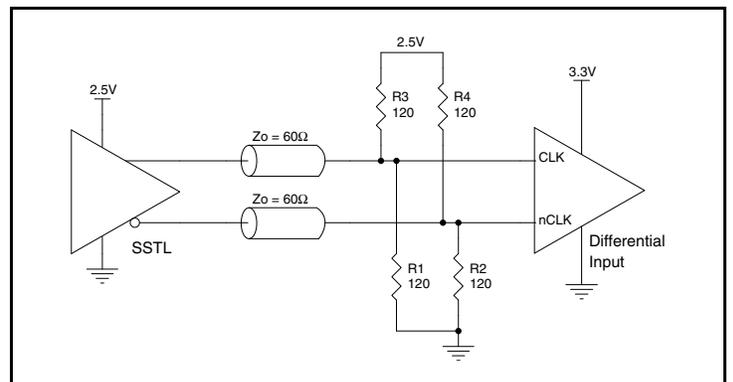
**Figure 2C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



**Figure 2D. CLK/nCLK Input Driven by a 3.3V LVDS Driver**



**Figure 2E. CLK/nCLK Input Driven by a 3.3V HCSL Driver**



**Figure 2F. CLK/nCLK Input Driven by an SSTL Driver**

## Recommendations for Unused Input Pins

### Inputs:

#### LVC MOS Control Pins

For the control pins that have internal pullups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

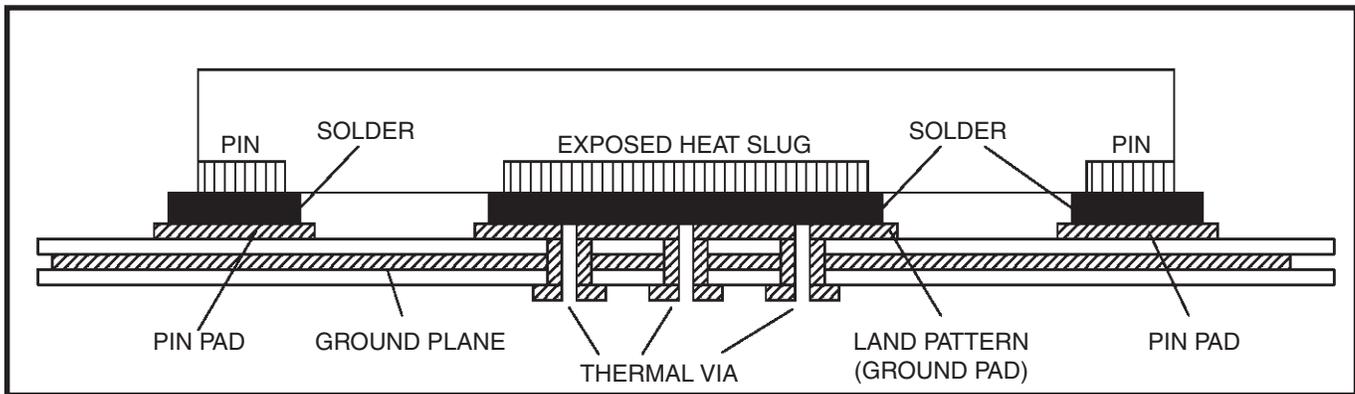


Figure 3. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

## Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible signals. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion.

Figures 4A and 4B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

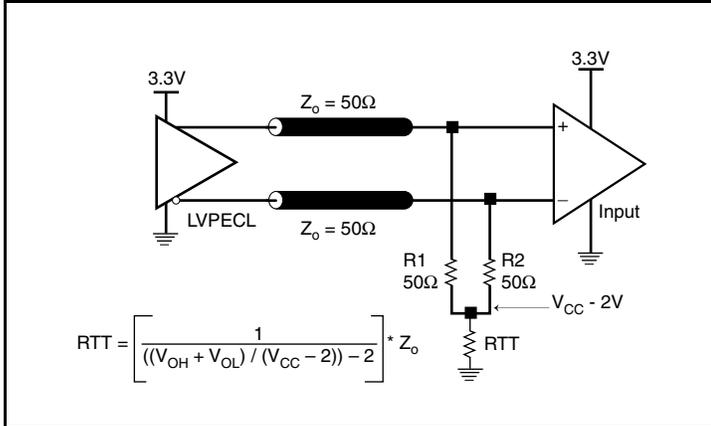


Figure 4A. 3.3V LVPECL Output Termination

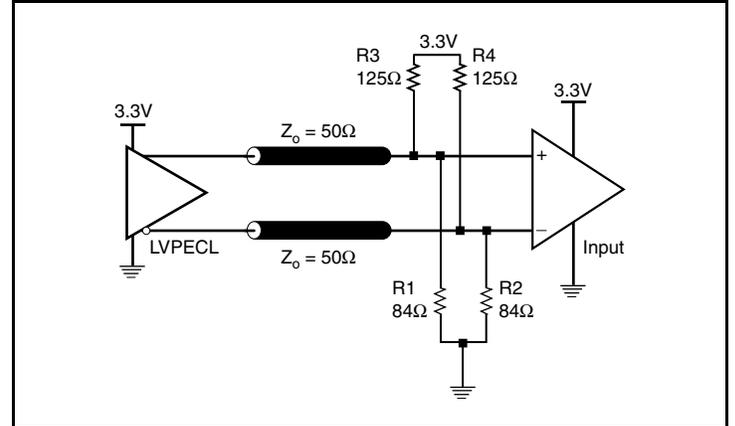


Figure 4B. 3.3V LVPECL Output Termination

## Termination for 2.5V LVPECL Outputs

Figure 5A and Figure 5B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating  $50\Omega$  to  $V_{CC} - 2V$ . For  $V_{CC} = 2.5V$ , the  $V_{CC} - 2V$  is very close to ground

level. The R3 in Figure 5B can be eliminated and the termination is shown in Figure 5C.

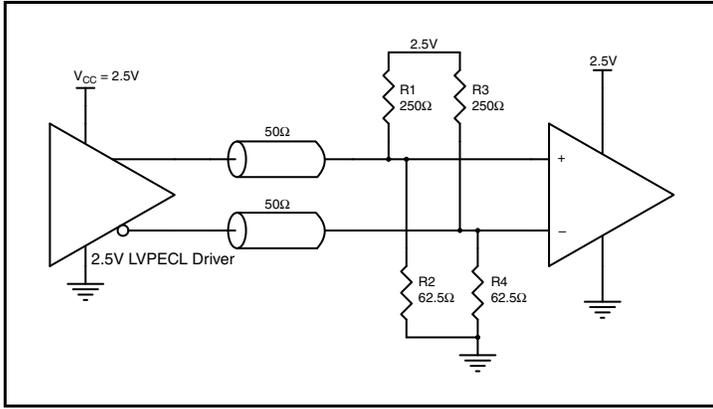


Figure 5A. 2.5V LVPECL Driver Termination Example

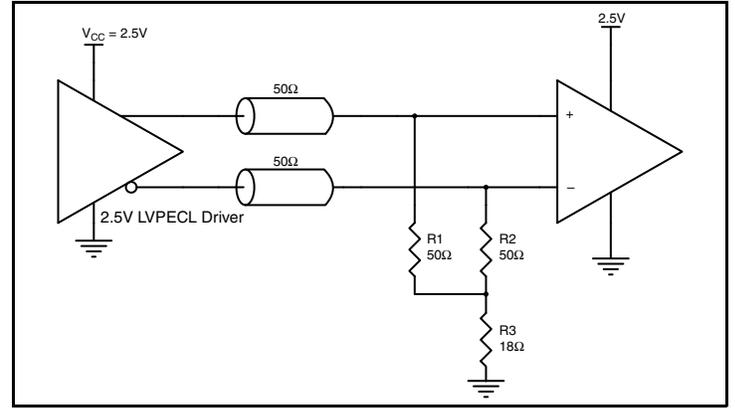


Figure 5B. 2.5V LVPECL Driver Termination Example

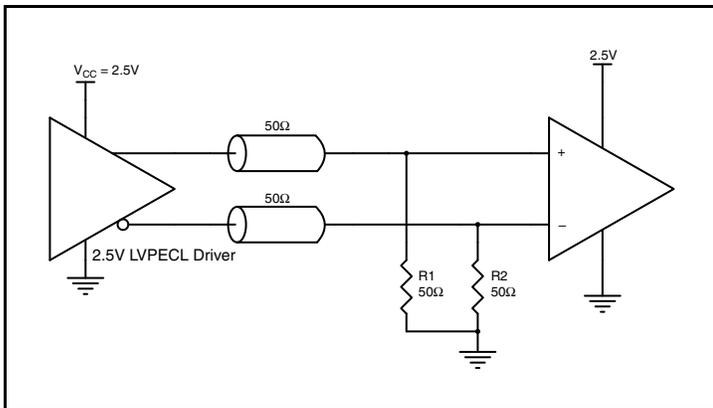


Figure 5C. 2.5V LVPECL Driver Termination Example

## Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8N3PGDAMBKI-025. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS8N3PGDAMBKI-025 is the sum of the core power plus the power dissipation in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 189mA = \mathbf{654.885mW}$
- Power (outputs)<sub>MAX</sub> = **30mW/Loaded Output pair**

**Total Power**<sub>MAX</sub> (3.3V, with all outputs switching) = 654.885mW + 30mW = **684.885mW**

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 39.2°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.685\text{W} * 39.2^\circ\text{C/W} = 111.9^\circ\text{C}. \text{ This is well below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

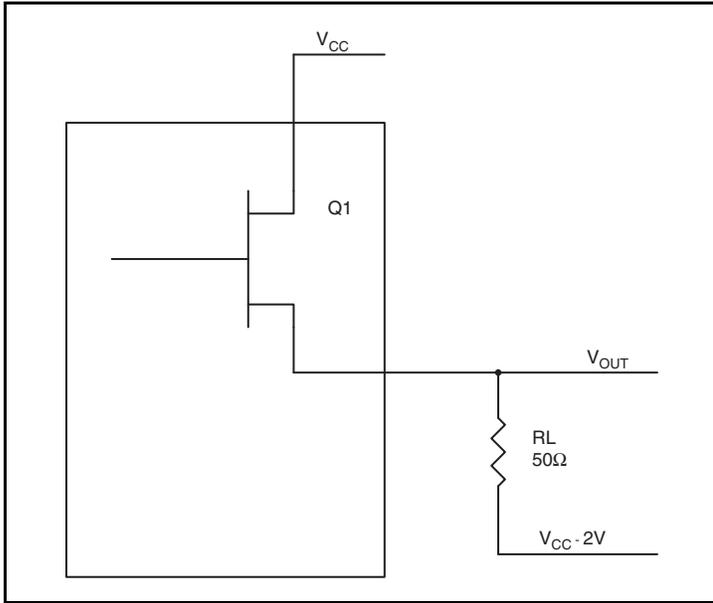
**Table 6. Thermal Resistance  $\theta_{JA}$  for 10 Lead VFQFN, Forced Convection**

$\theta_{JA}$ by Velocity	
Meters per Second	0
Multi-Layer PCB, JEDEC Standard Test Boards	39.2°C/W

### 3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

The LVPECL output driver circuit and termination are shown in *Figure 6*.



**Figure 6. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CC} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} - 0.9V$   
 $(V_{CC\_MAX} - V_{OH\_MAX}) = 0.9V$
- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} - 1.7V$   
 $(V_{CC\_MAX} - V_{OL\_MAX}) = 1.7V$

$Pd\_H$  is power dissipation when the output drives high.

$Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = \mathbf{30mW}$$

## Reliability Information

**Table 7.  $\theta_{JA}$  vs. Air Flow Table for a 10 Lead VFQFN**

$\theta_{JA}$ vs. Air Flow	
Meters per Second	<b>0</b>
Multi-Layer PCB, JEDEC Standard Test Boards	39.2°C/W

## Transistor Count

The transistor count for ICS8N3PGDAMBKI-025 is: 42,520

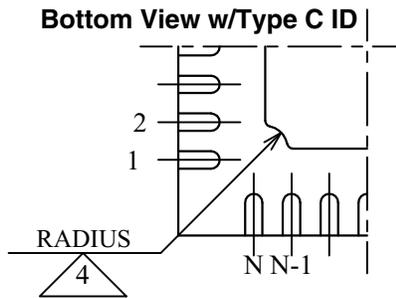
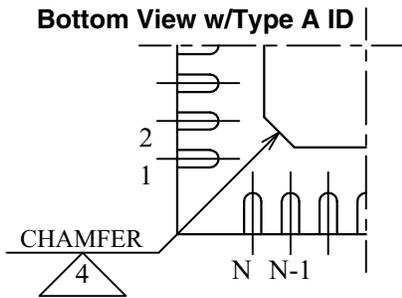
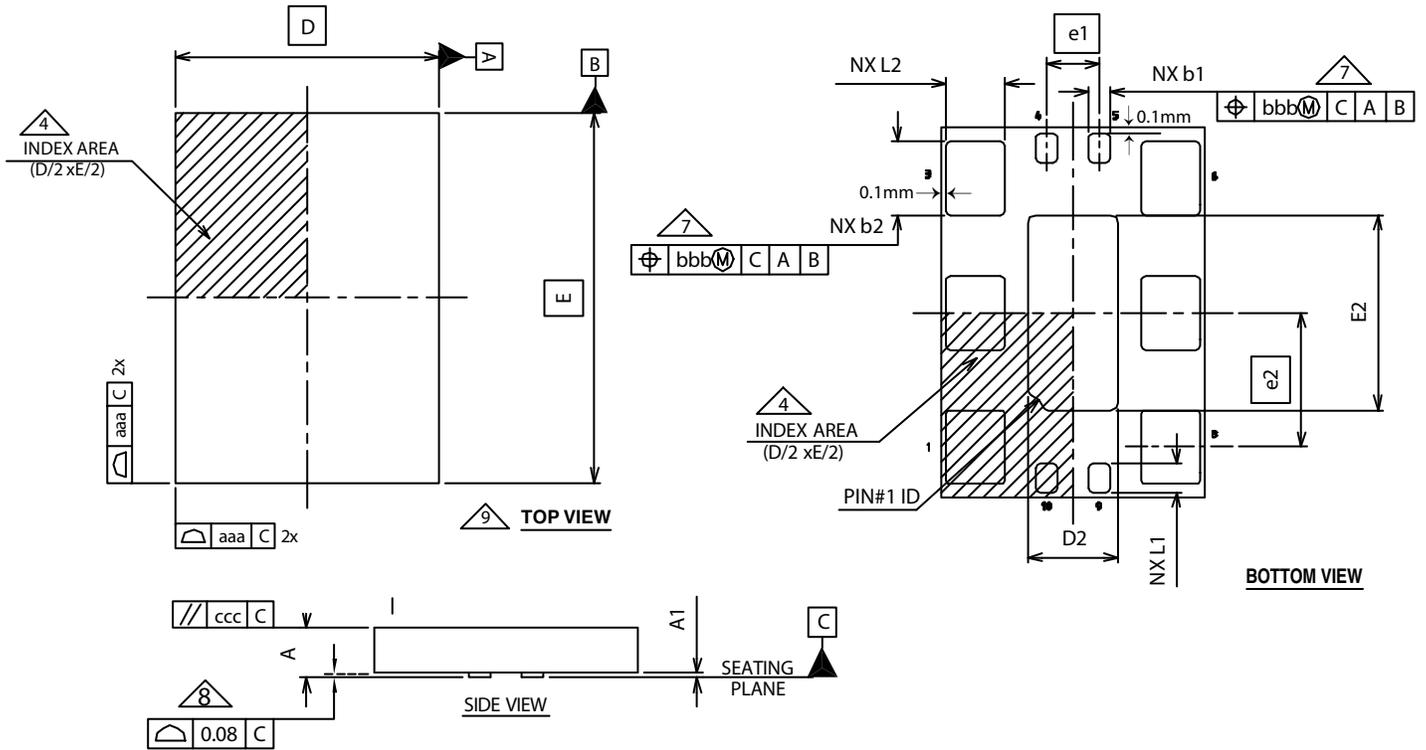
## Package Dimensions

**Table 8. Package Dimensions for 10-Lead VFQFN**

VNJR-1			
All Dimensions in Millimeters			
Symbol	Minimum	Nominal	Maximum
<b>N</b>	10		
<b>A</b>	0.80	0.90	1.00
<b>A1</b>	0	0.02	0.05
<b>b1</b>	0.35	0.40	0.45
<b>b2</b>	1.35	1.40	1.45
<b>D</b>	5.00 Basic		
<b>D2</b>	1.55	1.70	1.80
<b>E</b>	7.00 Basic		
<b>E2</b>	3.55	3.70	3.80
<b>e1</b>	1.0		
<b>e2</b>	2.54		
<b>L1</b>	0.45	0.55	0.65
<b>L2</b>	1.0	1.10	1.20
<b>N</b>	10		
<b>N<sub>D</sub></b>	2		
<b>N<sub>E</sub></b>	3		
<b>aaa</b>	0.15		
<b>bbb</b>	0.10		
<b>ccc</b>	0.10		

# Package Outline

## Package Outline - K Suffix for 10-Lead VFQFN



There are 2 methods of indicating pin 1 corner at the back of the VFQFN package are:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this

device. The pin count and pinout are shown on the front page. The package dimensions are in Table 8.

## Ordering Information

**Table 9. Ordering Information**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8N3PGDAMBKI-025LF	ICSDAMBI025L	"Lead-Free" 10 Lead VFQFN	Tray	-40°C to 85°C
8N3PGDAMBKI-025LFT	ICSDAMBI025L	"Lead-Free" 10 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

## Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T3	1	Frequency Select Table, corrected default to 19.44MHz output frequency.	5/4/10
		2	Table 3 Divider Function Table, corrected default in FSEL column to = 11 from 00.	
B	AMR	3	Per Errata NEN-11-03; Absolute Maximum Rating, changed $V_{CC}$ from 4.6V to 3.63V	10/11/12



## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).