

Device Overview

The 89HPES48T12G2 is a member of the IDT PRECISE™ family of PCI Express® switching solutions. The PES48T12G2 is a 48-lane, 12-port system interconnect switch optimized for PCI Express Gen2 packet switching in high-performance applications, supporting multiple simultaneous peer-to-peer traffic flows. Target applications include servers, storage, communications, embedded systems, and multi-host or intelligent I/O based systems with inter-domain communication.

Features

◆ High Performance Non-Blocking Switch Architecture

- 48-lane 12-port PCIe switch
 - Six x8 ports switch ports each of which can bifurcate to two x4 ports (total of twelve x4 ports)
- Integrated SerDes supports 5.0 GT/s Gen2 and 2.5 GT/s Gen1 operation
- Delivers up to 48 GBps (384 Gbps) of switching capacity
- Supports 128 Bytes to 2 KB maximum payload size
- Low latency cut-through architecture
- Supports one virtual channel and eight traffic classes

◆ Standards and Compatibility

- PCI Express Base Specification 2.0 compliant
- Implements the following optional PCI Express features
 - Advanced Error Reporting (AER) on all ports
 - End-to-End CRC (ECRC)
 - Access Control Services (ACS)
 - Power Budgeting Enhanced Capability
 - Device Serial Number Enhanced Capability
 - Sub-System ID and Sub-System Vendor ID Capability
 - Internal Error Reporting ECN
 - Multicast ECN
 - VGA and ISA enable
 - L0s and L1 ASPM
 - ARI ECN

◆ Port Configurability

- x4 and x8 ports
 - Ability to merge adjacent x4 ports to create a x8 port
- Automatic per port link width negotiation (x8 → x4 → x2 → x1)
- Crosslink support
- Automatic lane reversal
- Autonomous and software managed link width and speed control
- Per lane SerDes configuration

- De-emphasis
- Receive equalization
- Drive strength

◆ Initialization / Configuration

- Supports Root (BIOS, OS, or driver), Serial EEPROM, or SMBus switch initialization
- Common switch configurations are supported with pin strapping (no external components)
- Supports in-system Serial EEPROM initialization/programming

◆ Quality of Service (QoS)

- Port arbitration
 - Round robin
 - Weighted Round Robin (WRR)
- Request metering
 - IDT proprietary feature that balances bandwidth among switch ports for maximum system throughput
- High performance switch core architecture
 - Combined Input Output Queued (CIOQ) switch architecture with large buffers

◆ Multicast

- Compliant to the PCI-SIG multicast ECN
- Supports arbitrary multicasting of Posted transactions
- Supports 64 multicast groups
- Multicast overlay mechanism support
- ECRC regeneration support

◆ Clocking

- Supports 100 MHz and 125 MHz reference clock frequencies
- Flexible clocking modes
 - Common clock
 - Non-common clock

◆ Hot-Plug and Hot Swap

- Hot-plug controller on all ports
 - Hot-plug supported on all downstream switch ports
- All ports support hot-plug using low-cost external I²C I/O expanders
- Configurable presence detect supports card and cable applications
- GPE output pin for hot-plug event notification
 - Enables SCI/SMI generation for legacy operating system support
- Hot swap capable I/O

◆ Power Management

- Supports D0, D3hot and D3 power management states

- Active State Power Management (ASPM)
 - Supports L0, L0s, L1, L2/L3 Ready and L3 link states
 - Configurable L0s and L1 entry timers allow performance/power-savings tuning
- Supports PCI Express Power Budgeting Capability
- SerDes power savings
 - Supports low swing / half-swing SerDes operation
 - SerDes optionally turned-off in D3hot
 - SerDes associated with unused ports are turned-off
 - SerDes associated with unused lanes are placed in a low power state

◆ 9 General Purpose I/O

◆ Reliability, Availability and Serviceability (RAS)

- ECRC support
- AER on all ports
- SECDED ECC protection on all internal RAMs
- End-to-end data path parity protection
- Checksum Serial EEPROM content protected
- Autonomous link reliability (preserves system operation in the presence of faulty links)
- Ability to generate an interrupt (INTx or MSI) on link up/down transitions

◆ Test and Debug

- On-chip link activity and status outputs available for Port 0 (upstream port)
- Per port link activity and status outputs available using external I²C I/O expander for all other ports
- SerDes test modes
- Supports IEEE 1149.6 AC JTAG and IEEE 1149.1 JTAG

◆ Power Supplies

- Requires only two power supply voltages (1.0 V and 2.5 V)
Note that a 3.3V is preferred for V_{DD}I/O
- No power sequencing requirements

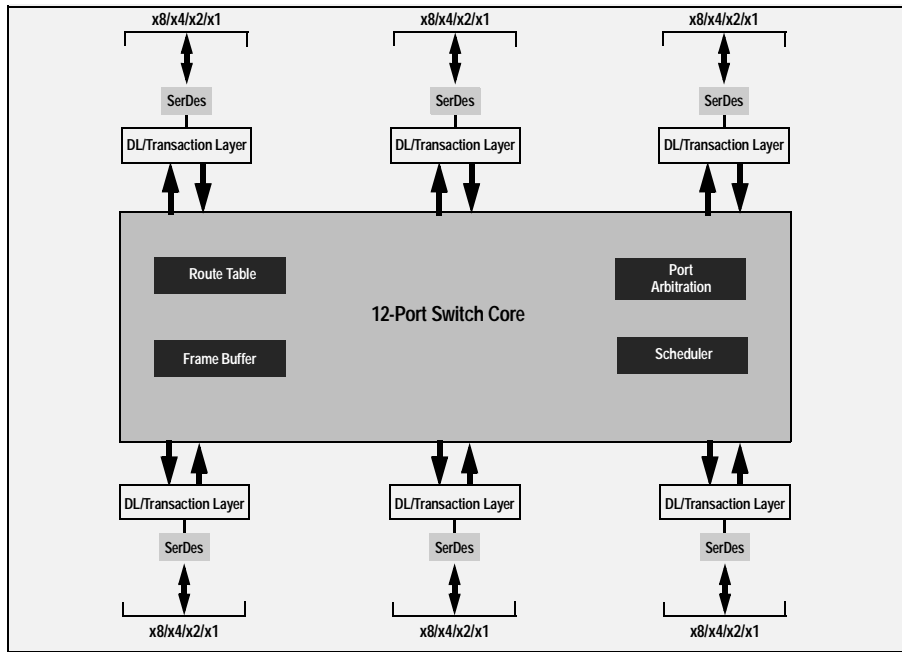
◆ Packaged in a 27mm x 27mm 676-ball Flip Chip BGA with 1mm ball spacing

Product Description

Utilizing standard PCI Express interconnect, the PES48T12G2 provides the most efficient fan-out solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. It provides 48 GBps (384 Gbps) of aggregated, full-duplex switching capacity through 48 integrated serial lanes, using proven and robust IDT technology. Each lane provides 5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base Specification, Revision 2.0.

The PES48T12G2 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 2.0. The PES48T12G2 can operate either as a store and forward or cut-through switch. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to enable efficient switching and I/O connectivity for servers, storage, and embedded processors with limited connectivity.

Block Diagram



48 PCI Express Lanes
Up to 6 x8 ports or 12 x4 Ports

Figure 1 Internal Block Diagram

SMBus Interface

The PES48T12G2 contains an SMBus master interface. This master interface allows the default configuration register values of the PES48T12G2 to be overridden following a reset with values programmed in an external serial EEPROM. The master interface is also used by an external Hot-Plug I/O expander. Two pins make up the SMBus master interface: an SMBus clock pin and an SMBus data pin. Four pins make up the SMBus slave interface: an SMBus clock pin and an SMBus data pin plus two address pins, SSMBADDR[2,1].

As shown in Figure 2, the master and slave SMBuses may only be used in a split configuration.

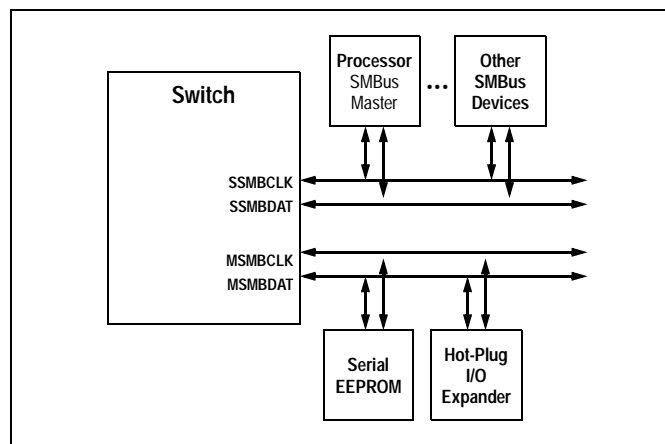


Figure 2 Split SMBus Interface Configuration

The switch's SMBus master interface does not support SMBus arbitration. As a result, the switch's SMBus master must be the only master in the SMBus lines that connect to the serial EEPROM and I/O expander slaves. In the split configuration, the master and slave SMBuses operate as two independent buses; thus, multi-master arbitration is not required.

Hot-Plug Interface

The PES48T12G2 supports PCI Express Hot-Plug on each downstream port. To reduce the number of pins required on the device, the PES48T12G2 utilizes an external I/O expander, such as that used on PC motherboards, connected to the SMBus master interface. Following reset and configuration, whenever the state of a Hot-Plug output needs to be modified, the PES48T12G2 generates an SMBus transaction to the I/O expander with the new value of all of the outputs. Whenever a Hot-Plug input changes, the I/O expander generates an interrupt which is received on the IOEXPINTN input pin (alternate function of GPIO) of the PES48T12G2. In response to an I/O expander interrupt, the PES48T12G2 generates an SMBus transaction to read the state of all of the Hot-Plug inputs from the I/O expander.

General Purpose Input/Output

The PES48T12G2 provides 9 General Purpose Input/Output (GPIO) pins that may be used by the system designer as bit I/O ports. Each GPIO pin may be configured independently as an input or output through software control. Some GPIO pins are shared with other on-chip functions. These alternate functions may be enabled via software, SMBus slave interface, or serial configuration EEPROM.

Pin Description

The following tables list the functions of the pins provided on the PES48T12G2. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an "N" are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Signal	Type	Name/Description
PE00RP[3:0] PE00RN[3:0]	I	PCI Express Port 0 Serial Data Receive. Differential PCI Express receive pairs for port 0.
PE00TP[3:0] PE00TN[3:0]	O	PCI Express Port 0 Serial Data Transmit. Differential PCI Express transmit pairs for port 0.
PE01RP[3:0] PE01RN[3:0]	I	PCI Express Port 1 Serial Data Receive. Differential PCI Express receive pairs for port 1. When port 0 is merged with port 1, these signals become port 0 receive pairs for lanes 4 through 7.
PE01TP[3:0] PE01TN[3:0]	O	PCI Express Port 1 Serial Data Transmit. Differential PCI Express transmit pairs for port 1. When port 0 is merged with port 1, these signals become port 0 transmit pairs for lanes 4 through 7.
PE02RP[3:0] PE02RN[3:0]	I	PCI Express Port 2 Serial Data Receive. Differential PCI Express receive pairs for port 2.
PE02TP[3:0] PE02TN[3:0]	O	PCI Express Port 2 Serial Data Transmit. Differential PCI Express transmit pairs for port 2.
PE03RP[3:0] PE03RN[3:0]	I	PCI Express Port 3 Serial Data Receive. Differential PCI Express receive pairs for port 3. When port 2 is merged with port 3, these signals become port 2 receive pairs for lanes 4 through 7.
PE03TP[3:0] PE03TN[3:0]	O	PCI Express Port 3 Serial Data Transmit. Differential PCI Express transmit pairs for port 3. When port 2 is merged with port 3, these signals become port 2 transmit pairs for lanes 4 through 7.
PE04RP[3:0] PE04RN[3:0]	I	PCI Express Port 4 Serial Data Receive. Differential PCI Express receive pairs for port 4.
PE04TP[3:0] PE04TN[3:0]	O	PCI Express Port 4 Serial Data Transmit. Differential PCI Express transmit pairs for port 4.
PE05RP[3:0] PE05RN[3:0]	I	PCI Express Port 5 Serial Data Receive. Differential PCI Express receive pairs for port 5. When port 4 is merged with port 5, these signals become port 4 receive pairs for lanes 4 through 7.

Table 1 PCI Express Interface Pins (Part 1 of 2)

Signal	Type	Name/Description
PE05TP[3:0] PE05TN[3:0]	O	PCI Express Port 5 Serial Data Transmit. Differential PCI Express transmit pairs for port 5. When port 4 is merged with port 5, these signals become port 4 transmit pairs for lanes 4 through 7.
PE06RP[3:0] PE06RN[3:0]	I	PCI Express Port 6 Serial Data Receive. Differential PCI Express receive pairs for port 6.
PE06TP[3:0] PE06TN[3:0]	O	PCI Express Port 6 Serial Data Transmit. Differential PCI Express transmit pairs for port 6.
PE07RP[3:0] PE07RN[3:0]	I	PCI Express Port 7 Serial Data Receive. Differential PCI Express receive pairs for port 7. When port 6 is merged with port 7, these signals become port 6 receive pairs for lanes 4 through 7.
PE07TP[3:0] PE07TN[3:0]	O	PCI Express Port 7 Serial Data Transmit. Differential PCI Express transmit pairs for port 7. When port 6 is merged with port 7, these signals become port 6 transmit pairs for lanes 4 through 7.
PE08RP[3:0] PE08RN[3:0]	I	PCI Express Port 8 Serial Data Receive. Differential PCI Express receive pairs for port 8.
PE08TP[3:0] PE08TN[3:0]	O	PCI Express Port 8 Serial Data Transmit. Differential PCI Express transmit pairs for port 8.
PE09RP[3:0] PE09RN[3:0]	I	PCI Express Port 9 Serial Data Receive. Differential PCI Express receive pairs for port 9. When port 8 is merged with port 9, these signals become port 8 receive pairs for lanes 4 through 7.
PE09TP[3:0] PE09TN[3:0]	O	PCI Express Port 9 Serial Data Transmit. Differential PCI Express transmit pairs for port 9. When port 8 is merged with port 9, these signals become port 8 transmit pairs for lanes 4 through 7.
PE12RP[3:0] PE12RN[3:0]	I	PCI Express Port 12 Serial Data Receive. Differential PCI Express receive pairs for port 12.
PE12TP[3:0] PE12TN[3:0]	O	PCI Express Port 12 Serial Data Transmit. Differential PCI Express transmit pairs for port 12.
PE13RP[3:0] PE13RN[3:0]	I	PCI Express Port 13 Serial Data Receive. Differential PCI Express receive pairs for port 13. When port 12 is merged with port 13, these signals become port 12 receive pairs for lanes 4 through 7.
PE13TP[3:0] PE13TN[3:0]	O	PCI Express Port 13 Serial Data Transmit. Differential PCI Express transmit pairs for port 13. When port 12 is merged with port 13, these signals become port 12 transmit pairs for lanes 4 through 7.

Table 1 PCI Express Interface Pins (Part 2 of 2)

Signal	Type	Name/Description
GCLKN[1:0] GCLKP[1:0]	I	Global Reference Clock. Differential reference clock input pair. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic. The frequency of the differential reference clock is determined by the GCLKFSEL signal.

Table 2 Reference Clock Pins

Signal	Type	Name/Description
MSMBCLK	I/O	Master SMBus Clock. This bidirectional signal is used to synchronize transfers on the master SMBus.
MSMBDAT	I/O	Master SMBus Data. This bidirectional signal is used for data on the master SMBus.
SSMBADDR[2,1]	I	Slave SMBus Address. These pins determine the SMBus address to which the slave SMBus interface responds.
SSMBCLK	I/O	Slave SMBus Clock. This bidirectional signal is used to synchronize transfers on the slave SMBus.
SSMBDAT	I/O	Slave SMBus Data. This bidirectional signal is used for data on the slave SMBus.

Table 3 SMBus Interface Pins

Signal	Type	Name/Description
GPIO[0]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART0PERSTN Alternate function pin type: Input/Output Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[1]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART1PERSTN Alternate function pin type: Input/Output Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[2]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART2PERSTN Alternate function pin type: Input/Output Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[3]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART3PERSTN Alternate function pin type: Input/Output Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[4]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function — Reserved 2nd Alternate function pin name: POLINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 0 Link Up Status output.

Table 4 General Purpose I/O Pins (Part 1 of 2)

Signal	Type	Name/Description
GPIO[5]	0	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: GPEN 1st Alternate function pin type: Output 1st Alternate function: Hot-plug general purpose even output. 2nd Alternate function pin name: P0ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 0 Link Active Status Output.
GPIO[6]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[7]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[8]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN Alternate function pin type: Input Alternate function: IO expander interrupt.

Table 4 General Purpose I/O Pins (Part 2 of 2)

Signal	Type	Name/Description
CLKMODE[1:0]		Clock Mode. These signals determine the port clocking mode used by ports of the device.
GCLKFSEL	I	Global Clock Frequency Select. These signals select the frequency of the GCLKP and GCLKN signals. 0x0 100 MHz 0x1 125 MHz
P01MERGEN	I	Port 0 and 1 Merge. P01MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 0 is merged with port 1 to form a single x8 port. The Serdes lanes associated with port 1 become lanes 4 through 7 of port 0. When this pin is high, port 0 and port 1 are not merged, and each operates as a single x4 port.
P23MERGEN	I	Port 2 and 3 Merge. P23MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 2 is merged with port 3 to form a single x8 port. The Serdes lanes associated with port 3 become lanes 4 through 7 of port 2. When this pin is high, port 2 and port 3 are not merged, and each operates as a single x4 port.
P45MERGEN	I	Port 4 and 5 Merge. P45MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 4 is merged with port 5 to form a single x8 port. The Serdes lanes associated with port 5 become lanes 4 through 7 of port 4. When this pin is high, port 4 and port 5 are not merged, and each operates as a single x4 port.
P67MERGEN	I	Port 6 and 7 Merge. P67MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 6 is merged with port 7 to form a single x8 port. The Serdes lanes associated with port 7 become lanes 4 through 7 of port 6. When this pin is high, port 6 and port 7 are not merged, and each operates as a single x4 port.

Table 5 System Pins (Part 1 of 2)

Signal	Type	Name/Description
P89MERGEN	I	Port 8 and 9 Merge. P89MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 8 is merged with port 9 to form a single x8 port. The Serdes lanes associated with port 9 become lanes 4 through 7 of port 8. When this pin is high, port 8 and port 9 are not merged, and each operates as a single x4 port.
P1213MERGEN	I	Port 12 and 13 Merge. P1213MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 12 is merged with port 13 to form a single x8 port. The Serdes lanes associated with port 13 become lanes 4 through 7 of port 12. When this pin is high, port 12 and port 13 are not merged, and each operates as a single x4 port.
PERSTN	I	Global Reset. Assertion of this signal resets all logic inside PES48T12G2.
RSTHALT	I	Reset Halt. When this signal is asserted during a PCI Express fundamental reset, PES48T12G2 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the SWCTL register by an SMBus master.
SWMODE[3:0]	I	Switch Mode. These configuration pins determine the PES48T12G2 switch operating mode. Note: These pins should be static and not change following the negation of PERSTN. 0x0 - Normal switch mode 0x1 - Normal switch mode with Serial EEPROM initialization 0x2 through 0x7 - Reserved 0x8 - Single partition with port 0 selected as the upstream port (port 2 disabled) 0x9 - Single partition with port 2 selected as the upstream port (port 0 disabled) 0xA - Single partition with Serial EEPROM initialization and port 0 selected as the upstream port (port 2 disabled) 0xB - Single partition with Serial EEPROM initialization and port 2 selected as the upstream port (port 0 disabled) 0xE - Reserved 0xF - Reserved

Table 5 System Pins (Part 2 of 2)

Signal	Type	Name/Description
JTAG_TCK	I	JTAG Clock. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	JTAG Data Input. This is the serial data input to the boundary scan logic or JTAG Controller.

Table 6 Test Pins (Part 1 of 2)

Signal	Type	Name/Description
JTAG_TDO	O	JTAG Data Output. This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	JTAG Mode. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.
JTAG_TRST_N	I	JTAG Reset. This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: <ul style="list-style-type: none"> 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 6 Test Pins (Part 2 of 2)

Signal	Type	Name/Description
REFRES[13,12,9:0]	I/O	External Reference Resistors. Provides a reference for the SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from these pins to ground.
REFRESPLL	I/O	PLL External Reference Resistor. Provides a reference for the PLL bias currents and PLL calibration circuitry. A 3K Ohm +/- 1% resistor should be connected from this pin to ground.
V _{DD} CORE	I	Core V_{DD}. Power supply for core logic (1.0V).
V _{DD} I/O	I	I/O V_{DD}. LVTTTL I/O buffer power supply (2.5V or preferred 3.3V).
V _{DD} PEA	I	PCI Express Analog Power. Serdes analog power supply (1.0V).
V _{DD} PEHA	I	PCI Express Analog High Power. Serdes analog power supply (2.5V).
V _{DD} PETA	I	PCI Express Transmitter Analog Voltage. Serdes transmitter analog power supply (1.0V).
V _{SS}	I	Ground.

Table 7 Power, Ground, and SerDes Resistor Pins

Pin Characteristics

Note: Some input pads of the switch do not contain internal pull-ups or pull-downs. Unused SMBus and System inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any of these pins left floating can cause a slight increase in power consumption. Finally, unused Serdes (Rx and Tx) pins should be left floating.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor ¹	Notes
PCI Express Interface	PE00RN[3:0]	I	PCIe Differential ²	Serial Link		
	PE00RP[3:0]	I				
	PE00TN[3:0]	O				
	PE00TP[3:0]	O				
	PE01RN[3:0]	I				
	PE01RP[3:0]	I				
	PE01TN[3:0]	O				
	PE01TP[3:0]	O				
	PE02RN[3:0]	I				
	PE02RP[3:0]	I				
	PE02TN[3:0]	O				
	PE02TP[3:0]	O				
	PE03RN[3:0]	I				
	PE03RP[3:0]	I				
	PE03TN[3:0]	O				
	PE03TP[3:0]	O				
	PE04RN[3:0]	I				
	PE04RP[3:0]	I				
	PE04TN[3:0]	O				
	PE04TP[3:0]	O				
	PE05RN[3:0]	I				
	PE05RP[3:0]	I				
	PE05TN[3:0]	O				
	PE05TP[3:0]	O				
	PE06RN[3:0]	I				
	PE06RP[3:0]	I				
	PE06TN[3:0]	O				
	PE06TP[3:0]	O				
	PE07RN[3:0]	I				
	PE07RP[3:0]	I				
	PE07TN[3:0]	O				
	PE07TP[3:0]	O				
PE08RN[3:0]	I					
PE08RP[3:0]	I					
PE08TN[3:0]	O					

Table 8 Pin Characteristics (Part 1 of 3)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor ¹	Notes
PCI Express Interface (Cont.)	PE08TP[3:0]	O	PCIe Differential	Serial Link		
	PE09RN[3:0]	I				
	PE09RP[3:0]	I				
	PE09TN[3:0]	O				
	PE09TP[3:0]	O				
	PE12RN[3:0]	I				
	PE12RP[3:0]	I				
	PE12TN[3:0]	O				
	PE12TP[3:0]	O				
	PE13RN[3:0]	I				
	PE13RP[3:0]	I				
	PE13TN[3:0]	O				
	PE13TP[3:0]	O				
	GCLKN[1:0]	I	HCSL	Diff. Clock Input		Refer to Table 9
GCLKP[1:0]	I					
SMBus	MSMBCLK	I/O	LVTTTL	STI ³		pull-up on board
	MSMBDAT	I/O		STI		pull-up on board
	SSMBADDR[2:1]	I		Input	pull-up	
	SSMBCLK	I/O		STI		pull-up on board
	SSMBDAT	I/O		STI		pull-up on board
General Purpose I/O	GPIO[8:0]	I/O	LVTTTL	STI, High Drive	pull-up	
System Pins	CLKMODE[1:0]	I	LVTTTL	Input	pull-up	
	GCLKFSEL	I			pull-down	
	P01MERGEN	I			pull-down	
	P23MERGEN	I			pull-down	
	P45MERGEN	I			pull-down	
	P67MERGEN	I			pull-down	
	P89MERGEN	I			pull-down	
	P1213MERGEN	I			pull-down	
	PERSTN	I		STI		
	RSTHALT	I		Input	pull-down	
	SWMODE[3:0]	I			pull-down	
EJTAG / JTAG	JTAG_TCK	I	LVTTTL	STI	pull-up	
	JTAG_TDI	I		STI	pull-up	
	JTAG_TDO	O				
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I		STI	pull-up	

Table 8 Pin Characteristics (Part 2 of 3)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor ¹	Notes
SerDes Reference Resistors	REFRES00	I/O	Analog			
	REFRES01	I/O				
	REFRES02	I/O				
	REFRES03	I/O				
	REFRES04	I/O				
	REFRES05	I/O				
	REFRES06	I/O				
	REFRES07	I/O				
	REFRES08	I/O				
	REFRES09	I/O				
	REFRES12	I/O				
	REFRES13	I/O				
	REFRESPLL	I/O				

Table 8 Pin Characteristics (Part 3 of 3)

- ¹. Internal resistor values under typical operating conditions are 92K Ω for pull-up and 91K Ω for pull-down.
- ². All receiver pins set the DC common mode voltage to ground. All transmitters must be AC coupled to the media.
- ³. Schmitt Trigger Input (STI).

Logic Diagram — PES48T12G2

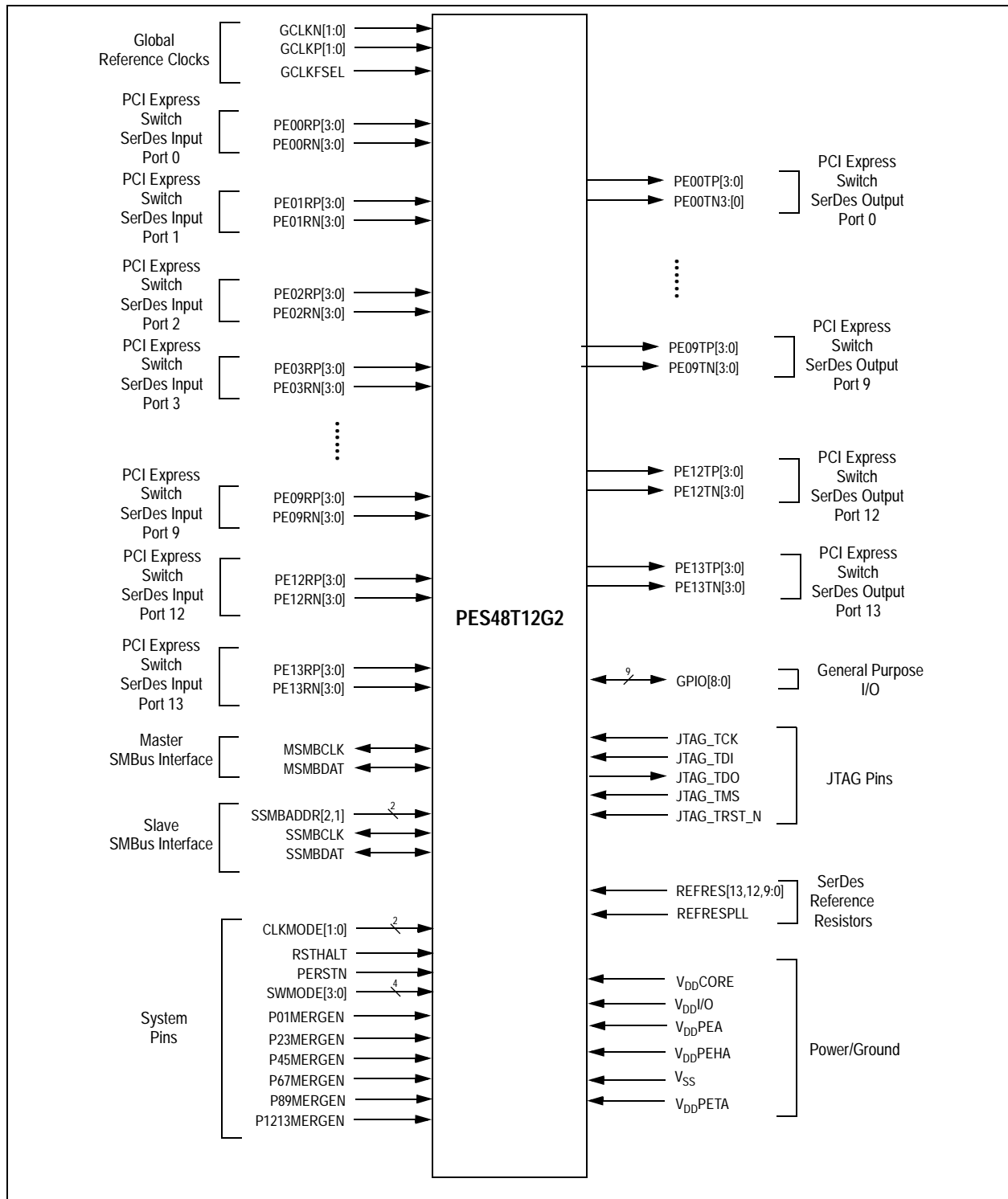


Figure 3 PES48T12G2 Logic Diagram

System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 13 and 14.

Parameter	Description	Condition	Min	Typical	Max	Unit
Refclk _{FREQ}	Input reference clock frequency range		100		125 ¹	MHz
T _{C-RISE}	Rising edge rate	Differential	0.6		4	V/ns
T _{C-FALL}	Falling edge rate	Differential	0.6		4	V/ns
V _{IH}	Differential input high voltage	Differential	+150			mV
V _{IL}	Differential input low voltage	Differential			-150	mV
V _{CROSS}	Absolute single-ended crossing point voltage	Single-ended	+250		+550	mV
V _{CROSS-DELTA}	Variation of V _{CROSS} over all rising clock edges	Single-ended			+140	mV
V _{RB}	Ring back voltage margin	Differential	-100		+100	mV
T _{STABLE}	Time before V _{RB} is allowed	Differential	500			ps
T _{PERIOD-AVG}	Average clock period accuracy		-300		2800	ppm
T _{PERIOD-ABS}	Absolute period, including spread-spectrum and jitter		9.847		10.203	ns
T _{CC-JITTER}	Cycle to cycle jitter				150	ps
V _{MAX}	Absolute maximum input voltage				+1.15	V
V _{MIN}	Absolute minimum input voltage		-0.3			V
Duty Cycle	Duty cycle		40		60	%
Rise/Fall Matching	Single ended rising Refclk edge rate versus falling Refclk edge rate			20		%
Z _{C-DC}	Clock source output DC impedance		40		60	Ω

Table 9 Input Clock Requirements

¹ The input clock frequency will be either 100 or 125 MHz depending on signal GCLKFSEL.

AC Timing Characteristics

Parameter	Description	Gen 1			Gen 2			Units
		Min ¹	Typ ¹	Max ¹	Min ¹	Typ ¹	Max ¹	
PCIe Transmit								
UI	Unit Interval	399.88	400	400.12	199.94	200	200.06	ps
T _{TX-EYE}	Minimum Tx Eye Width	0.75			0.75			UI
T _{TX-EYE-MEDIAN-to-MAX-JITTER}	Maximum time between the jitter median and maximum deviation from the median			0.125				UI
T _{TX-RISE} , T _{TX-FALL}	TX Rise/Fall Time: 20% - 80%	0.125			0.15			UI
T _{TX-IDLE-MIN}	Minimum time in idle	20			20			UI

Table 10 PCIe AC Timing Characteristics (Part 1 of 2)

Parameter	Description	Gen 1			Gen 2			Units
		Min ¹	Typ ¹	Max ¹	Min ¹	Typ ¹	Max ¹	
T _{TX-IDLE-SET-TO-IDLE}	Maximum time to transition to a valid Idle after sending an Idle ordered set			8			8	ns
T _{TX-IDLE-TO-DIFF-DATA}	Maximum time to transition from valid idle to diff data			8			8	ns
T _{TX-SKEW}	Transmitter data skew between any 2 lanes			1.3			1.3	ns
T _{MIN-PULSED}	Minimum Instantaneous Lone Pulse Width	NA			0.9			UI
T _{TX-HF-DJ-DD}	Transmitter Deterministic Jitter > 1.5MHz Bandwidth	NA					0.15	UI
T _{RF-MISMATCH}	Rise/Fall Time Differential Mismatch	NA					0.1	UI
PCIe Receive								
UI	Unit Interval	399.88	400	400.12	199.94		200.06	ps
T _{RX-EYE (with jitter)}	Minimum Receiver Eye Width (jitter tolerance)	0.4			0.4			UI
T _{RX-EYE-MEDIUM TO MAX JITTER}	Max time between jitter median & max deviation			0.3				UI
T _{RX-SKEW}	Lane to lane input skew			20			8	ns
T _{RX-HF-RMS}	1.5 — 100 MHz RMS jitter (common clock)	NA					3.4	ps
T _{RX-HF-DJ-DD}	Maximum tolerable DJ by the receiver (common clock)	NA					88	ps
T _{RX-LF-RMS}	10 KHz to 1.5 MHz RMS jitter (common clock)	NA					4.2	ps
T _{RX-MIN-PULSE}	Minimum receiver instantaneous eye width	NA			0.6			UI

Table 10 PCIe AC Timing Characteristics (Part 2 of 2)

¹ Minimum, Typical, and Maximum values meet the requirements under PCI Specification 2.0

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
GPIO						
GPIO[8:0] ¹	T _{pw} ²	None	50	—	ns	

Table 11 GPIO AC Timing Characteristics

¹ GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.

² The values for this symbol were determined by calculation, not by testing.

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
JTAG						
JTAG_TCK	Tper_16a	none	50.0	—	ns	See Figure 4.
	Thigh_16a, Tlow_16a		10.0	25.0	ns	
JTAG_TMS ¹ , JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	ns	
	Thld_16b		1.0	—	ns	
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	20	ns	
	Tdz_16c ²		—	20	ns	
JTAG_TRST_N	Tpw_16d ²	none	25.0	—	ns	

Table 12 JTAG AC Timing Characteristics

¹ The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

² The values for this symbol were determined by calculation, not by testing.

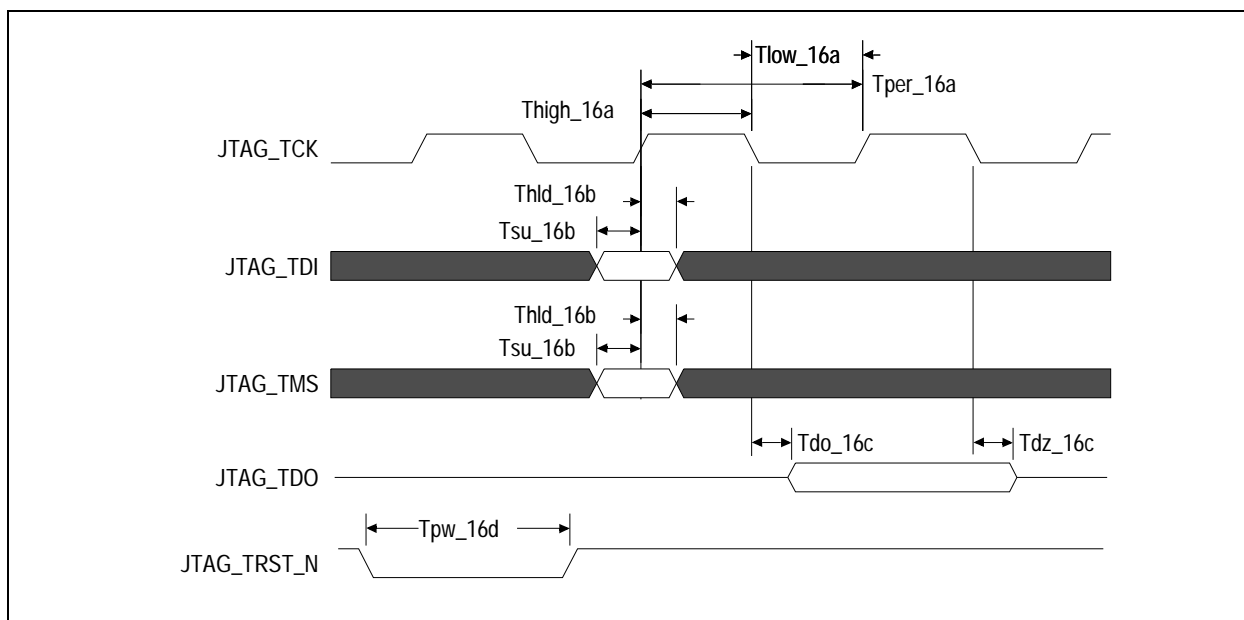


Figure 4 JTAG AC Timing Waveform

Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DDCORE}	Internal logic supply	0.9	1.0	1.1	V
$V_{DDI/O}$	I/O supply except for SerDes	2.25	2.5	2.75	V
		3.125	3.3	3.465	V
V_{DDPEA}^1	PCI Express Analog Power	0.95	1.0	1.1	V
V_{DDPEHA}^2	PCI Express Analog High Power	2.25	2.5	2.75	V
V_{DDPETA}^1	PCI Express Transmitter Analog Voltage	0.95	1.0	1.1	V
V_{SS}	Common ground	0	0	0	V

Table 13 PES48T12G2 Operating Voltages

¹ V_{DDPEA} and V_{DDPETA} should have no more than 25mV_{peak-peak} AC power supply noise superimposed on the 1.0V nominal DC value.

² V_{DDPEHA} should have no more than 50mV_{peak-peak} AC power supply noise superimposed on the 2.5V nominal DC value.

Power-Up/Power-Down Sequence

During power supply ramp-up, V_{DDCORE} must remain at least 1.0V below $V_{DDI/O}$ at all times. There are no other power-up sequence requirements for the various operating supply voltages.

The power-down sequence can occur in any order.

Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient
Industrial	-40°C to +85°C Ambient

Table 14 PES48T12G2 Operating Temperatures

Power Consumption

Typical power is measured under the following conditions: 25°C Ambient, 35% total link usage on all ports, typical voltages defined in Table 13 (and also listed below).

Maximum power is measured under the following conditions: 70°C Ambient, 85% total link usage on all ports, maximum voltages defined in Table 13 (and also listed below).

Number of Active Lanes per Port		Core Supply		PCIe Analog Supply		PCIe Analog High Supply		PCIe Transmitter Supply		I/O Supply		Total	
		Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 2.5V	Max 2.75V	Typ 1.0V	Max 1.1V	Typ 2.5V	Max 2.75V	Typ Power	Max Power
8/8/8/8/8/8 (Full Swing)	mA	3200	5336	2313	2705	816	825	845	898	24	29		
	Watts	3.20	5.87	2.31	2.98	2.04	2.27	0.85	0.99	0.06	0.08	8.46	12.18
8/8/8/8/8/8 (Half Swing)	mA	3200	5336	1989	2327	816	825	439	467	24	29		
	Watts	3.20	5.87	1.99	2.56	2.04	2.27	0.44	0.51	0.06	0.08	7.73	11.29

Table 15 PES48T12G2 Power Consumption — 2.5V I/O

Number of Active Lanes per Port		Core Supply		PCIe Analog Supply		PCIe Analog High Supply		PCIe Transmitter Supply		I/O Supply		Total	
		Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 2.5V	Max 2.75V	Typ 1.0V	Max 1.1V	Typ 3.3V	Max 3.465V	Typ Power	Max Power
8/8/8/8/8/8 (Full Swing)	mA	3200	5336	2313	2705	816	825	845	898	30	35		
	Watts	3.20	5.87	2.31	2.98	2.04	2.27	0.85	0.99	0.10	0.12	8.50	12.22
8/8/8/8/8/8 (Half Swing)	mA	3200	5336	1989	2327	816	825	439	467	30	35		
	Watts	3.20	5.87	1.99	2.56	2.04	2.27	0.44	0.51	0.10	0.12	7.77	11.33

Table 16 PES48T12G2 Power Consumption — 3.3V I/O

Note 1: I/O supply of 3.3V is preferred.

Note 2: The above power consumption assumes that all ports are functioning at Gen2 (5.0 GT/S) speeds. Power consumption can be reduced by turning off unused ports through software or through boot EEPROM. Power savings will occur in V_{DDPEA} , V_{DDPEHA} , and V_{DDPETA} . Power savings can be estimated as directly proportional to the number of unused ports, since the power consumption of a turned-off port is close to zero. For example, if 2 ports out of 12 are turned off, then the power savings for each of the above three power rails can be calculated quite simply as 2/12 multiplied by the power consumption indicated in the above table.

Note 3: Using a port in Gen1 mode (2.5GT/S) results in approximately 18% power savings for each power rail: V_{DDPEA} , V_{DDPEHA} , and V_{DDPETA} .

Thermal Considerations

This section describes thermal considerations for the PES48T12G2 (27mm² FCBGA676 package). The data in Table 17 below contains information that is relevant to the thermal performance of the PES48T12G2 switch.

Symbol	Parameter	Value	Units	Conditions
$T_{J(max)}$	Junction Temperature	125	°C	Maximum
$T_{A(max)}$	Ambient Temperature	70	°C	Maximum for commercial-rated products
		85	°C	Maximum for industrial-rated products
$\theta_{JA(effective)}$	Effective Thermal Resistance, Junction-to-Ambient	14.6	°C/W	Zero air flow
		7.8	°C/W	1 m/S air flow
		6.4	°C/W	2 m/S air flow
θ_{JB}	Thermal Resistance, Junction-to-Board	2.7	°C/W	
θ_{JC}	Thermal Resistance, Junction-to-Case	0.15	°C/W	
P	Power Dissipation of the Device	12.22	Watts	Maximum

Table 17 Thermal Specifications for PES48T12G2, 27x27 mm FCBGA676 Package

Note: It is important for the reliability of this device in any user environment that the junction temperature not exceed the $T_{J(max)}$ value specified in Table 17. Consequently, the effective junction to ambient thermal resistance (θ_{JA}) for the worst case scenario must be maintained below the value determined by the formula:

$$\theta_{JA} = (T_{J(max)} - T_{A(max)})/P$$

Given that the values of $T_{J(max)}$, $T_{A(max)}$, and P are known, the value of desired θ_{JA} becomes a known entity to the system designer. How to achieve the desired θ_{JA} is left up to the board or system designer, but in general, it can be achieved by adding the effects of θ_{JC} (value provided in Table 17), thermal resistance of the chosen adhesive (θ_{CS}), that of the heat sink (θ_{SA}), amount of airflow, and properties of the circuit board (number of layers and size of the board). It is strongly recommended that users perform their own thermal analysis for their own board and system design scenarios.

DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 13.

Note: See Table 8, Pin Characteristics, for a complete I/O listing.

I/O Type	Parameter	Description	Gen1			Gen2			Unit	Condi- tions
			Min ¹	Typ ¹	Max ¹	Min ¹	Typ ¹	Max ¹		
Serial Link	PCIe Transmit									
	V _{TX-DIFFp-p}	Differential peak-to-peak output voltage	800		1200	800		1200	mV	
	V _{TX-DIFFp-p-LOW}	Low-Drive Differential Peak to Peak Output Voltage	400		1200	400		1200	mV	
	V _{TX-DE-RATIO-3.5dB}	De-emphasized differential output voltage	-3		-4	-3.0	-3.5	-4.0	dB	
	V _{TX-DE-RATIO-6.0dB}	De-emphasized differential output voltage	NA			-5.5	-6.0	-6.5	dB	
	V _{TX-DC-CM}	DC Common mode voltage	0		3.6	0		3.6	V	
	V _{TX-CM-ACP}	RMS AC peak common mode output voltage			20				mV	
	V _{TX-CM-DC-active-idle-delta}	Abs delta of DC common mode voltage between LO and idle			100			100	mV	
	V _{TX-CM-DC-line-delta}	Abs delta of DC common mode voltage between D+ and D-			25			25	mV	
	V _{TX-Idle-DiffP}	Electrical idle diff peak output			20			20	mV	
	RL _{TX-DIFF}	Transmitter Differential Return loss	10					10	dB	0.05 - 1.25GHz
									8	dB
	RL _{TX-CM}	Transmitter Common Mode Return loss	6					6	dB	
	Z _{TX-DIFF-DC}	DC Differential TX impedance	80	100	120			120	Ω	
	V _{TX-CM-ACpp}	Peak-Peak AC Common	NA					100	mV	
	V _{TX-DC-CM}	Transmit Driver DC Common Mode Voltage	0		3.6	0		3.6	V	
V _{TX-RCV-DETECT}	The amount of voltage change allowed during Receiver Detection			600			600	mV		
I _{TX-SHORT}	Transmitter Short Circuit Current Limit	0		90				90	mA	

Table 18 DC Electrical Characteristics (Part 1 of 2)

I/O Type	Parameter	Description	Gen1			Gen2			Unit	Conditions
			Min ¹	Typ ¹	Max ¹	Min ¹	Typ ¹	Max ¹		
Serial Link (cont.)	PCIe Receive									
	$V_{RX-DIFFp-p}$	Differential input voltage (peak-to-peak)	175		1200	120		1200	mV	
	$RL_{RX-DIFF}$	Receiver Differential Return Loss	10					10	dB	0.05 - 1.25GHz
								8		1.25 - 2.5GHz
	RL_{RX-CM}	Receiver Common Mode Return Loss	6					6	dB	
	$Z_{RX-DIFF-DC}$	Differential input impedance (DC)	80	100	120	Refer to return loss spec			Ω	
	Z_{RX--DC}	DC common mode impedance	40	50	60	40		60	Ω	
	$Z_{RX-COMM-DC}$	Powered down input common mode impedance (DC)	200k	350k				50k	Ω	
	$Z_{RX-HIGH-IMP-DC-POS}$	DC input CM input impedance for $V > 0$ during reset or power down			50k			50k	Ω	
	$Z_{RX-HIGH-IMP-DC-NEG}$	DC input CM input impedance for $V < 0$ during reset or power down			1.0k			1.0k	Ω	
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65		175	65		175	mV		
$V_{RX-CM-ACp}$	Receiver AC common-mode peak voltage			150			150	mV	$V_{RX-CM-ACp}$	
PCIe REFCLK										
	C_{IN}	Input Capacitance	1.5	—		1.5	—		pF	
Other I/Os										
LOW Drive Output	I_{OL}		—	2.5	—	—	2.5	—	mA	$V_{OL} = 0.4v$
	I_{OH}		—	-5.5	—	—	-5.5	—	mA	$V_{OH} = 1.5V$
High Drive Output	I_{OL}		—	12.0	—	—	12.0	—	mA	$V_{OL} = 0.4v$
	I_{OH}		—	-20.0	—	—	-20.0	—	mA	$V_{OH} = 1.5V$
Schmitt Trigger Input (STI)	V_{IL}		-0.3	—	0.8	-0.3	—	0.8	V	—
	V_{IH}		2.0	—	$V_{DD}/O + 0.5$	2.0	—	$V_{DD}/O + 0.5$	V	—
Input	V_{IL}		-0.3	—	0.8	-0.3	—	0.8	V	—
	V_{IH}		2.0	—	$V_{DD}/O + 0.5$	2.0	—	$V_{DD}/O + 0.5$	V	—
Capacitance	C_{IN}		—	—	8.5	—	—	8.5	pF	—
Leakage	Inputs		—	—	± 10	—	—	± 10	μA	V_{DD}/O (max)
	I/O_{LEAK} W/O Pull-ups/downs		—	—	± 10	—	—	± 10	μA	V_{DD}/O (max)
	I/O_{LEAK} WITH Pull-ups/downs		—	—	± 80	—	—	± 80	μA	V_{DD}/O (max)

Table 18 DC Electrical Characteristics (Part 2 of 2)

¹ Minimum, Typical, and Maximum values meet the requirements under PCI Specification 2.0.

Absolute Maximum Voltage Rating

Core Supply	PCIe Analog Supply	PCIe Analog High Supply	PCIe Transmitter Supply	I/O Supply
1.5V	1.5V	4.6V	1.5V	4.6V

Table 19 PES48T12G2 Absolute Maximum Voltage Rating

Warning: For proper and reliable operation in adherence with this data sheet, the device should not exceed the recommended operating voltages in Table 13. The absolute maximum operating voltages in Table 19 are offered to provide guidelines for voltage excursions outside the recommended voltage ranges. Device functionality is not guaranteed at these conditions and sustained operation at these values or any exposure to voltages outside the maximum range may adversely affect device functionality and reliability.

SMBus Characterization

Symbol	Parameter	SMBus 2.0 Char. Data ¹			Unit
		3V	3.3V	3.6V	
DC Parameter for SDA Pin					
V _{IL}	Input Low	1.16	1.26	1.35	V
V _{IH}	Input High	1.56	1.67	1.78	V
V _{OL@350uA}	Output Low	15	15	15	mV
I _{OL@0.4V}		23	24	25	mA
I _{Pullup}	Current Source	—	—	—	μA
I _{IL_Leak}	Input Low Leakage	0	0	0	μA
I _{IH_Leak}	Input High Leakage	0	0	0	μA
DC Parameter for SCL Pin					
V _{IL (V)}	Input Low	1.11	1.2	1.31	V
V _{IH (V)}	Input High	1.54	1.65	1.76	V
I _{IL_Leak}	Input Low Leakage	0	0	0	μA
I _{IH_Leak}	Input High Leakage	0	0	0	μA

Table 20 SMBus DC Characterization Data

¹ Data at room and hot temperature.

Symbol	Parameter	SMBus @3.3V $\pm 10\%$ ¹		Unit
		Min	Max	
F _{SCL}	Clock frequency	5	600	KHz
T _{BUF}	Bus free time between Stop and Start	3.5	—	μ s
T _{HD:STA}	Start condition hold time	1	—	μ s
T _{SU:STA}	Start condition setup time	1	—	μ s
T _{SU:STO}	Stop condition setup time	1	—	μ s
T _{HD:DAT}	Data hold time	1	—	ns
T _{SU:DAT}	Data setup time	1	—	ns
T _{TIMEOUT}	Detect clock low time out	—	74.7	ms
T _{LOW}	Clock low period	3.7	—	μ s
T _{HIGH}	Clock high period	3.7	—	μ s
T _F	Clock/Data fall time	—	72.2	ns
T _R	Clock/Data rise time	—	68.3	ns
T _{POR@10kHz}	Time which a device must be operational after power-on reset	20	—	ms

Table 21 SMBus AC Timing Data

¹. Data at room and hot temperature.

PES48T12G2 Package Pinout, 27x27mm 676-BGA Signal Pinout

The following table lists the pin numbers and signal names for the PES48T12G2 (27x27mm) device.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	V _{SS}		B9	PE08TN0		C17	V _{SS}		D25	V _{DD} /O	
A2	V _{SS}		B10	V _{SS}		C18	V _{SS}		D26	V _{DD} /O	
A3	V _{DD} /O		B11	PE03TN3		C19	V _{SS}		E1	V _{SS}	
A4	V _{SS}		B12	PE03TN2		C20	V _{SS}		E2	V _{SS}	
A5	PE08TP3		B13	V _{SS}		C21	V _{SS}		E3	V _{SS}	
A6	PE08TP2		B14	PE03TN1		C22	V _{SS}		E4	V _{SS}	
A7	V _{SS}		B15	PE03TN0		C23	JTAG_TDO		E5	PE08RP3	
A8	PE08TP1		B16	V _{SS}		C24	JTAG_TDI		E6	PE08RP2	
A9	PE08TP0		B17	PE02TN3		C25	SSMBCLK		E7	V _{SS}	
A10	V _{SS}		B18	PE02TN2		C26	SSMBADDR1		E8	PE08RP1	
A11	PE03TP3		B19	V _{SS}		D1	V _{DD} /O		E9	PE08RP0	
A12	PE03TP2		B20	PE02TN1		D2	V _{DD} /O		E10	V _{SS}	
A13	V _{SS}		B21	PE02TN0		D3	V _{SS}		E11	PE03RP3	
A14	PE03TP1		B22	V _{DD} /O		D4	V _{SS}		E12	PE03RP2	
A15	PE03TP0		B23	MSMBCLK		D5	PE08RN3		E13	V _{SS}	
A16	V _{SS}		B24	PERSTN		D6	PE08RN2		E14	PE03RP1	
A17	PE02TP3		B25	SSMBDAT		D7	V _{SS}		E15	PE03RP0	
A18	PE02TP2		B26	SSMBADDR2		D8	PE08RN1		E16	V _{SS}	
A19	V _{SS}		C1	V _{SS}		D9	PE08RN0		E17	PE02RP3	
A20	PE02TP1		C2	V _{SS}		D10	V _{SS}		E18	PE02RP2	
A21	PE02TP0		C3	V _{SS}		D11	PE03RN3		E19	V _{SS}	
A22	V _{DD} /O		C4	V _{SS}		D12	PE03RN2		E20	PE02RP1	
A23	MSMBDAT		C5	V _{SS}		D13	REFRES03		E21	PE02RP0	
A24	JTAG_TMS		C6	V _{SS}		D14	PE03RN1		E22	PE01RP3	
A25	CLKMODE1		C7	V _{SS}		D15	PE03RN0		E23	PE01RN3	
A26	JTAG_TCK		C8	V _{SS}		D16	V _{SS}		E24	V _{SS}	
B1	V _{SS}		C9	V _{SS}		D17	PE02RN3		E25	PE01TN3	
B2	V _{SS}		C10	V _{SS}		D18	PE02RN2		E26	PE01TP3	
B3	V _{DD} /O		C11	V _{SS}		D19	V _{SS}		F1	PE09TP0	
B4	V _{SS}		C12	V _{SS}		D20	PE02RN1		F2	PE09TN0	
B5	PE08TN3		C13	V _{SS}		D21	PE02RN0		F3	V _{SS}	
B6	PE08TN2		C14	V _{SS}		D22	JTAG_TRST_N		F4	PE09RN0	
B7	V _{SS}		C15	V _{SS}		D23	V _{SS}		F5	PE09RP0	
B8	PE08TN1		C16	V _{SS}		D24	V _{SS}		F6	V _{SS}	

Table 22 PES48T12G2 Signal Pin-Out (Part 1 of 5)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
F7	V _{SS}		G18	V _{DD} PETA		J3	V _{SS}		K14	V _{SS}	
F8	V _{DD} PEHA		G19	V _{DD} PEHA		J4	PE09RN2		K15	V _{DD} CORE	
F9	REFRES08		G20	V _{SS}		J5	PE09RP2		K16	V _{DD} CORE	
F10	V _{DD} PEHA		G21	V _{SS}		J6	V _{DD} PEA		K17	V _{SS}	
F11	V _{DD} PETA		G22	V _{SS}		J7	V _{DD} PEA		K18	V _{SS}	
F12	REFRESPLL		G23	V _{SS}		J8	V _{DD} PEA		K19	V _{DD} PETA	
F13	GCLKP0		G24	V _{SS}		J9	V _{SS}		K20	V _{DD} PETA	
F14	V _{DD} PEA		G25	V _{SS}		J10	V _{SS}		K21	V _{DD} PETA	
F15	V _{SS}		G26	V _{SS}		J11	V _{DD} CORE		K22	V _{SS}	
F16	REFRES02		H1	V _{SS}		J12	V _{DD} CORE		K23	V _{SS}	
F17	V _{DD} PEA		H2	V _{SS}		J13	V _{SS}		K24	V _{SS}	
F18	V _{DD} PETA		H3	V _{SS}		J14	V _{SS}		K25	V _{SS}	
F19	V _{DD} PEHA		H4	V _{SS}		J15	V _{DD} CORE		K26	V _{SS}	
F20	V _{SS}		H5	V _{SS}		J16	V _{DD} CORE		L1	V _{SS}	
F21	V _{SS}		H6	V _{DD} PEA		J17	V _{SS}		L2	V _{SS}	
F22	PE01RP2		H7	V _{DD} PEA		J18	V _{SS}		L3	V _{SS}	
F23	PE01RN2		H8	V _{DD} PEA		J19	V _{DD} PEA		L4	V _{SS}	
F24	V _{SS}		H9	V _{SS}		J20	V _{DD} PEA		L5	V _{SS}	
F25	PE01TN2		H10	V _{SS}		J21	V _{DD} PEA		L6	V _{DD} PEHA	
F26	PE01TP2		H11	V _{DD} CORE		J22	PE01RP0		L7	V _{DD} PEHA	
G1	PE09TP1		H12	V _{DD} CORE		J23	PE01RN0		L8	V _{DD} PEHA	
G2	PE09TN1		H13	V _{SS}		J24	V _{SS}		L9	V _{SS}	
G3	V _{SS}		H14	V _{SS}		J25	PE01TN0		L10	V _{SS}	
G4	PE09RN1		H15	V _{DD} CORE		J26	PE01TP0		L11	V _{DD} CORE	
G5	PE09RP1		H16	V _{DD} CORE		K1	PE09TP3		L12	V _{DD} CORE	
G6	V _{SS}		H17	V _{SS}		K2	PE09TN3		L13	V _{SS}	
G7	V _{SS}		H18	V _{SS}		K3	V _{SS}		L14	V _{SS}	
G8	V _{DD} PEHA		H19	V _{DD} PEA		K4	PE09RN3		L15	V _{DD} CORE	
G9	REFRES09		H20	V _{DD} PEA		K5	PE09RP3		L16	V _{DD} CORE	
G10	V _{DD} PEHA		H21	V _{DD} PEA		K6	V _{DD} PETA		L17	V _{SS}	
G11	V _{DD} PETA		H22	PE01RP1		K7	V _{DD} PETA		L18	V _{SS}	
G12	V _{SS}		H23	PE01RN1		K8	V _{DD} PETA		L19	V _{DD} PEHA	
G13	GCLKN0		H24	V _{SS}		K9	V _{SS}		L20	REFRES01	
G14	V _{DD} PEA		H25	PE01TN1		K10	V _{SS}		L21	V _{DD} PETA	
G15	V _{SS}		H26	PE01TP1		K11	V _{DD} CORE		L22	PE00RP3	
G16	NC		J1	PE09TP2		K12	V _{DD} CORE		L23	PE00RN3	
G17	V _{DD} PEA		J2	PE09TN2		K13	V _{SS}		L24	V _{SS}	

Table 22 PES48T12G2 Signal Pin-Out (Part 2 of 5)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
L25	PE00TN3		N10	V _{SS}		P21	V _{DD} PEA		T6	V _{DD} PETA	
L26	PE00TP3		N11	V _{DD} CORE		P22	PE00RP1		T7	V _{DD} PETA	
M1	PE04TP0		N12	V _{DD} CORE		P23	PE00RN1		T8	V _{DD} PETA	
M2	PE04TN0		N13	V _{SS}		P24	V _{SS}		T9	V _{SS}	
M3	V _{SS}		N14	V _{SS}		P25	PE00TN1		T10	V _{SS}	
M4	PE04RN0		N15	V _{DD} CORE		P26	PE00TP1		T11	V _{DD} CORE	
M5	PE04RP0		N16	V _{DD} CORE		R1	PE04TP2		T12	V _{DD} CORE	
M6	V _{SS}		N17	V _{SS}		R2	PE04TN2		T13	V _{SS}	
M7	V _{SS}		N18	V _{SS}		R3	V _{SS}		T14	V _{SS}	
M8	V _{SS}		N19	V _{DD} PEHA		R4	PE04RN2		T15	V _{DD} CORE	
M9	V _{SS}		N20	NC		R5	PE04RP2		T16	V _{DD} CORE	
M10	V _{SS}		N21	NC		R6	REFRES05		T17	V _{SS}	
M11	V _{DD} CORE		N22	NC		R7	REFRES04		T18	V _{SS}	
M12	V _{DD} CORE		N23	REFRES00		R8	V _{DD} PETA		T19	V _{DD} PEHA	
M13	V _{SS}		N24	V _{SS}		R9	V _{SS}		T20	V _{DD} PEHA	
M14	V _{SS}		N25	V _{SS}		R10	V _{SS}		T21	V _{DD} PEHA	
M15	V _{DD} CORE		N26	V _{SS}		R11	V _{DD} CORE		T22	V _{SS}	
M16	V _{DD} CORE		P1	V _{SS}		R12	V _{DD} CORE		T23	V _{SS}	
M17	V _{SS}		P2	V _{SS}		R13	V _{SS}		T24	V _{SS}	
M18	V _{SS}		P3	V _{SS}		R14	V _{SS}		T25	V _{SS}	
M19	V _{DD} PEHA		P4	V _{SS}		R15	V _{DD} CORE		T26	V _{SS}	
M20	V _{SS}		P5	V _{SS}		R16	V _{DD} CORE		U1	V _{SS}	
M21	V _{SS}		P6	NC		R17	V _{SS}		U2	V _{SS}	
M22	PE00RP2		P7	NC		R18	V _{SS}		U3	V _{SS}	
M23	PE00RN2		P8	V _{DD} PEA		R19	V _{DD} PETA		U4	V _{SS}	
M24	V _{SS}		P9	V _{SS}		R20	V _{DD} PETA		U5	V _{SS}	
M25	PE00TN2		P10	V _{SS}		R21	V _{DD} PETA		U6	V _{DD} PEHA	
M26	PE00TP2		P11	V _{DD} CORE		R22	PE00RP0		U7	V _{DD} PEHA	
N1	PE04TP1		P12	V _{DD} CORE		R23	PE00RN0		U8	V _{DD} PEHA	
N2	PE04TN1		P13	V _{SS}		R24	V _{SS}		U9	V _{SS}	
N3	V _{SS}		P14	V _{SS}		R25	PE00TN0		U10	V _{SS}	
N4	PE04RN1		P15	V _{DD} CORE		R26	PE00TP0		U11	V _{DD} CORE	
N5	PE04RP1		P16	V _{DD} CORE		T1	PE04TP3		U12	V _{DD} CORE	
N6	V _{DD} PEA		P17	V _{SS}		T2	PE04TN3		U13	V _{SS}	
N7	V _{DD} PEA		P18	V _{SS}		T3	V _{SS}		U14	V _{SS}	
N8	V _{DD} PEA		P19	V _{DD} PEA		T4	PE04RN3		U15	V _{DD} CORE	
N9	V _{SS}		P20	V _{DD} PEA		T5	PE04RP3		U16	V _{DD} CORE	

Table 22 PES48T12G2 Signal Pin-Out (Part 3 of 5)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
U17	V _{SS}		W2	PE05TN1		Y13	V _{DD} PEHA		AA24	V _{SS}	
U18	V _{SS}		W3	V _{SS}		Y14	GCLKN1		AA25	PE13TN0	
U19	V _{SS}		W4	PE05RN1		Y15	REFRES12		AA26	PE13TP0	
U20	V _{SS}		W5	PE05RP1		Y16	REFRES13		AB1	PE05TP3	
U21	V _{SS}		W6	V _{DD} PEA		Y17	V _{DD} PEA		AB2	PE05TN3	
U22	PE13RP3		W7	V _{DD} PEA		Y18	V _{DD} PEHA		AB3	V _{DD} I/O	
U23	PE13RN3		W8	V _{DD} PEA		Y19	V _{DD} PETA		AB4	PE05RN3	
U24	V _{SS}		W9	V _{SS}		Y20	V _{SS}		AB5	PE05RP3	
U25	PE13TN3		W10	V _{SS}		Y21	V _{SS}		AB6	PE06RP0	
U26	PE13TP3		W11	V _{DD} CORE		Y22	PE13RP1		AB7	PE06RP1	
V1	PE05TP0		W12	V _{DD} CORE		Y23	PE13RN1		AB8	V _{SS}	
V2	PE05TN0		W13	V _{SS}		Y24	V _{SS}		AB9	PE06RP2	
V3	V _{SS}		W14	V _{SS}		Y25	PE13TN1		AB10	PE06RP3	
V4	PE05RN0		W15	V _{DD} CORE		Y26	PE13TP1		AB11	V _{SS}	
V5	PE05RP0		W16	V _{DD} CORE		AA1	PE05TP2		AB12	PE07RP0	
V6	V _{DD} PEA		W17	V _{SS}		AA2	PE05TN2		AB13	PE07RP1	
V7	V _{DD} PEA		W18	V _{SS}		AA3	V _{DD} I/O		AB14	V _{SS}	
V8	V _{DD} PEA		W19	V _{DD} PEA		AA4	PE05RN2		AB15	PE07RP2	
V9	V _{SS}		W20	V _{DD} PEA		AA5	PE05RP2		AB16	PE07RP3	
V10	V _{SS}		W21	V _{DD} PEA		AA6	V _{SS}		AB17	V _{SS}	
V11	V _{DD} CORE		W22	V _{SS}		AA7	V _{SS}		AB18	PE12RP0	
V12	V _{DD} CORE		W23	V _{SS}		AA8	V _{DD} PETA		AB19	PE12RP1	
V13	V _{SS}		W24	V _{SS}		AA9	V _{DD} PEHA		AB20	V _{SS}	
V14	V _{SS}		W25	V _{SS}		AA10	V _{DD} PEA		AB21	PE12RP2	
V15	V _{DD} CORE		W26	V _{SS}		AA11	V _{DD} PETA		AB22	PE12RP3	
V16	V _{DD} CORE		Y1	V _{SS}		AA12	V _{DD} PETA		AB23	V _{SS}	
V17	V _{SS}		Y2	V _{SS}		AA13	V _{DD} PEHA		AB24	V _{DD} I/O	
V18	V _{SS}		Y3	V _{SS}		AA14	GCLKP1		AB25	V _{SS}	
V19	V _{DD} PEA		Y4	V _{SS}		AA15	V _{SS}		AB26	V _{SS}	
V20	V _{DD} PEA		Y5	V _{SS}		AA16	V _{SS}		AC1	V _{DD} I/O	
V21	V _{DD} PEA		Y6	V _{SS}		AA17	V _{DD} PEA		AC2	V _{DD} I/O	
V22	PE13RP2		Y7	V _{SS}		AA18	V _{DD} PEHA		AC3	V _{DD} I/O	
V23	PE13RN2		Y8	V _{DD} PETA		AA19	V _{DD} PETA		AC4	V _{SS}	
V24	V _{SS}		Y9	V _{DD} PEHA		AA20	V _{SS}		AC5	V _{SS}	
V25	PE13TN2		Y10	V _{DD} PEA		AA21	V _{SS}		AC6	PE06RN0	
V26	PE13TP2		Y11	REFRES06		AA22	PE13RP0		AC7	PE06RN1	
W1	PE05TP1		Y12	REFRES07		AA23	PE13RN0		AC8	V _{SS}	

Table 22 PES48T12G2 Signal Pin-Out (Part 4 of 5)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
AC9	PE06RN2		AD7	V _{SS}		AE5	SWMODE1		AF3	RSTHALT	
AC10	PE06RN3		AD8	V _{SS}		AE6	PE06TN0		AF4	SWMODE2	
AC11	V _{SS}		AD9	V _{SS}		AE7	PE06TN1		AF5	SWMODE3	
AC12	PE07RN0		AD10	V _{SS}		AE8	V _{SS}		AF6	PE06TP0	
AC13	PE07RN1		AD11	V _{SS}		AE9	PE06TN2		AF7	PE06TP1	
AC14	V _{SS}		AD12	V _{SS}		AE10	PE06TN3		AF8	V _{SS}	
AC15	PE07RN2		AD13	V _{SS}		AE11	V _{SS}		AF9	PE06TP2	
AC16	PE07RN3		AD14	V _{SS}		AE12	PE07TN0		AF10	PE06TP3	
AC17	V _{SS}		AD15	V _{SS}		AE13	PE07TN1		AF11	V _{SS}	
AC18	PE12RN0		AD16	V _{SS}		AE14	V _{SS}		AF12	PE07TP0	
AC19	PE12RN1		AD17	V _{SS}		AE15	PE07TN2		AF13	PE07TP1	
AC20	V _{SS}		AD18	V _{SS}		AE16	PE07TN3		AF14	V _{SS}	
AC21	PE12RN2		AD19	V _{SS}		AE17	V _{SS}		AF15	PE07TP2	
AC22	PE12RN3		AD20	V _{SS}		AE18	PE12TN0		AF16	PE07TP3	
AC23	V _{SS}		AD21	V _{SS}		AE19	PE12TN1		AF17	V _{SS}	
AC24	V _{DD} /I/O		AD22	V _{SS}		AE20	V _{SS}		AF18	PE12TP0	
AC25	GPIO_04	1	AD23	V _{SS}		AE21	PE12TN2		AF19	PE12TP1	
AC26	GPIO_08	1	AD24	V _{DD} /I/O		AE22	PE12TN3		AF20	V _{SS}	
AD1	V _{DD} /I/O		AD25	GPIO_05	2	AE23	V _{SS}		AF21	PE12TP2	
AD2	P23MERGEN		AD26	GPIO_06		AE24	V _{DD} /I/O		AF22	PE12TP3	
AD3	P1213MERGEN		AE1	P01MERGEN		AE25	GPIO_02	1	AF23	V _{SS}	
AD4	GCLKFSEL		AE2	P67MERGEN		AE26	GPIO_07		AF24	GPIO_01	1
AD5	SWMODE0		AE3	P89MERGEN		AF1	CLKMODE0		AF25	GPIO_00	1
AD6	V _{SS}		AE4	V _{DD} /I/O		AF2	P45MERGEN		AF26	GPIO_03	1

Table 22 PES48T12G2 Signal Pin-Out (Part 5 of 5)

Alternate Signal Functions

Pin	GPIO	1st Alternate	2nd Alternate
AF25	GPIO_00	PART0PERSTN	—
AF24	GPIO_01	PART1PERSTN	—
AE25	GPIO_02	PART2PERSTN	—
AF26	GPIO_03	PART3PERSTN	—
AC25	GPIO_04	—	POLINKUPN
AD25	GPIO_05	GPEN	POACTIVEN
AC26	GPIO_08	IOEXPINTN	—

Table 23 PES48T12G2 Alternate Signal Functions

Power Pins

V _{DD} Core	V _{DD} Core	V _{DD} I/O	V _{DD} PEA	V _{DD} PEA	V _{DD} PEHA	V _{DD} PETA
H11	P11	A3	F14	P19	F8	F11
H12	P12	A22	F17	P20	F10	F18
H15	P15	B3	G14	P21	F19	G11
H16	P16	B22	G17	V6	G8	G18
J11	R11	D1	H6	V7	G10	K6
J12	R12	D2	H7	V8	G19	K7
J15	R15	D25	H8	V19	L6	K8
J16	R16	D26	H19	V20	L7	K19
K11	T11	AA3	H20	V21	L8	K20
K12	T12	AB3	H21	W6	L19	K21
K15	T15	AB24	J6	W7	M19	L21
K16	T16	AC1	J7	W8	N19	R8
L11	U11	AC2	J8	W19	T19	R19
L12	U12	AC3	J19	W20	T20	R20
L15	U15	AC24	J20	W21	T21	R21
L16	U16	AD1	J21	Y10	U6	T6
M11	V11	AD24	N6	Y17	U7	T7
M12	V12	AE4	N7	AA10	U8	T8
M15	V15	AE24	N8	AA17	Y9	Y8
M16	V16		P8	—	Y13	Y19
N11	W11				Y18	AA8
N12	W12				AA9	AA11
N15	W15				AA13	AA12
N16	W16				AA18	AA19

Table 24 PES48T12G2 Power Pins

No Connection Pins

NC	
G16	N22
N20	P6
N21	P7

Table 25 PES48T12G2 No Connection Pins

Ground Pins

V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}
A1	C19	G20	K22	N14	T23	W22	AC14
A2	C20	G21	K23	N17	T24	W23	AC17
A4	C21	G22	K24	N18	T25	W24	AC20
A7	C22	G23	K25	N24	T26	W25	AC23
A10	D3	G24	K26	N25	U1	W26	AD6
A13	D4	G25	L1	N26	U2	Y1	AD7
A16	D7	G26	L2	P1	U3	Y2	AD8
A19	D10	H1	L3	P2	U4	Y3	AD9
B1	D16	H2	L4	P3	U5	Y4	AD10
B2	D19	H3	L5	P4	U9	Y5	AD11
B4	D23	H4	L9	P5	U10	Y6	AD12
B7	D24	H5	L10	P9	U13	Y7	AD13
B10	E1	H9	L13	P10	U14	Y20	AD14
B13	E2	H10	L14	P13	U17	Y21	AD15
B16	E3	H13	L17	P14	U18	Y24	AD16
B19	E4	H14	L18	P17	U19	AA6	AD17
C1	E7	H17	L24	P18	U20	AA7	AD18
C2	E10	H18	M3	P24	U21	AA15	AD19
C3	E13	H24	M6	R3	U24	AA16	AD20
C4	E16	J3	M7	R9	V3	AA20	AD21
C5	E19	J9	M8	R10	V9	AA21	AD22
C6	E24	J10	M9	R13	V10	AA24	AD23
C7	F3	J13	M10	R14	V13	AB8	AE8
C8	F6	J14	M13	R17	V14	AB11	AE11
C9	F7	J17	M14	R18	V17	AB14	AE14
C10	F15	J18	M17	R24	V18	AB17	AE17
C11	F20	J24	M18	T3	V24	AB20	AE20
C12	F21	K3	M20	T9	W3	AB23	AE23
C13	F24	K9	M21	T10	W9	AB25	AF8
C14	G3	K10	M24	T13	W10	AB26	AF11
C15	G6	K13	N3	T14	W13	AC4	AF14
C16	G7	K14	N9	T17	W14	AC5	AF17
C17	G12	K17	N10	T18	W17	AC8	AF20
C18	G15	K18	N13	T22	W18	AC11	AF23

Table 26 PES48T12G2 Ground Pins

Signals Listed Alphabetically

Signal Name	I/O Type	Location	Signal Category
CLKMODE0	I	AF1	System
CLKMODE1		A25	
GCLKFSEL		AD4	
GCLKN0		G13	
GCLKN1		Y14	
GCLKP0		F13	
GCLKP1		AA14	
GPIO_00	I/O	AF25	General Purpose I/O
GPIO_01		AF24	
GPIO_02		AE25	
GPIO_03		AF26	
GPIO_04		AC25	
GPIO_05		AD25	
GPIO_06		AD26	
GPIO_07		AE26	
GPIO_08		AC26	
JTAG_TCK	I	A26	Test
JTAG_TDI	I	C24	
JTAG_TDO	O	C23	
JTAG_TMS	I	A24	
JTAG_TRST_N	I	D22	
MSMBCLK	I/O	B23	SMBus Interface
MSMBDAT		A23	
NO CONNECT	See Table 25 for a listing of No Connect pins.		
P01MERGEN	I	AE1	System
P23MERGEN		AD2	
P45MERGEN		AF2	
P67MERGEN		AE2	
P89MERGEN		AE3	
P1213MERGEN		AD3	

Table 27 PES48T12G2 Alphabetical Signal List (Part 1 of 8)

Signal Name	I/O Type	Location	Signal Category
PE00RN0	I	R23	PCI Express
PE00RN1		P23	
PE00RN2		M23	
PE00RN3		L23	
PE00RP0		R22	
PE00RP1		P22	
PE00RP2		M22	
PE00RP3		L22	
PE00TN0	O	R25	
PE00TN1		P25	
PE00TN2		M25	
PE00TN3		L25	
PE00TP0		R26	
PE00TP1		P26	
PE00TP2		M26	
PE00TP3		L26	
PE01RN0	I	J23	
PE01RN1		H23	
PE01RN2		F23	
PE01RN3		E23	
PE01RP0		J22	
PE01RP1		H22	
PE01RP2		F22	
PE01RP3		E22	
PE01TN0	O	J25	
PE01TN1		H25	
PE01TN2		F25	
PE01TN3		E25	
PE01TP0		J26	
PE01TP1		H26	
PE01TP2		F26	
PE01TP3		E26	

Table 27 PES48T12G2 Alphabetical Signal List (Part 2 of 8)

Signal Name	I/O Type	Location	Signal Category
PE02RN0	I	D21	PCI Express (cont.)
PE02RN1		D20	
PE02RN2		D18	
PE02RN3		D17	
PE02RP0		E21	
PE02RP1		E20	
PE02RP2		E18	
PE02RP3		E17	
PE02TN0	O	B21	
PE02TN1		B20	
PE02TN2		B18	
PE02TN3		B17	
PE02TP0		A21	
PE02TP1		A20	
PE02TP2		A18	
PE02TP3		A17	
PE03RN0	I	D15	
PE03RN1		D14	
PE03RN2		D12	
PE03RN3		D11	
PE03RP0		E15	
PE03RP1		E14	
PE03RP2		E12	
PE03RP3		E11	
PE03TN0	O	B15	
PE03TN1		B14	
PE03TN2		B12	
PE03TN3		B11	
PE03TP0		A15	
PE03TP1		A14	
PE03TP2		A12	
PE03TP3		A11	

Table 27 PES48T12G2 Alphabetical Signal List (Part 3 of 8)

Signal Name	I/O Type	Location	Signal Category
PE04RN0	I	M4	PCI Express (cont.)
PE04RN1		N4	
PE04RN2		R4	
PE04RN3		T4	
PE04RP0		M5	
PE04RP1		N5	
PE04RP2		R5	
PE04RP3		T5	
PE04TN0	O	M2	
PE04TN1		N2	
PE04TN2		R2	
PE04TN3		T2	
PE04TP0		M1	
PE04TP1		N1	
PE04TP2		R1	
PE04TP3		T1	
PE05RN0	I	V4	
PE05RN1		W4	
PE05RN2		AA4	
PE05RN3		AB4	
PE05RP0		V5	
PE05RP1		W5	
PE05RP2		AA5	
PE05RP3		AB5	
PE05TN0	O	V2	
PE05TN1		W2	
PE05TN2		AA2	
PE05TN3		AB2	
PE05TP0		V1	
PE05TP1		W1	
PE05TP2		AA1	
PE05TP3		AB1	

Table 27 PES48T12G2 Alphabetical Signal List (Part 4 of 8)

Signal Name	I/O Type	Location	Signal Category
PE06RN0	I	AC6	PCI Express (cont.)
PE06RN1		AC7	
PE06RN2		AC9	
PE06RN3		AC10	
PE06RP0		AB6	
PE06RP1		AB7	
PE06RP2		AB9	
PE06RP3		AB10	
PE06TN0	O	AE6	
PE06TN1		AE7	
PE06TN2		AE9	
PE06TN3		AE10	
PE06TP0		AF6	
PE06TP1		AF7	
PE06TP2		AF9	
PE06TP3		AF10	
PE07RN0	I	AC12	
PE07RN1		AC13	
PE07RN2		AC15	
PE07RN3		AC16	
PE07RP0		AB12	
PE07RP1		AB13	
PE07RP2		AB15	
PE07RP3		AB16	
PE07TN0	O	AE12	
PE07TN1		AE13	
PE07TN2		AE15	
PE07TN3		AE16	
PE07TP0		AF12	
PE07TP1		AF13	
PE07TP2		AF15	
PE07TP3		AF16	

Table 27 PES48T12G2 Alphabetical Signal List (Part 5 of 8)

Signal Name	I/O Type	Location	Signal Category
PE08RN0	I	D9	PCI Express (cont.)
PE08RN1		D8	
PE08RN2		D6	
PE08RN3		D5	
PE08RP0		E9	
PE08RP1		E8	
PE08RP2		E6	
PE08RP3		E5	
PE08TN0	O	B9	
PE08TN1		B8	
PE08TN2		B6	
PE08TN3		B5	
PE08TP0		A9	
PE08TP1		A8	
PE08TP2		A6	
PE08TP3		A5	
PE09RN0	I	F4	
PE09RN1		G4	
PE09RN2		J4	
PE09RN3		K4	
PE09RP0		F5	
PE09RP1		G5	
PE09RP2		J5	
PE09RP3		K5	
PE09TN0	O	F2	
PE09TN1		G2	
PE09TN2		J2	
PE09TN3		K2	
PE09TP0		F1	
PE09TP1		G1	
PE09TP2		J1	
PE09TP3		K1	

Table 27 PES48T12G2 Alphabetical Signal List (Part 6 of 8)

Signal Name	I/O Type	Location	Signal Category
PE12RN0	I	AC18	PCI Express (cont.)
PE12RN1		AC19	
PE12RN2		AC21	
PE12RN3		AC22	
PE12RP0		AB18	
PE12RP1		AB19	
PE12RP2		AB21	
PE12RP3		AB22	
PE12TN0	O	AE18	
PE12TN1		AE19	
PE12TN2		AE21	
PE12TN3		AE22	
PE12TP0		AF18	
PE12TP1		AF19	
PE12TP2		AF21	
PE12TP3		AF22	
PE13RN0	I	AA23	
PE13RN1		Y23	
PE13RN2		V23	
PE13RN3		U23	
PE13RP0		AA22	
PE13RP1		Y22	
PE13RP2		V22	
PE13RP3		U22	
PE13TN0	O	AA25	
PE13TN1		Y25	
PE13TN2		V25	
PE13TN3		U25	
PE13TP0		AA26	
PE13TP1		Y26	
PE13TP2		V26	
PE13TP3		U26	

Table 27 PES48T12G2 Alphabetical Signal List (Part 7 of 8)

Signal Name	I/O Type	Location	Signal Category
PERSTN	I	B24	System
REFRES00	I/O	N23	SerDes Reference Resistors
REFRES01		L20	
REFRES02		F16	
REFRES03		D13	
REFRES04		R7	
REFRES05		R6	
REFRES06		Y11	
REFRES07		Y12	
REFRES08		F9	
REFRES09		G9	
REFRES12		Y15	
REFRES13		Y16	
REFRESPLL		F12	
RSTHALT		I	
SSMBADDR1	I	C26	SMBus Interface
SSMBADDR2	I	B26	
SSMBCLK	I/O	C25	
SSMBDAT	I/O	B25	
SWMODE0	I	AD5	
SWMODE1		AE5	
SWMODE2		AF4	
SWMODE3		AF5	
V _{DD} CORE, V _{DD} I/O, V _{DD} PEA, V _{DD} PEHA, V _{DD} - PETA	See Table 24 for a listing of power pins.		
V _{SS}	See Table 26 for a listing of ground pins.		

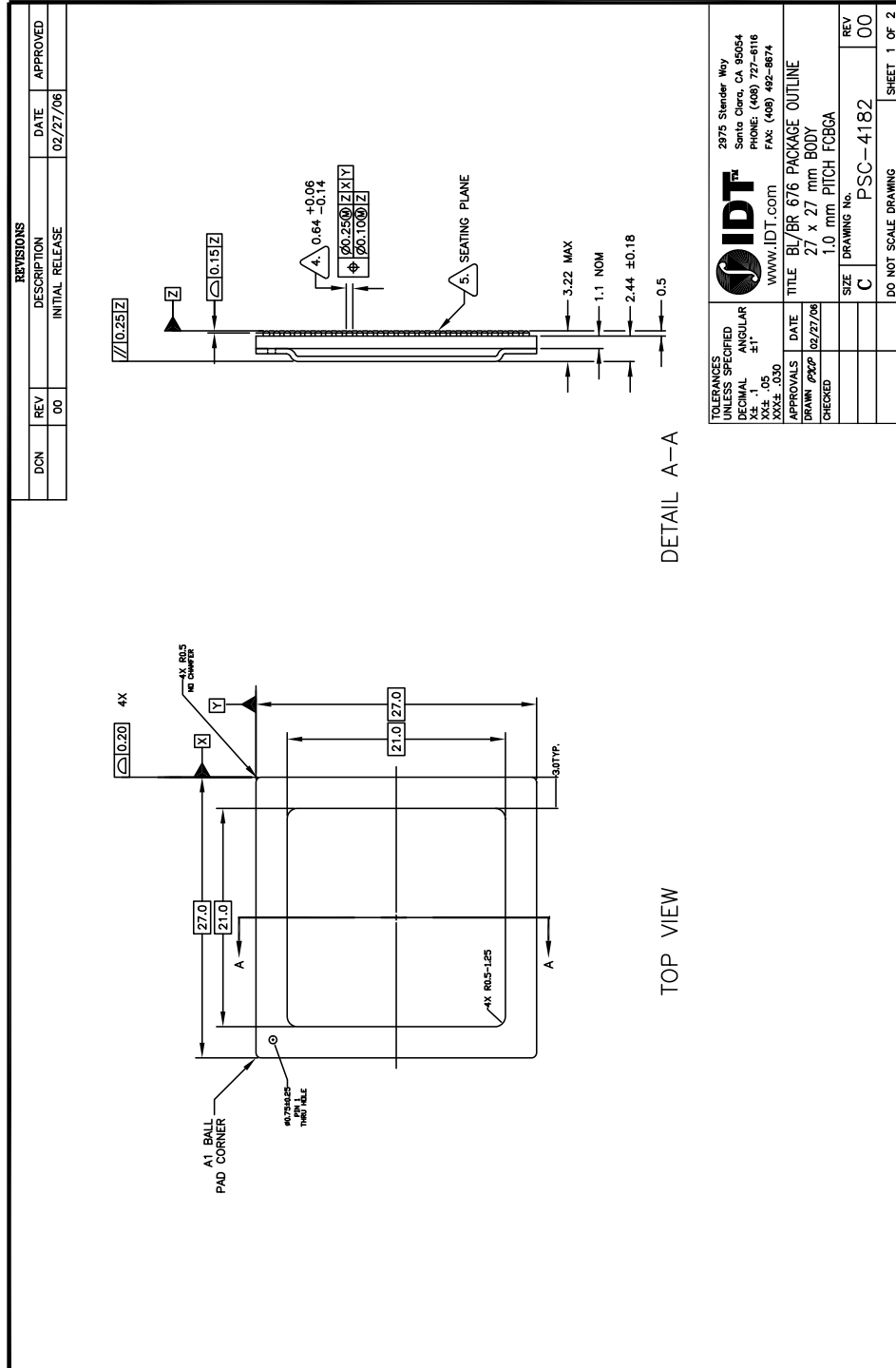
Table 27 PES48T12G2 Alphabetical Signal List (Part 8 of 8)

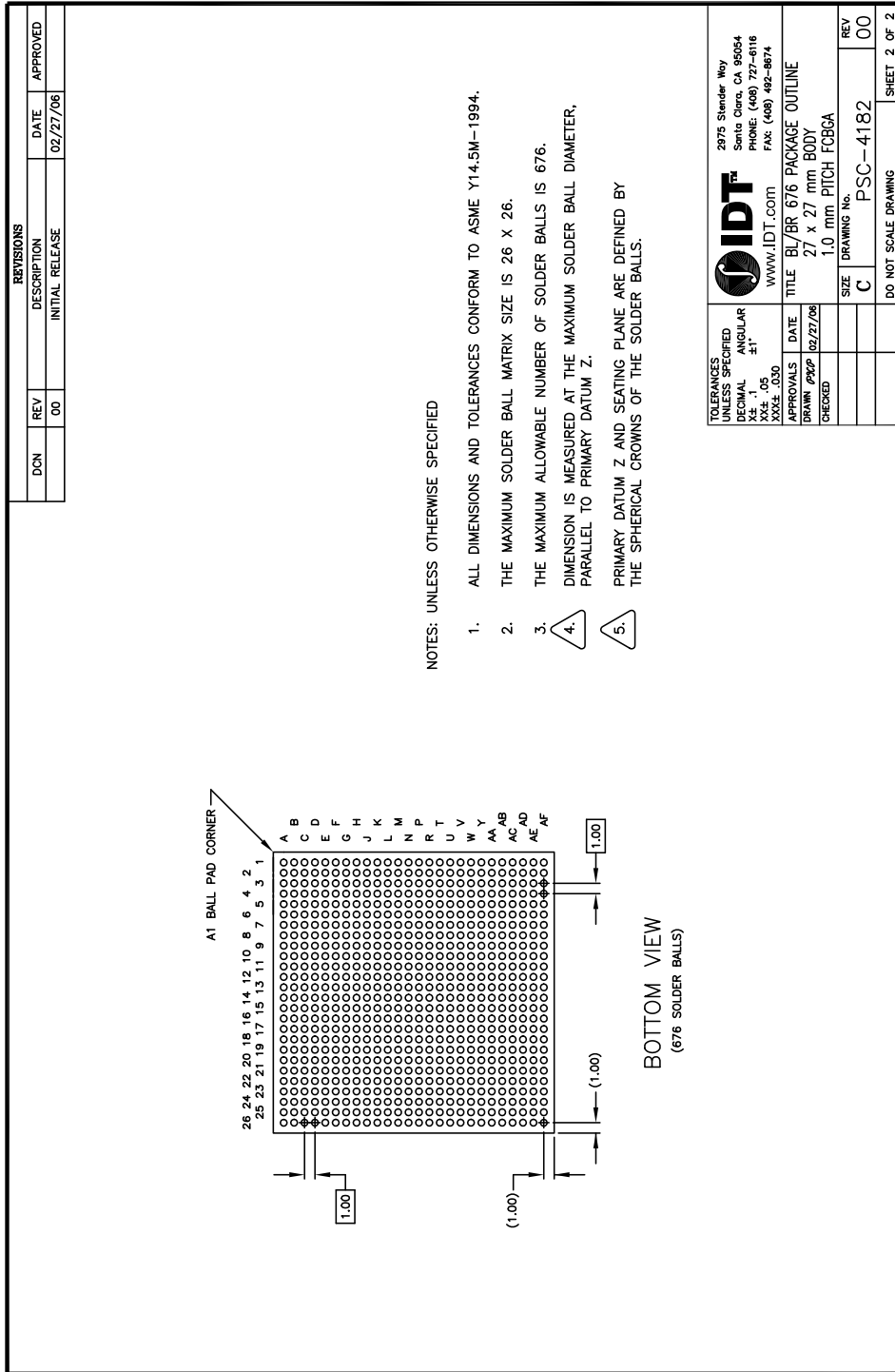
PES48T12G2 Pinout — Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A																											A
B																											B
C																											C
D																											D
E																											E
F																											F
G																											G
H																											H
J																											J
K																											K
L																											L
M																											M
N																											N
P																											P
R																											R
T																											T
U																											U
V																											V
W																											W
Y																											Y
AA																											AA
AB																											AB
AC																											AC
AD																											AD
AE																											AE
AF																											AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

	V _{DD} Core (Power)		V _{DD} PETA (Transmitter Power)		Signals
	V _{DD} I/O (Power)		V _{DD} PEA (Analog Power)		No Connect
	V _{SS} (Ground)		V _{DD} PEHA (High Analog Power)		

PES48T12G2 Package Drawing — 676-Pin BL676/BLG676





REVISIONS			
DCN	REV	DESCRIPTION	DATE
	00	INITIAL RELEASE	02/27/06
			APPROVED

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR X.X: .1 1° X.XX: .05 1/2° APPROVALS DATE DRAWN: PWP 02/27/06 CHECKED:		2975 Slender Way Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 482-8874 WWW.IDT.COM TITLE: BL/BR 676 PACKAGE OUTLINE 27 x 27 mm BODY 1.0 mm PITCH FCBGA SIZE: DRAWING No. PSC-4182 REV: 00	
		DO NOT SCALE DRAWING	
		SHEET 2 OF 2	

Revision History

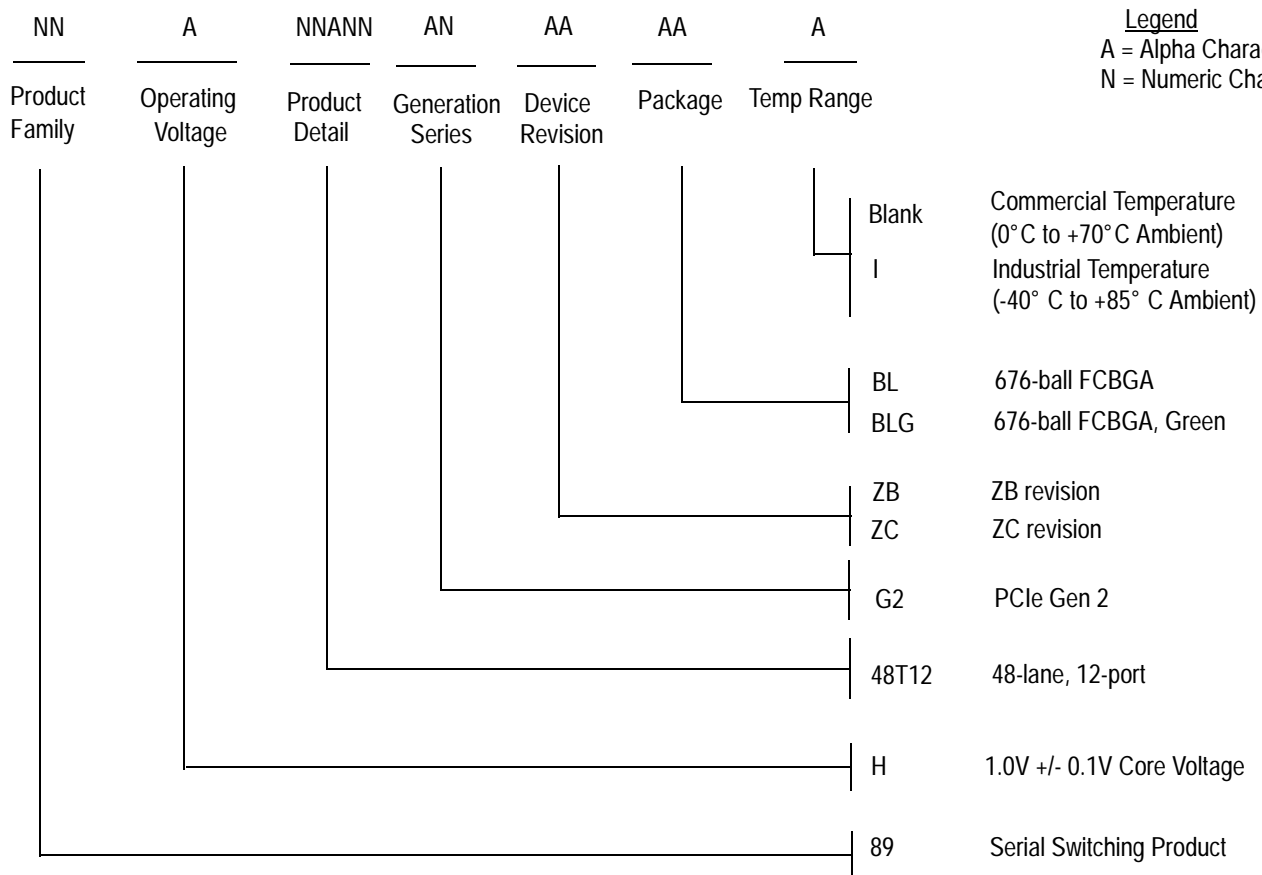
January 21, 2010: Publication of Final data sheet.

March 30, 2011: In Table 13, added $V_{DD}PETA$ to footnote #1.

November 18, 2011: Added new Table 20, SMBus DC Characterization Data.

November 28, 2011: Added new Tables 20 and 21, SMBus Characterization and Timing.

Ordering Information



Valid Combinations

- 89H48T12G2ZBBL 676-ball FCBGA package, Commercial Temperature
- 89H48T12G2ZBBLG 676-ball Green FCBGA package, Commercial Temperature
- 89H48T12G2ZBBLI 676-ball FCBGA package, Industrial Temperature
- 89H48T12G2ZBBLGI 676-ball Green FCBGA package, Industrial Temperature
- 89H48T12G2ZCBL 676-ball FCBGA package, Commercial Temperature
- 89H48T12G2ZCBLG 676-ball Green FCBGA package, Commercial Temperature
- 89H48T12G2ZCBLI 676-ball FCBGA package, Industrial Temperature
- 89H48T12G2ZCBLGI 676-ball Green FCBGA package, Industrial Temperature

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.