24-Lane 3-Port PCI Express® Switch

89HPES24N3
Data Sheet

Device Overview

The 89HPES24N3 is a member of IDT's PRECISE™ family of PCI Express® switching solutions offering the next-generation I/O interconnect standard. The PES24N3 is a 24-lane, 3-port peripheral chip that performs PCI Express Base switching with a feature set optimized for high performance applications such as servers, storage, and communications/networking. It provides high-performance I/O connectivity and switching functions between a PCIe® upstream port and two downstream ports or peer-to-peer switching between downstream ports.

Features

- High Performance PCI Express Switch
  - *24 PCI Express lanes (2.5Gbps), 3 switch ports*
  - *Delivers 12 GBps (96 Gbps) aggregate switching capacity*
  - *Low latency cut-through switch architecture*
  - *Supports 128 to 2048 byte maximum payload size*
  - *Supports one virtual channel*
  - *PCI Express Base specification Revision 1.0a compliant*
- Flexible Architecture with Numerous Configuration Options
  - *Port arbitration schemes utilizing round robin or weighted round robin algorithms*
  - *Supports automatic per port link with negotiation (x8, x4, x2, or x1)*
  - *Supports static lane reversal on all ports*
  - *Supports polarity inversion*
  - *Supports locked transactions, allowing use with legacy software*
  - *Ability to load device configuration from serial EEPROM*
- Highly Integrated Solution
  - *Requires no external components*
  - *Incorporates on-chip internal memory for packet buffering and queueing*
  - *Integrates 24 2.5 Gbps embedded SerDes, 8B/10B encoder/decoder (no separate transceivers needed)*
- Reliability, Availability, and Serviceability (RAS) Features
  - *Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)*
  - *Supports ECRC passed through*
  - *Supports PCI Express Native Hot-Plug*
    - *Compatible with Hot-Plug I/O expanders used on PC motherboards*
  - *Supports Hot-Swap*
- Power Management
  - *Supports PCI Express Power Management Interface specification, Revision 1.1 (PCI-PM)*
  - *Unused SerDes are disabled*
  - *Supports Advanced Configuration and Power Interface Specification, Revision 2.0 (ACPI) supporting active link state*
- Testability and Debug Features
  - *Built in SerDes Pseudo-Random Bit Stream (PRBS) generator*
  - *Ability to read and write any internal register via the SMBus*

Block Diagram

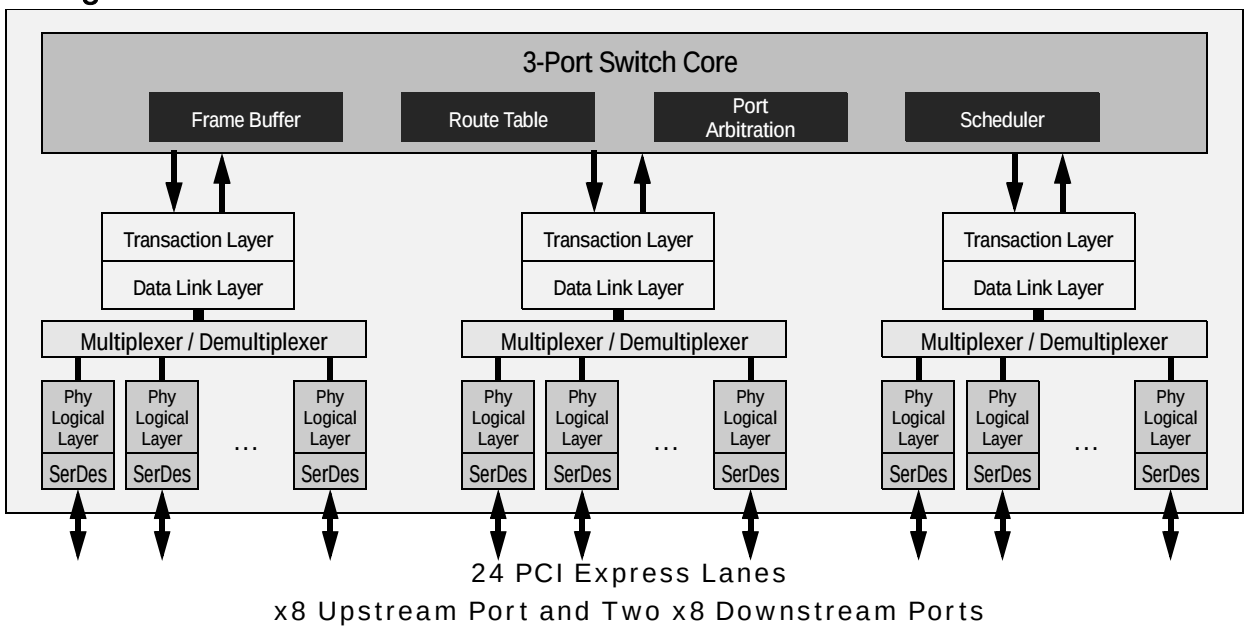


Figure 1 Internal Block Diagram

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- *Ability to bypass link training and force any link into any mode*
- *Provides statistics and performance counters*

- Two SMBus Interfaces
  - *Slave interface provides full access to all software-visible registers by an external SMBus master*
  - *Master interface provides connection for an optional serial EEPROM used for initialization*
  - *Master interface is also used by an external Hot-Plug I/O expander*
  - *Master and slave interfaces may be tied together so the PES24N3 can act as both master and slave*
- 8 General Purpose Input/Output pins
- Packaged in 27x27mm 420 ball BGA with 1mm ball spacing

Product Description

Utilizing standard PCI Express interconnect, the PES24N3 provides the most efficient high-performance I/O connectivity solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. It provides 12 GBps (96 Gbps) of aggregated, full-duplex switching capacity through 24 integrated serial lanes, using proven and robust IDT technology. Each lane provides 2.5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification 1.0a.

The PES24N3 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 1.0a. The PES24N3 can operate either as a store and forward or cut-through switch depending on the packet size and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management. This includes system selectable algorithms such as round robin, weighted round-robin, and strict priority schemes guaranteeing bandwidth allocation and/or latency for critical traffic classes in applications such as high throughput 10 Gigabit I/Os, SATA controllers, and Fibre Channel HBAs.

Switch Configuration

The PES24N3 is a three port switch that contains 24 PCI Express lanes. Each of the three ports is statically allocated 8 lanes with ports labeled as A, B and C. Port A is always the upstream port while ports B and C are always downstream ports. The switch operating mode, as well as an optional initialization from a serial EEPROM, is selected via the Switch Mode (SWMODE[3:0]) inputs.

During link training, link width is automatically negotiated. Each PES24N3 port is capable of independently negotiating to a x8, x4, x2 or x1 width. Thus, the PES24N3 may be used in virtually any three port switch configuration (e.g., {x8, x8, x8}, {x4, x4, x4}, {x4, x2, x1}, etc.). The PES24N3 supports static lane reversal. For example, lane reversal for upstream port A may be configured by asserting the PCI Express Port A Lane Reverse (PEALREV) input signal or through serial EEPROM or SMBus initialization. Lane reversal for ports B and C may be enabled via a configuration space register, serial EEPROM, or the SMBus.

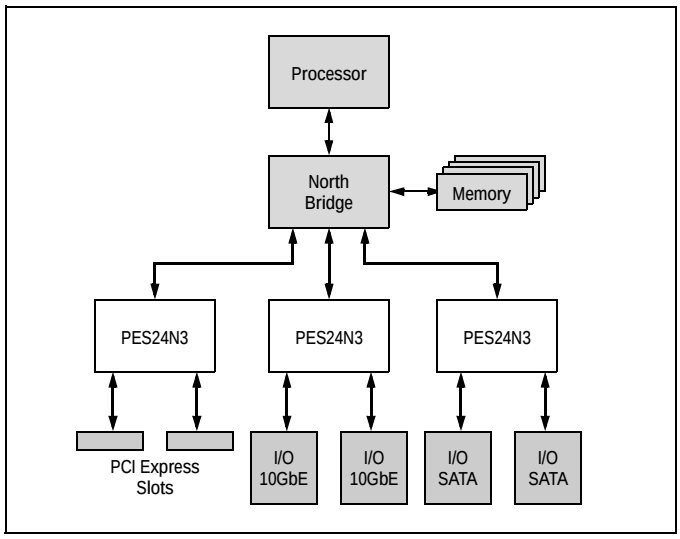


Figure 2 I/O Expansion Application

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Pin Description

The following tables list the functions of the pins provided on the PES24N3. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an "N" are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Signal	Type	Name/Description
PEALREV	I	**PCI Express Port A Lane Reverse.** When this bit is asserted, the lanes of PCI Express Port A are reversed. This value may be overridden by modifying the value of the PALREV bit in the PA_SWCTL register.
PEARP[7:0] PEARN[7:0]	I	**PCI Express Port A Serial Data Receive.** Differential PCI Express receive pairs for port A.
PEATP[7:0] PEATN[7:0	O	**PCI Express Port A Serial Data Transmit.** Differential PCI Express transmit pairs for port A
PEBLREV	I	**PCI Express Port B Lane Reverse.** When this bit is asserted, the lanes of PCI Express Port B are reversed. This value may be overridden by modifying the value of the PBLREV bit in the PA_SWCTL register.
PEBRP[7:0] PEBRN[7:0]	I	**PCI Express Port B Serial Data Receive.** Differential PCI Express receive pairs for port B.
PEBTP[7:0] PEBTN[7:0]	O	**PCI Express Port B Serial Data Transmit.** Differential PCI Express transmit pairs for port B
PECLREV	I	**PCI Express Port C Lane Reverse.** When this bit is asserted, the lanes of PCI Express Port C are reversed. This value may be overridden by modifying the value of the PCLREV bit in the PA_SWCTL register.
PECRP[7:0] PECRN[7:0]	I	**PCI Express Port C Serial Data Receive.** Differential PCI Express receive pairs for port C.
PECTP[7:0] PECTN[7:0]	O	**PCI Express Port C Serial Data Transmit.** Differential PCI Express transmit pairs for port C
PEREFCLKP[1:0] PEREFCLKN[1:0]	I	**PCI Express Reference Clock.** Differential reference clock pair input. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic and on-chip SerDes. The frequency of the differential reference clock is determined by the REFCLKM signal.
REFCLKM	I	**PCI Express Reference Clock Mode Select.** These signals select the frequency of the reference clock input. 0x0 - 100 MHz 0x1 - 125 MHz

Table 1 PCI Express Interface Pins

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Signal	Type	Name/Description
MSMBADDR[4:1]	I	**Master SMBus Address.** These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded.
MSMBCLK	I/O	**Master SMBus Clock.** This bidirectional signal is used to synchronize transfers on the master SMBus.
MSMBDAT	I/O	**Master SMBus Data.** This bidirectional signal is used for data on the master SMBus.
SSMBADDR[5,3:1]	I	**Slave SMBus Address.** These pins determine the SMBus address to which the slave SMBus interface responds.
SSMBCLK	I/O	**Slave SMBus Clock.** This bidirectional signal is used to synchronize transfers on the slave SMBus.
SSMBDAT	I/O	**Slave SMBus Data.** This bidirectional signal is used for data on the slave SMBus.

Table 2 SMBus Interface Pins

Signal	Type	Name/Description
GPIO[0]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[1]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[2]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN Alternate function pin type: Input Alternate function: Hot-Plug I/O expander interrupt input
GPIO[3]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PAABN Alternate function pin type: Input Alternate function: Port A attention button input
GPIO[4]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PAAIN Alternate function pin type: Output Alternate function: Port A attention indicator output
GPIO[5]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PAPIN Alternate function pin type: Output Alternate function: Port A power indicator output
GPIO[6]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[7]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.

Table 3 General Purpose I/O Pins

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Signal	Type	Name/Description
CCLKDS	I	**Common Clock Downstream.** The assertion of this pin indicates that all downstream ports are using the same clock source as that provided to downstream devices.This bit is used as the initial value of the Slot Clock Configuration bit in all of the Link Status Registers for downstream ports. The value may be override by modifying the SCLK bit in the PB_PCIELSTS or PC_PCIELSTS register.
CCLKUS	I	**Common Clock Upstream.** The assertion of this pin indicates that the upstream port is using the same clock source as the upstream device. This bit is used as the initial value of the Slot Clock Configuration bit in the Link Status Register for the upstream port. The value may be overridden by modifying the SCLK bit in the PA_PCIELSTS register.
MSMBSMODE	I	**Master SMBus Slow Mode.** The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 KHz. This value may not be overridden.
PERSTN	I	**Fundamental Reset.** Assertion of this signal resets all logic inside the PES24N3 and initiates a PCI Express fundamental reset.
RSTHALT	I	**Reset Halt.** When this signal is asserted during a PCI Express fundamental reset, the PES24N3 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the PA_SWCTL register by an SMBus master.
TSTRSVD	I	**Reserved.** Reserved for future test mode. Must be tied to ground.
SWMODE[3:0]	I	**Switch Mode.** These configuration pins determine the PES24N3 switch operating mode. 0x0 - Transparent mode 0x1 -Transparent mode with serial EEPROM initialization 0x2 through 0x7 - Reserved 0x8 - 10-bit loopback test mode 0x9 - Reserved 0xA - Internal pseudo random bit stream self-test test mode 0xB - External pseudo random bit stream self-test test mode 0xC - Reserved 0xD - SerDes broadcast test mode 0xE - 0xF Reserved

Table 4 System Pins

Signal	Type	Name/Description
JTAG_TCK	I	**JTAG Clock.** This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	**JTAG Data Input.** This is the serial data input to the boundary scan logic or JTAG Controller.

Table 5 Test Pins (Part 1 of 2)

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Signal	Type	Name/Description
JTAG_TDO	O	**JTAG Data Output**. This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	**JTAG Mode**. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.
JTAG_TRST_N	I	**JTAG Reset**. This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 5 Test Pins (Part 2 of 2)

Signal	Type	Name/Description
V_{DD}CORE	I	**Core V_{DD}**. Power supply for core logic.
V_{DD}IO	I	**I/O V_{DD}**. LVTTL I/O buffer power supply.
V_{DD}PE	I	**PCI Express Digital Power**. PCI Express digital power used by the digital power of the SerDes.
V_{DD}APE	I	**PCI Express Analog Power**. PCI Express analog power used by the PLL and bias generator.
V_{TT}PE	I	**PCI Express Termination Power**.
V_{SS}	I	Ground.

Table 6 Power and Ground Pins

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Pin Characteristics

Note: Some input pads of the PES24N3 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any input pin left floating can cause a slight increase in power consumption.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes
PCI Express Interface	PEALREV	I	LVTTL	Input	pull-down	
	PEARN[7:0]	I	CML	Serial link		
	PEARP[7:0]	I				
	PEATN[7:0]	O				
	PEATP[7:0]	O				
	PEBLREV	I	LVTTL	Input	pull-down	
	PEBRN[7:0]	I	CML	Serial link		
	PEBRP[7:0]	I				
	PEBTN[7:0]	O				
	PEBTP[7:0]	O				
	PECLREV	I	LVTTL	Input	pull-down	
	PECRN[7:0]	I	CML	Serial link		
	PECRP[7:0]	I				
	PECTN[7:0]	O				
	PECTP[7:0]	O				
	PEREFCLKN[1:0]	I	LVPECL/ CML	Diff. Clock Input		Refer to Table 8
	PEREFCLKP[1:0]	I				
	REFCLKM	I	LVTTL	Input	pull-down	
SMBus	MSMBADDR[4:1]	I	LVTTL	Input	pull-up	
	MSMBCLK	I/O		STI		
	MSMBDAT	I/O				
	SSMBADDR[5,3:1]	I		Input	pull-up	
	SSMBCLK	I/O		STI		
	SSMBDAT	I/O				
General Purpose I/O	GPIO[7:0]	I/O	LVTTL	Input, High Drive	pull-up	
System Pins	CCLKDS	I	LVTTL	Input	pull-up	
	CCLKUS	I			pull-up	
	MSMBSMODE	I			pull-down	
	PERSTN	I				
	RSTHALT	I			pull-down	
	TSTRSVD	I			pull-down	External pulldown
	SWMODE[3:0]	I			pull-up	

Table 7 Pin Characteristics (Part 1 of 2)

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Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes
JTAG	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDI	I			pull-up	
	JTAG_TDO	O		Low Drive		
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I			pull-up	External pulldown

Table 7 Pin Characteristics (Part 2 of 2)

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Logic Diagram — PES24N3

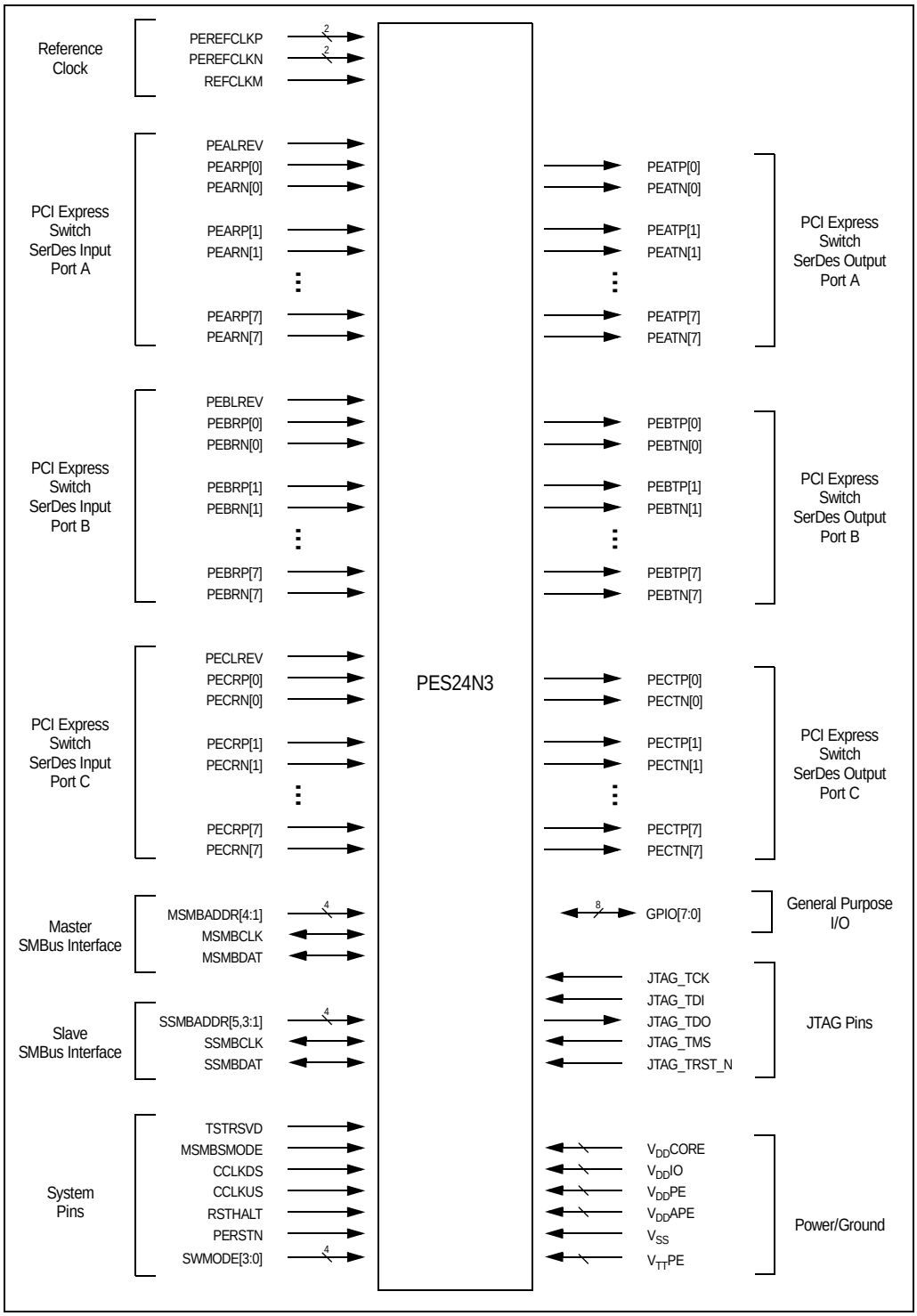


Figure 3 PES24N3 Logic Diagram

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System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 12 and 13.

Parameter	Description	Min	Typical	Max	Unit
$Refclk_{FREQ}$	Input reference clock frequency range	100		125[1]	MHz
$Refclk_{DC}$[2]	Duty cycle of input clock	40	50	60	%
T_R, T_F	Rise/Fall time of input clocks			0.2*RCUI	RCUI[3]
V_{SW}	Differential input voltage swing[4]	0.6		1.6	V
T_{jitter}	Input clock jitter (cycle-to-cycle)			125	ps

Table 8 Input Clock Requirements

1. The input clock frequency will be either 100 or 125 MHz depending on signal REFCLKM.
2. ClkIn must be AC coupled. Use 0.01 — 0.1 µF ceramic capacitors.
3. RCUI (Reference Clock Unit Interval) refers to the reference clock period.
4. AC coupling required.

AC Timing Characteristics

Parameter	Description	Min[1]	Typical[1]	Max[1]	Units
PCIe Transmit					
UI	Unit Interval	399.88	400	400.12	ps
T_{TX-EYE}	Minimum Tx Eye Width	0.7	.9		UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.15	UI
$T_{TX-RISE}$, $T_{TX-FALL}$	D+ / D- Tx output rise/fall time	50	90		ps
$T_{TX-IDLE-MIN}$	Minimum time in idle	50			UI
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Idle after sending an Idle ordered set			20	UI
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition from valid idle to diff data			20	UI
$T_{TX-IDLE-RCV-DET-MAX}$	Max time spend in idle before initiating a RX detect sequence		20	100	ms
$T_{TX-SKEW}$	Transmitter data skew between any 2 lanes		500	1300	ps
PCIe Receive					
UI	Unit Interval	399.88	400	400.12	ps
$T_{RX-EYE (with jitter)}$	Minimum Receiver Eye Width (jitter tolerance)	0.4			UI

Table 9 PCIe AC Timing Characteristics (Part 1 of 2)

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Parameter	Description	Min[1]	Typical[1]	Max[1]	Units
$T_{RX-EYE-MEDIUM\ TO\ MAX\ JITTER}$	Max time between jitter median & max deviation			0.3	UI
$T_{RX-IDLE-DET-DIFF-ENTER\ TIME}$	Unexpected Idle Enter Detect Threshold Integration Time			10	ms
$T_{RX-SKEW}$	Lane to lane input skew			20	ns

Table 9 PCIe AC Timing Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.0a

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
GPIO						
GPIO[7:0][1]	Tpw_13b[2]	None	50	—	ns	

Table 10 GPIO AC Timing Characteristics

1. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.
2. The values for this symbol were determined by calculation, not by testing.

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
JTAG						
JTAG_TCK	Tper_16a	none	50.0	—	ns	See Figure 4.
	Thigh_16a, Tlow_16a		10.0	25.0	ns	
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	ns	
	Thld_16b		1.0	—	ns	
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	20	ns	
	Tdz_16c[2]		—	20	ns	
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	ns	

Table 11 JTAG AC Timing Characteristics

1. The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.
2. The values for this symbol were determined by calculation, not by testing.

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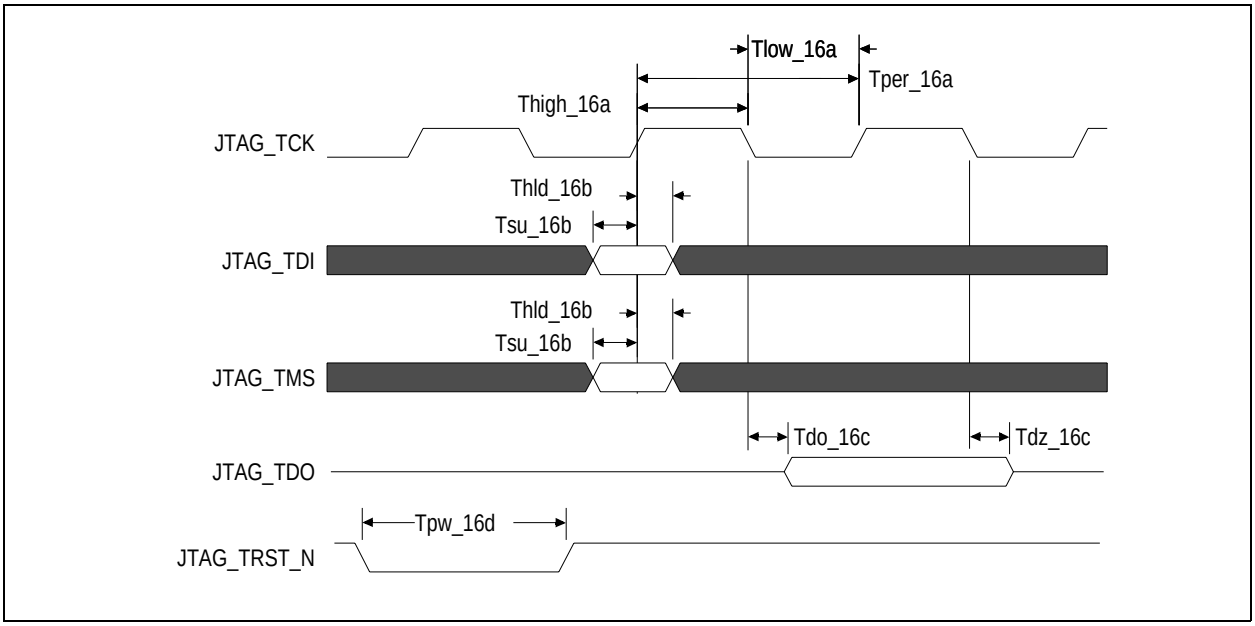


Figure 4 JTAG AC Timing Waveform

Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}CORE	Internal logic supply	0.9	1.0	1.1	V
V_{DD}I/O	I/O supply except for SerDes LVPECL/CML	3.135	3.3	3.465	V
V_{DD}PE	PCI Express Digital Power	0.9	1.0	1.1	V
V_{DD}APE	PCI Express Analog Power	0.9	1.0	1.1	V
V_{TT}PE	PCI Express Serial Data Transmit Termination Voltage	1.425	1.5	1.575	V
V_{SS}	Common ground	0	0	0	V

Table 12 PES24N3 Operating Voltages

Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient

Table 13 PES24N3 Operating Temperatures

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Power-Up Sequence

This section describes the sequence in which various voltages must be applied to the part during power-up to ensure proper functionality. For the PES24N3, the power-up sequence must be as follows:

1. V_{DD}I/O — 3.3V
2. V_{DD}Core, V_{DD}PE, V_{DD}APE — 1.0V
3. V_{TT}PE — 1.5V

When powering up, each voltage level must ramp and stabilize prior to applying the next voltage in the sequence to ensure internal latch-up issues are avoided. There are no maximum time limitations in ramping to valid power levels. The power-down sequence must be in the reverse order of the power-up sequence.

Power Consumption

Typical power is measured under the following conditions: 25°C Ambient, 35% total link usage on all ports, typical voltages defined in Table 14.

Maximum power is measured under the following conditions: 70°C Ambient, 85% total link usage on all ports, maximum voltages defined in Table 14.

All power measurements assume that the part is mounted on a 10 layer printed circuit board with 0 LFM airflow.

Number of Connected Lanes: Port-A/Port-B/Port-C	Core (Watts) (1.0V supply)		PCIe Digital (Watts) (1.0V supply)		PCIe Analog (Watts) (1.0V supply)		PCIe Termination (Watts) (1.5V supply)		I/O (Watts) (3.3V supply)		Total (Watts)	
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max
8/4/4	0.59	0.84	0.75	1.08	0.33	0.42	0.62	0.78	0.002	0.01	2.3	3.12
8/8/8	0.68	0.95	0.98	1.43	0.38	0.48	0.88	1.01	0.002	0.01	2.92	3.88

Table 14 PES24N3 Power Consumption

DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 12.

Note: See Table 7, Pin Characteristics, for a complete I/O listing.

I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Serial Link	PCIe Transmit						
	$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	800		1200	mV	
	$V_{TX-DE-RATIO}$	De-emphasized differential output voltage	-3		-4	dB	
	$V_{TX-DC-CM}$	DC Common mode voltage	-0.1	1	3.7	V	
	$V_{TX-CM-ACP}$	RMS AC peak common mode output voltage			20	mV	
	$V_{TX-CM-DC-active-idle-delta}$	Abs delta of DC common mode voltage between L0 and idle			100	mV	
	$V_{TX-CM-DC-line-delta}$	Abs delta of DC common mode voltage between D+ and D-			25	mV	
	$V_{TX-Idle-DiffP}$	Electrical idle diff peak output			20	mV	

Table 15 DC Electrical Characteristics (Part 1 of 3)

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I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Serial Link (cont.)	$V_{TX-RCV-Detect}$	Voltage change during receiver detection			600	mV	
	$RL_{TX-DIFF}$	Transmitter Differential Return loss	12			dB	
	RL_{TX-CM}	Transmitter Common Mode Return loss	6			dB	
	$Z_{TX-DEFF-DC}$	DC Differential TX impedance	80	100	120	Ω	
	Z_{OSE}	Single ended TX Impedance	40	50	60	Ω	
	Transmitter Eye Diagram	TX Eye Height (De-emphasized bits)	505	650		mV	
	Transmitter Eye Diagram	TX Eye Height (Transition bits)	800	950		mV	
	PCIe Receive						
	$V_{RX-DIFFp-p}$	Differential input voltage (peak-to-peak)	175		1200	mV	
	$V_{RX-CM-AC}$	Receiver common-mode voltage for AC coupling			150	mV	
	$RL_{RX-DIFF}$	Receiver Differential Return Loss	15			dB	
	RL_{RX-CM}	Receiver Common Mode Return Loss	6			dB	
	$Z_{RX-DIFF-DC}$	Differential input impedance (DC)	80	100	120	Ω	
	$Z_{RX-COMM-DC}$	Single-ended input impedance	40	50	60	Ω	
	$Z_{RX-COMM-HIGH-Z-DC}$	Powered down input common mode impedance (DC)	200k	350k		Ω	
	$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65		175	mV	
PCIe REFCLK							
	C_{IN}	Input Capacitance	1.5	—		pF	
Other I/Os							
LOW Drive Output	I_{OL}		—	2.5	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-5.5	—	mA	V_{OH} = 1.5V
High Drive Output	I_{OL}		—	12.0	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-20.0	—	mA	V_{OH} = 1.5V
Schmitt Trigger Input (STI)	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	$V_{DD}IO$ + 0.5	V	—
Input	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	$V_{DD}IO$ + 0.5	V	—
Capacitance	C_{IN}		—	—	8.5	pF	—

Table 15 DC Electrical Characteristics (Part 2 of 3)

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I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Leakage	Inputs		—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ W/O}$ Pull-ups/downs		—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ WITH}$ Pull-ups/downs		—	—	± 80	µA	V_{DD}I/O (max)

Table 15 DC Electrical Characteristics (Part 3 of 3)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.0a.

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Package Pinout — 420-BGA Signal Pinout for PES24N3

The following table lists the pin numbers and signal names for the PES24N3 device.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	V_{SS}		B9	MSMBDAT		C17	$V_{DD}IO$		D25	V_{SS}	
A2	V_{SS}		B10	SSMBADDR_2		C18	V_{SS}		D26	PEREFCLKN2	
A3	V_{SS}		B11	SSMBADDR_5		C19	$V_{DD}IO$		E1	V_{SS}	
A4	JTAG_TDI		B12	SSMBDAT		C20	V_{SS}		E2	V_{SS}	
A5	JTAG_TMS		B13	PEALREV		C21	$V_{DD}IO$		E3	V_{SS}	
A6	MSMBADDR_1		B14	SWMODE_0		C22	V_{SS}		E4	V_{SS}	
A7	MSMBADDR_3		B15	SWMODE_2		C23	$V_{DD}IO$		E5	V_{SS}	
A8	MSMBCLK		B16	PECLREV		C24	V_{SS}		E6	$V_{DD}CORE$	
A9	SSMBADDR_1		B17	$V_{DD}IO$		C25	V_{SS}		E7	$V_{DD}CORE$	
A10	SSMBADDR_3		B18	GPIO_00		C26	PEREFCLKP2		E8	V_{SS}	
A11	SSMBCLK		B19	GPIO_02	1	D1	PEREFCLKP1		E9	$V_{DD}CORE$	
A12	CCLKUS		B20	GPIO_04	1	D2	V_{SS}		E10	V_{SS}	
A13	CCLKDS		B21	GPIO_06		D3	V_{SS}		E11	$V_{DD}CORE$	
A14	PEBLREV		B22	MSMBSMODE		D4	V_{SS}		E12	V_{SS}	
A15	SWMODE_1		B23	REFCLKM		D5	$V_{DD}CORE$		E13	$V_{DD}CORE$	
A16	SWMODE_3		B24	$V_{DD}IO$		D6	$V_{DD}CORE$		E14	V_{SS}	
A17	PERSTN		B25	V_{SS}		D7	V_{SS}		E15	$V_{DD}CORE$	
A18	RSTHALT		B26	V_{SS}		D8	$V_{DD}CORE$		E16	V_{SS}	
A19	GPIO_01		C1	PEREFCLKN1		D9	V_{SS}		E17	$V_{DD}CORE$	
A20	GPIO_03	1	C2	V_{SS}		D10	$V_{DD}CORE$		E18	V_{SS}	
A21	GPIO_05	1	C3	V_{SS}		D11	V_{SS}		E19	$V_{DD}CORE$	
A22	GPIO_07		C4	$V_{DD}CORE$		D12	$V_{DD}CORE$		E20	$V_{DD}CORE$	
A23	TSTRSVD		C5	$V_{DD}IO$		D13	$V_{DD}CORE$		E21	$V_{DD}CORE$	
A24	V_{SS}		C6	V_{SS}		D14	V_{SS}		E22	V_{SS}	
A25	V_{SS}		C7	$V_{DD}IO$		D15	$V_{DD}CORE$		E23	V_{SS}	
A26	V_{SS}		C8	V_{SS}		D16	V_{SS}		E24	V_{SS}	
B1	V_{SS}		C9	$V_{DD}IO$		D17	$V_{DD}CORE$		E25	V_{SS}	
B2	V_{SS}		C10	V_{SS}		D18	$V_{DD}CORE$		E26	V_{SS}	
B3	$V_{DD}IO$		C11	$V_{DD}IO$		D19	$V_{DD}CORE$		F1	$V_{DD}CORE$	
B4	JTAG_TCK		C12	V_{SS}		D20	V_{SS}		F2	$V_{DD}CORE$	
B5	JTAG-TDO		C13	$V_{DD}IO$		D21	$V_{DD}CORE$		F3	$V_{DD}APE$	
B6	JTAG-TRST_N		C14	$V_{DD}CORE$		D22	$V_{DD}CORE$		F4	V_{SS}	
B7	MSMBADDR_2		C15	$V_{DD}IO$		D23	V_{SS}		F5	V_{SS}	
B8	MSMBADDR_4		C16	$V_{DD}CORE$		D24	V_{SS}		F22	V_{SS}	

Table 16 PES24N3 420-pin Signal Pin-Out (Part 1 of 3)

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Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
F23	V_{SS}		K4	V_{DD}APE		P1	V_{DD}CORE		U24	V_{DD}PE	
F24	V_{DD}APE		K5	V_{DD}APE		P2	V_{SS}		U25	PECTP05	
F25	V_{DD}CORE		K22	V_{DD}APE		P3	V_{TT}PE		U26	PECTN05	
F26	V_{DD}CORE		K23	V_{DD}APE		P4	V_{TT}PE		V1	V_{DD}CORE	
G1	PEBTN07		K24	V_{DD}APE		P5	V_{SS}		V2	V_{SS}	
G2	PEBTP07		K25	V_{SS}		P22	V_{SS}		V3	V_{DD}APE	
G3	V_{DD}PE		K26	V_{SS}		P23	V_{TT}PE		V4	V_{DD}APE	
G4	PEBRN07		L1	PEBTN05		P24	V_{TT}PE		V5	V_{DD}APE	
G5	PEBRP07		L2	PEBTP05		P25	V_{SS}		V22	V_{DD}APE	
G22	PECRP00		L3	V_{DD}PE		P26	V_{DD}CORE		V23	V_{DD}APE	
G23	PECRN00		L4	PEBRN05		R1	PEBTN03		V24	V_{DD}APE	
G24	V_{DD}PE		L5	PEBRP05		R2	PEBTP03		V25	V_{SS}	
G25	PECTP00		L22	PECRP02		R3	V_{DD}PE		V26	V_{DD}CORE	
G26	PECTN00		L23	PECRN02		R4	PEBRN03		W1	PEBTN01	
H1	V_{SS}		L24	V_{DD}PE		R5	PEBRP03		W2	PEBTP01	
H2	V_{SS}		L25	PECTP02		R22	PECRP04		W3	V_{DD}PE	
H3	V_{TT}PE		L26	PECTN02		R23	PECRN04		W4	PEBRN01	
H4	V_{TT}PE		M1	V_{DD}CORE		R24	V_{DD}PE		W5	PEBRP01	
H5	V_{SS}		M2	V_{SS}		R25	PECTP04		W22	PECRP06	
H22	V_{SS}		M3	V_{TT}PE		R26	PECTN04		W23	PECRN06	
H23	V_{TT}PE		M4	V_{TT}PE		T1	V_{DD}CORE		W24	V_{DD}PE	
H24	V_{TT}PE		M5	V_{SS}		T2	V_{SS}		W25	PECTP06	
H25	V_{SS}		M22	V_{SS}		T3	V_{DD}APE		W26	PECTN06	
H26	V_{SS}		M23	V_{TT}PE		T4	V_{DD}APE		Y1	V_{SS}	
J1	PEBTN06		M24	V_{TT}PE		T5	V_{SS}		Y2	V_{SS}	
J2	PEBTP06		M25	V_{SS}		T22	V_{SS}		Y3	V_{TT}PE	
J3	V_{DD}PE		M26	V_{DD}CORE		T23	V_{DD}APE		Y4	V_{TT}PE	
J4	PEBRN06		N1	PEBTN04		T24	V_{DD}APE		Y5	V_{SS}	
J5	PEBRP06		N2	PEBTP04		T25	V_{SS}		Y22	V_{SS}	
J22	PECRP01		N3	V_{DD}PE		T26	V_{DD}CORE		Y23	V_{TT}PE	
J23	PECRN01		N4	PEBRN04		U1	PEBTN02		Y24	V_{TT}PE	
J24	V_{DD}PE		N5	PEBRP04		U2	PEBTP02		Y25	V_{SS}	
J25	PECTP01		N22	PECRP03		U3	V_{DD}PE		Y26	V_{SS}	
J26	PECTN01		N23	PECRN03		U4	PEBRN02		AA1	PEBTN00	
K1	V_{SS}		N24	V_{DD}PE		U5	PEBRP02		AA2	PEBTP00	
K2	V_{SS}		N25	PECTP03		U22	PECRP05		AA3	V_{DD}PE	
K3	V_{DD}APE		N26	PECTN03		U23	PECRN05		AA4	PEBRN00	

Table 16 PES24N3 420-pin Signal Pin-Out (Part 2 of 3)

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Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
AA5	PEBRP00		AC3	V_{DD}CORE		AD11	V_{DD}PE		AE19	PEATP01	
AA22	PECRP07		AC4	V_{DD}CORE		AD12	V_{TT}PE		AE20	V_{SS}	
AA23	PECRN07		AC5	V_{DD}CORE		AD13	V_{DD}PE		AE21	PEATP00	
AA24	V_{DD}PE		AC6	V_{TT}PE		AD14	V_{TT}PE		AE22	V_{SS}	
AA25	PECTP07		AC7	PEARN07		AD15	V_{DD}PE		AE23	V_{DD}CORE	
AA26	PECTN07		AC8	V_{DD}APE		AD16	V_{DD}APE		AE24	V_{DD}CORE	
AB1	V_{SS}		AC9	PEARN06		AD17	V_{SS}		AE25	V_{SS}	
AB2	V_{SS}		AC10	V_{DD}APE		AD18	V_{DD}PE		AE26	V_{SS}	
AB3	V_{DD}CORE		AC11	PEARN05		AD19	V_{DD}PE		AF1	V_{SS}	
AB4	V_{DD}CORE		AC12	V_{TT}PE		AD20	V_{TT}PE		AF2	V_{SS}	
AB5	V_{DD}CORE		AC13	PEARN04		AD21	V_{DD}PE		AF3	V_{DD}CORE	
AB6	V_{SS}		AC14	V_{TT}PE		AD22	V_{SS}		AF4	V_{DD}CORE	
AB7	PEARP07		AC15	PEARN03		AD23	V_{DD}CORE		AF5	V_{DD}CORE	
AB8	V_{SS}		AC16	V_{DD}APE		AD24	V_{DD}CORE		AF6	V_{SS}	
AB9	PEARP06		AC17	PEARN02		AD25	V_{SS}		AF7	PEATN07	
AB10	V_{DD}APE		AC18	V_{DD}APE		AD26	V_{SS}		AF8	V_{SS}	
AB11	PEARP05		AC19	PEARN01		AE1	V_{SS}		AF9	PEATN06	
AB12	V_{SS}		AC20	V_{TT}PE		AE2	V_{SS}		AF10	V_{DD}CORE	
AB13	PEARP04		AC21	PEARN00		AE3	V_{DD}CORE		AF11	PEATN05	
AB14	V_{DD}APE		AC22	V_{SS}		AE4	V_{DD}CORE		AF12	V_{DD}CORE	
AB15	PEARP03		AC23	V_{DD}CORE		AE5	V_{SS}		AF13	PEATN04	
AB16	V_{SS}		AC24	V_{DD}CORE		AE6	V_{SS}		AF14	V_{DD}CORE	
AB17	PEARP02		AC25	V_{SS}		AE7	PEATP07		AF15	PEATN03	
AB18	V_{DD}APE		AC26	V_{SS}		AE8	V_{SS}		AF16	V_{DD}CORE	
AB19	PEARP01		AD1	V_{SS}		AE9	PEATP06		AF17	PEATN02	
AB20	V_{SS}		AD2	V_{SS}		AE10	V_{SS}		AF18	V_{SS}	
AB21	PEARP00		AD3	V_{DD}CORE		AE11	PEATP05		AF19	PEATN01	
AB22	V_{SS}		AD4	V_{DD}CORE		AE12	V_{SS}		AF20	V_{SS}	
AB23	V_{DD}CORE		AD5	V_{DD}CORE		AE13	PEATP04		AF21	PEATN00	
AB24	V_{DD}CORE		AD6	V_{TT}PE		AE14	V_{SS}		AF22	V_{SS}	
AB25	V_{SS}		AD7	V_{SS}		AE15	PEATP03		AF23	V_{DD}CORE	
AB26	V_{SS}		AD8	V_{DD}PE		AE16	V_{SS}		AF24	V_{DD}CORE	
AC1	V_{SS}		AD9	V_{SS}		AE17	PEATP02		AF25	V_{SS}	
AC2	V_{SS}		AD10	V_{DD}PE		AE18	V_{SS}		AF26	V_{SS}	

Table 16 PES24N3 420-pin Signal Pin-Out (Part 3 of 3)

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Power Pins

V_{DD}Core	V_{DD}Core	V_{DD}Core	V_{DD}IO	V_{DD}PE	V_{DD}APE	V_{TT}PE
C4	F2	AE3	B3	G3	F3	H3
C14	F25	AE4	B17	G24	F24	H4
C16	F26	AE23	B24	J3	K3	H23
D5	M1	AE24	C5	J24	K4	H24
D6	M26	AF3	C7	L3	K5	M3
D8	P1	AF4	C9	L24	K22	M4
D10	P26	AF5	C11	N3	K23	M23
D12	T1	AF10	C13	N24	K24	M24
D13	T26	AF12	C15	R3	T3	P3
D15	V1	AF14	C17	R24	T4	P4
D17	V26	AF16	C19	U3	T23	P23
D18	AB3	AF23	C21	U24	T24	P24
D19	AB4	AF24	C23	W3	V3	Y3
D21	AB5			W24	V4	Y4
D22	AB23			AA3	V5	Y23
E6	AB24			AA24	V22	Y24
E7	AC3			AD8	V23	AC6
E9	AC4			AD10	V24	AC12
E11	AC5			AD11	AB10	AC14
E13	AC23			AD13	AB14	AC20
E15	AC24			AD15	AB18	AD6
E17	AD3			AD18	AC8	AD12
E19	AD4			AD19	AC10	AD14
E20	AD5			AD21	AC16	AD20
E21	AD23				AC18	
F1	AD24				AD16	

Table 17 PES24N3 Power Pins

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Ground Pins

V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
A1	D11	F23	Y2	AD25
A2	D14	H1	Y5	AD26
A3	D16	H2	Y22	AE1
A24	D20	H5	Y25	AE2
A25	D23	H22	Y26	AE5
A26	D24	H25	AB1	AE6
B1	D25	H26	AB2	AE8
B2	E1	K1	AB6	AE10
B25	E2	K2	AB8	AE12
B26	E3	K25	AB12	AE14
C2	E4	K26	AB16	AE16
C3	E5	M2	AB20	AE18
C6	E8	M5	AB22	AE20
C8	E10	M22	AB25	AE22
C10	E12	M25	AB26	AE25
C12	E14	P2	AC1	AE26
C18	E16	P5	AC2	AF1
C20	E18	P22	AC22	AF2
C22	E22	P25	AC25	AF6
C24	E23	T2	AC26	AF8
C25	E24	T5	AD1	AF18
D2	E25	T22	AD2	AF20
D3	E26	T25	AD7	AF22
D4	F4	V2	AD9	AF25
D7	F5	V25	AD17	AF26
D9	F22	Y1	AD22	—

Table 18 PES24N3 Ground Pins

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Alternate Signal Functions

Pin	GPIO	Alternate
B19	GPIO[2]	IOEXPINTN
A20	GPIO[3]	PAABN
B20	GPIO[4]	PAAIN
A21	GPIO[5]	PAPIN

Table 19 PES24N3 Alternate Signal Functions

Signals Listed Alphabetically

Signal Name	I/O Type	Location	Signal Category
CCLKDS	I	A13	System
CCLKUS	I	A12	
GPIO_00	I/O	B18	General Purpose Input/Output
GPIO_01	I/O	A19	
GPIO_02	I/O	B19	
GPIO_03	I/O	A20	
GPIO_04	I/O	B20	
GPIO_05	I/O	A21	
GPIO_06	I/O	B21	
GPIO_07	I/O	A22	
JTAG_TCK	I	B4	JTAG
JTAG_TDI	I	A4	
JTAG_TMS	I	A5	
JTAG-TDO	O	B5	
JTAG-TRST_N	I	B6	
MSMBADDR_1	I	A6	SMBus
MSMBADDR_2	I	B7	
MSMBADDR_3	I	A7	
MSMBADDR_4	I	B8	
MSMBCLK	I/O	A8	
MSMBDAT	I/O	B9	
MSMBSMODE	I	B22	System

Table 20 89PES24N3 Alphabetical Signal List (Part 1 of 5)

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Signal Name	I/O Type	Location	Signal Category
PEALREV	I	B13	PCI Express
PEARN00	I	AC21	
PEARN01	I	AC19	
PEARN02	I	AC17	
PEARN03	I	AC15	
PEARN04	I	AC13	
PEARN05	I	AC11	
PEARN06	I	AC9	
PEARN07	I	AC7	
PEARP00	I	AB21	
PEARP01	I	AB19	
PEARP02	I	AB17	
PEARP03	I	AB15	
PEARP04	I	AB13	
PEARP05	I	AB11	
PEARP06	I	AB9	
PEARP07	I	AB7	
PEATN00	O	AF21	
PEATN01	O	AF19	
PEATN02	O	AF17	
PEATN03	O	AF15	
PEATN04	O	AF13	
PEATN05	O	AF11	
PEATN06	O	AF9	
PEATN07	O	AF7	
PEATP00	O	AE21	
PEATP01	O	AE19	
PEATP02	O	AE17	
PEATP03	O	AE15	
PEATP04	O	AE13	
PEATP05	O	AE11	
PEATP06	O	AE9	
PEATP07	O	AE7	
PEBLREV	I	A14	
PEBRN00	I	AA4	
PEBRN01	I	W4	

Table 20 89PES24N3 Alphabetical Signal List (Part 2 of 5)

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Signal Name	I/O Type	Location	Signal Category
PEBRN02	I	U4	PCI Express
PEBRN03	I	R4	
PEBRN04	I	N4	
PEBRN05	I	L4	
PEBRN06	I	J4	
PEBRN07	I	G4	
PEBRP00	I	AA5	
PEBRP01	I	W5	
PEBRP02	I	U5	
PEBRP03	I	R5	
PEBRP04	I	N5	
PEBRP05	I	L5	
PEBRP06	I	J5	
PEBRP07	I	G5	
PEBTN00	O	AA1	
PEBTN01	O	W1	
PEBTN02	O	U1	
PEBTN03	O	R1	
PEBTN04	O	N1	
PEBTN05	O	L1	
PEBTN06	O	J1	
PEBTN07	O	G1	
PEBTP00	O	AA2	
PEBTP01	O	W2	
PEBTP02	O	U2	
PEBTP03	O	R2	
PEBTP04	O	N2	
PEBTP05	O	L2	
PEBTP06	O	J2	
PEBTP07	O	G2	
PECLREV	I	B16	
PECRN00	I	G23	
PECRN01	I	J23	
PECRN02	I	L23	
PECRN03	I	N23	
PECRN04	I	R23	

Table 20 89PES24N3 Alphabetical Signal List (Part 3 of 5)

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Signal Name	I/O Type	Location	Signal Category
PECRN05	I	U23	PCI Express
PECRN06	I	W23	
PECRN07	I	AA23	
PECRP00	I	G22	
PECRP01	I	J22	
PECRP02	I	L22	
PECRP03	I	N22	
PECRP04	I	R22	
PECRP05	I	U22	
PECRP06	I	W22	
PECRP07	I	AA22	
PECTN00	O	G26	
PECTN01	O	J26	
PECTN02	O	L26	
PECTN03	O	N26	
PECTN04	O	R26	
PECTN05	O	U26	
PECTN06	O	W26	
PECTN07	O	AA26	
PECTP00	O	G25	
PECTP01	O	J25	
PECTP02	O	L25	
PECTP03	O	N25	
PECTP04	O	R25	
PECTP05	O	U25	
PECTP06	O	W25	
PECTP07	O	AA25	
PEREFCLKN1	I	C1	
PEREFCLKN2	I	D26	
PEREFCLKP1	I	D1	
PEREFCLKP2	I	C26	
PERSTN	I	A17	System
REFCLKM	I	B23	PCI Express
RSTHALT	I	A18	System

Table 20 89PES24N3 Alphabetical Signal List (Part 4 of 5)

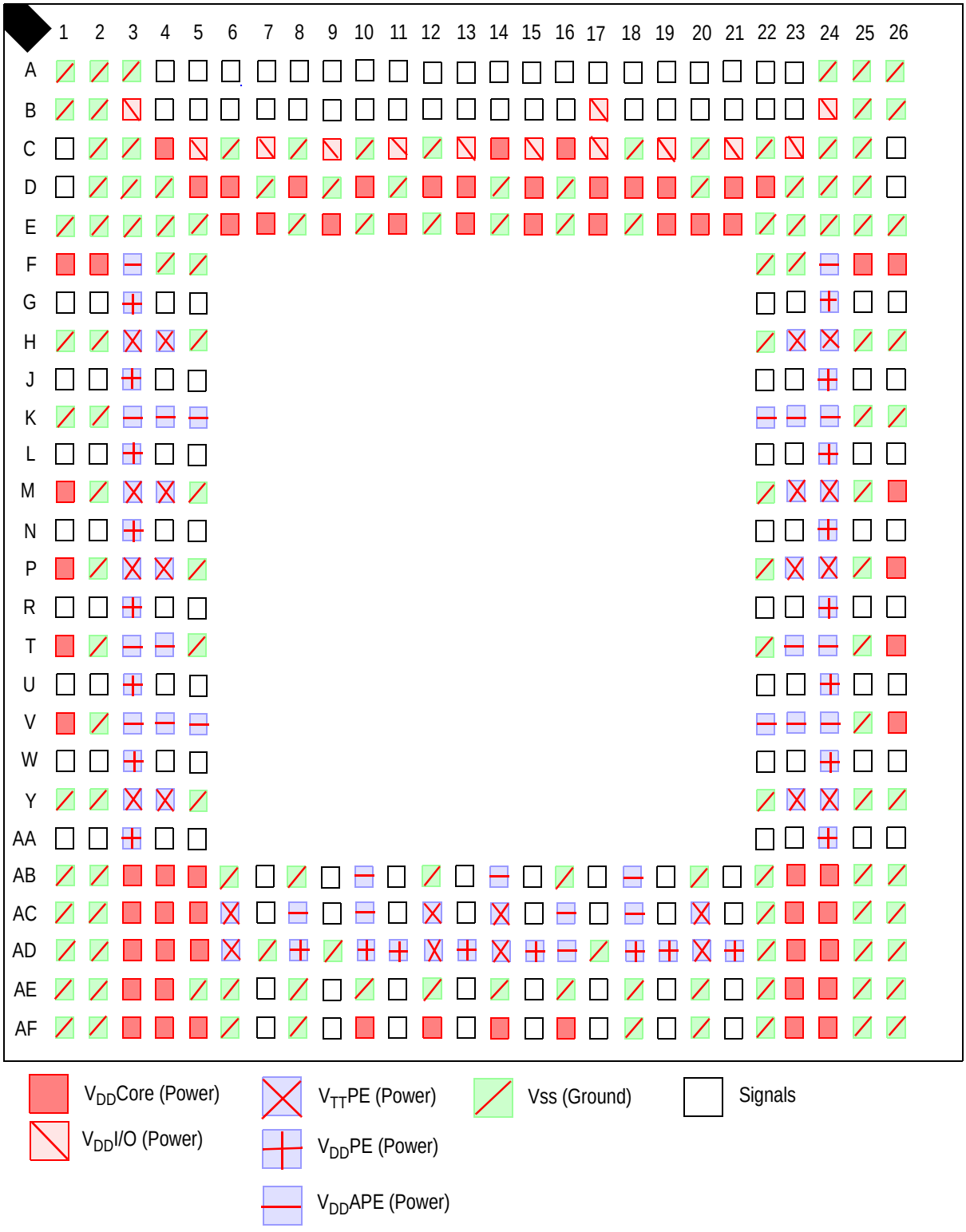
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Signal Name	I/O Type	Location	Signal Category
SSMBADDR_1	I	A9	SMBus
SSMBADDR_2	I	B10	
SSMBADDR_3	I	A10	
SSMBADDR_5	I	B11	
TSTRSVD	I	A23	System
SSMBCLK	I/O	A11	SMBus
SSMBDAT	I/O	B12	
SWMODE_0	I	B14	System
SWMODE_1	I	A15	
SWMODE_2	I	B15	
SWMODE_3	I	A16	System
V_{DD}CORE, V_{DD}APE, V_{DD}IO, V_{DD}PE, V_{TT}PE	See Table 17 for a listing of power pins.		
V_{SS}	See Table 18 for a listing of ground pins.		

Table 20 89PES24N3 Alphabetical Signal List (Part 5 of 5)

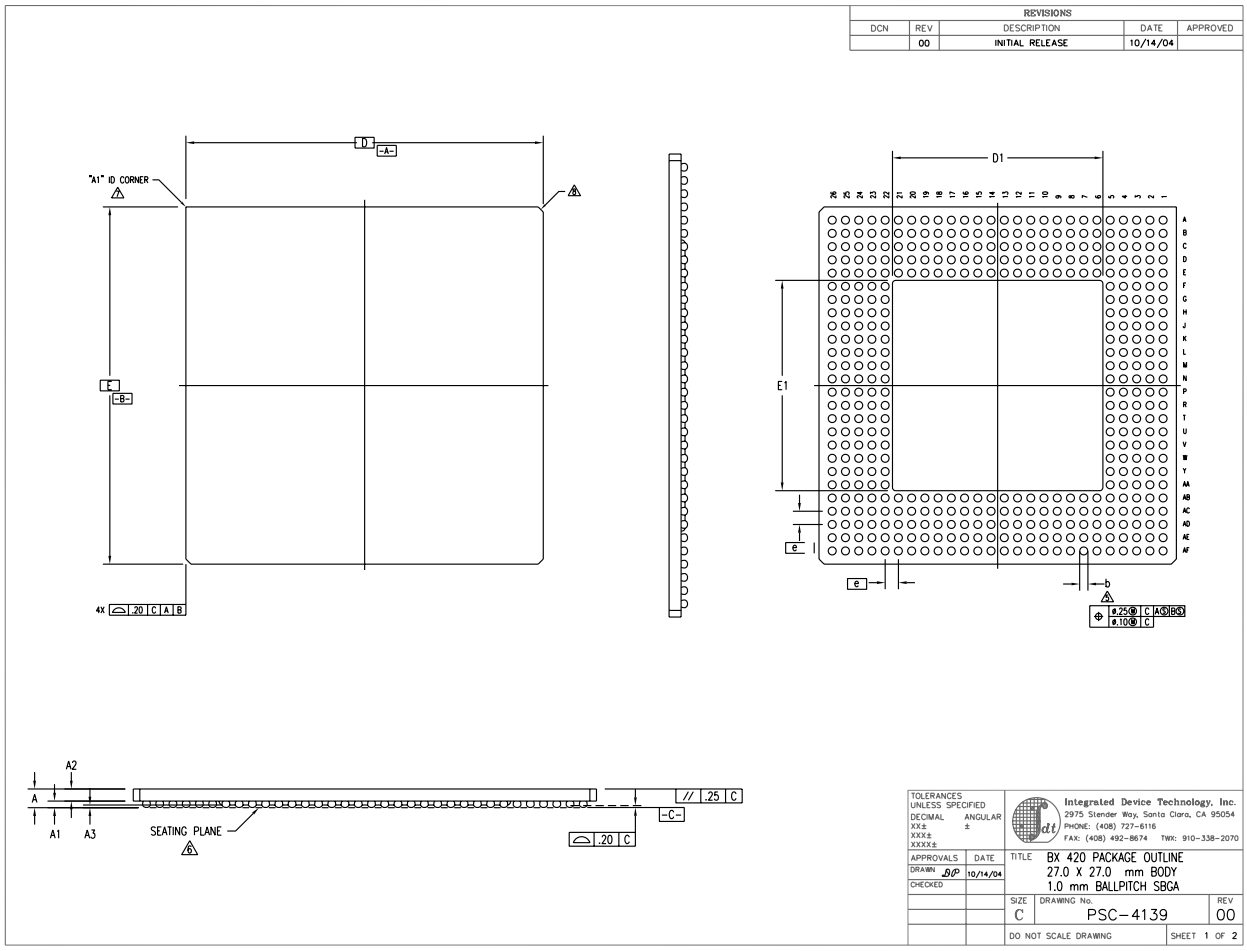
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PES24N3 Pinout — Top View



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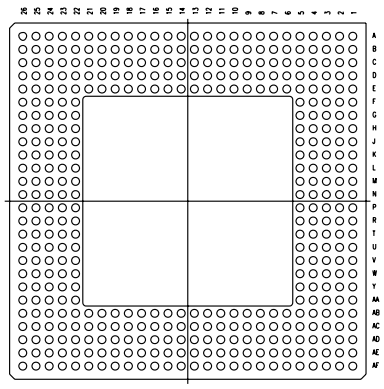
PES24N3 Package Drawing — 420-Pin BX420/BXG420



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PES24N3 Package Drawing — Page Two

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	10/14/04	



SYMBOL	JEDEC VARIATION NONE			NOTE
	MIN	NOM	MAX	
A	–	–	1.70	
A1	.30	–	–	
A2	.25	–	1.10	
A3	.15	–	–	
D	27.00 BSC			
D1	–	–	15.9	
E	27.00 BSC			
E1	–	–	15.9	
M	26 (DEPOPULATED)			3
N	420			4
e	1.00 BSC			
b	.50	.60	.70	5
CENTER BALL MATRIX	N/A			

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH
3. "M" REPRESENTS THE MAXIMUM SOLDER BALL MATRIX SIZE
4. "N" REPRESENTS THE BALLCOUNT NUMBER
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -C-
6. SEATING PLANE AND PRIMARY DATUM -C- ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS
7. "A1" ID CORNER MUST BE IDENTIFIED BY CHAMFER, INK MARK, METALLIZED MARKING, INDENTATION OR OTHER FEATURE ON PACKAGE BODY
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. ALL DIMENSIONS ARE IN MILLIMETERS

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

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APPROVALS	DATE
DRAWN BJP	10/14/04
CHECKED	

TITLE: BX 420 PACKAGE OUTLINE
27.0 X 27.0 mm BODY
1.0 mm BALLPITCH SBGA

SIZE: C | DRAWING No.: PSC-4139 | REV: 00

DO NOT SCALE DRAWING | SHEET 2 OF 2

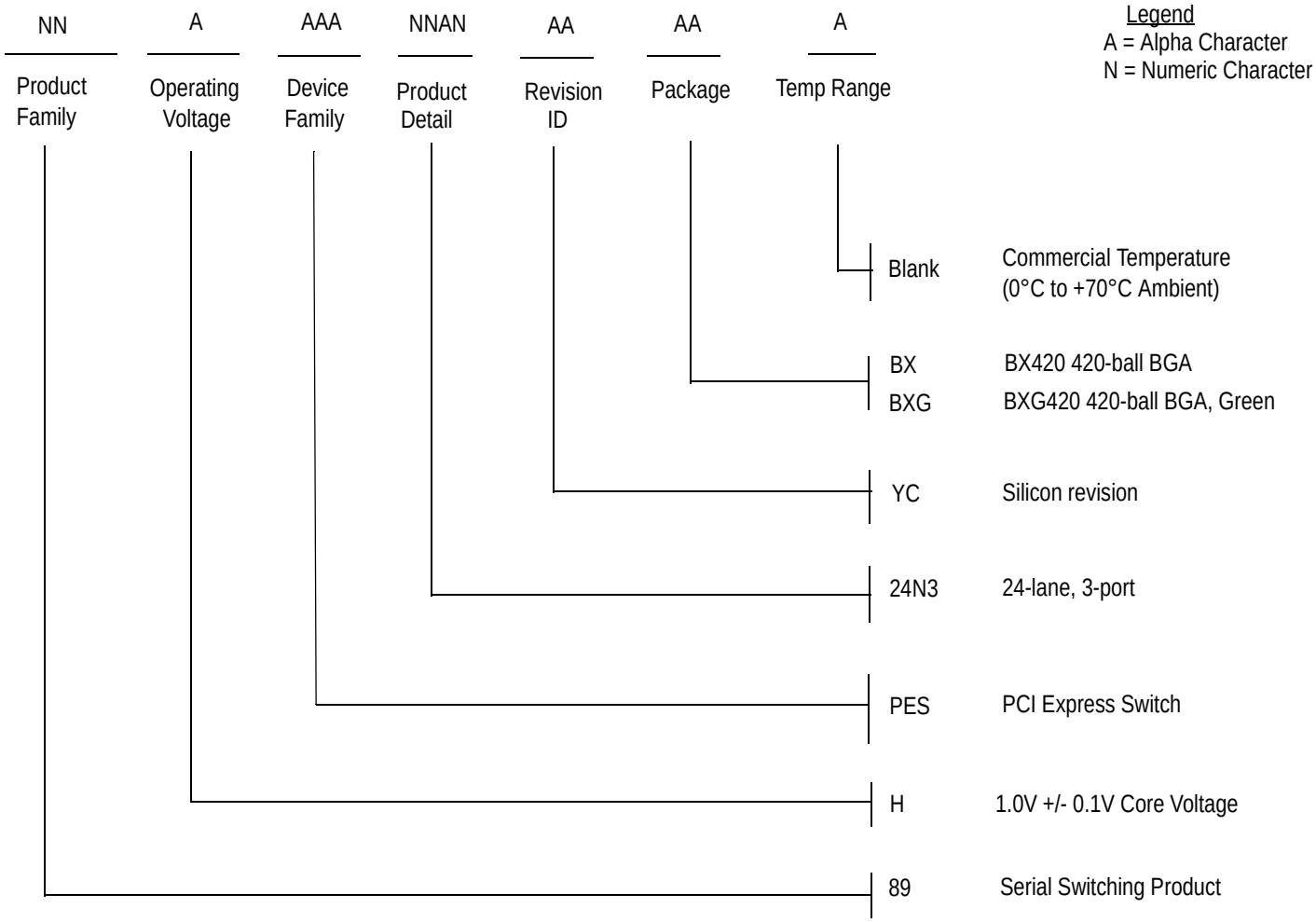
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Revision History

July 18, 2006: Publication of YC data sheet.

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Ordering Information



Valid Combinations

89HPES24N3YCBX	420-pin BX420 package, Commercial Temperature
89HPES24N3YCBXG	420-pin Green BX420 package, Commercial Temperature

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