

## General Description

The ICS879S216I-02 is a Differential-to-LVPECL/ LVDS Clock Divider which can operate up to 2.5GHz. ICS879S216I-02 has 2 selectable differential clock inputs. The fully differential architecture and low propagation delay make it ideal for use in clock distribution circuits. ICS879S216I-02 can divide the input clock by  $\div 2$ ,  $\div 4$ ,  $\div 8$  and  $\div 16$ . Table 4A lists all the available output dividers.

## Features

- High speed 2:2 differential divider
- Two differential LVPECL or LVDS output pairs
- Four selectable divide combinations
- PCLKx can accept the following input levels: LVPECL, LVDS, CML
- Maximum input frequency: 2.5GHz
- Propagation delay: 0.8ns (minimum), 1.6ns (maximum)
- Output Skew: 25ps (maximum)
- Full 3.3V or 2.5V supply modes
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 5) package

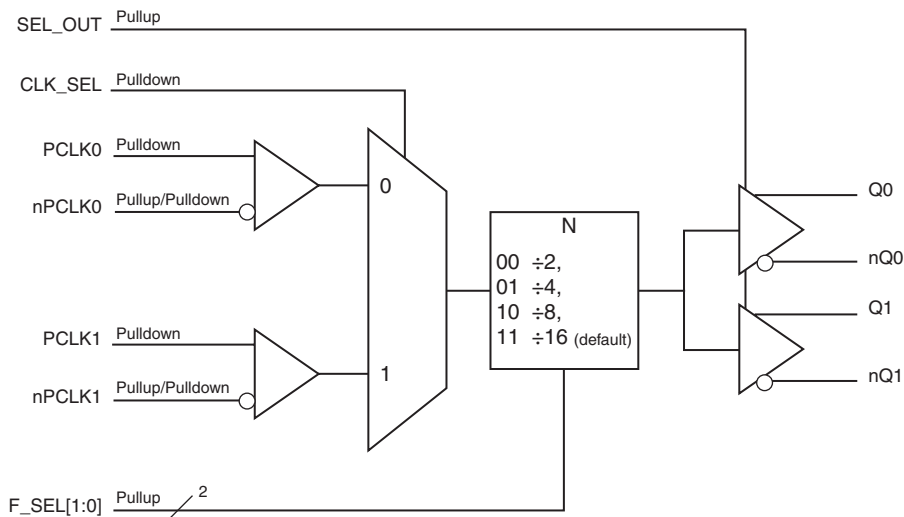
Table 1A. V<sub>CC\_TAP</sub> Function Table

| Outputs         | Output Level Supply | V <sub>CC_TAP</sub> |
|-----------------|---------------------|---------------------|
| Q[1:0], nQ[1:0] |                     |                     |
| LVPECL          | 2.5V                | V <sub>CC</sub>     |
| LVPECL          | 3.3V                | V <sub>CC</sub>     |
| LVDS            | 2.5V                | V <sub>CC</sub>     |
| LVDS            | 3.3V                | Float               |

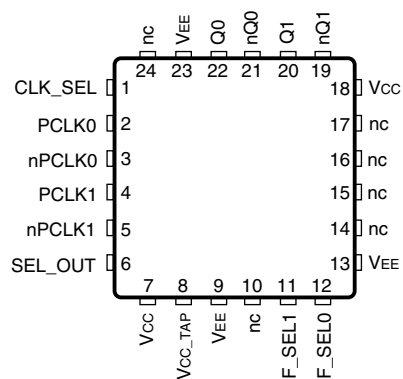
Table 1B. SEL\_OUT Function Table

| Input   | Outputs          |
|---------|------------------|
| SEL_OUT | Q[1:0], nQ[1:0]  |
| 1       | LVPECL (default) |
| 0       | LVDS             |

## Block Diagram



## Pin Assignment



ICS879S216I-02

24-Lead VFQFN

4mm x 4mm x 0.95mm package body  
K Package  
Top View

**Table 2. Pin Descriptions**

| Number                    | Name                | Type   |                     | Description   |
|---------------------------|---------------------|--------|---------------------|---|
| 1                         | CLK_SEL             | Input  | Pulldown            | Clock select input. See Table 4B. LVCMOS/LVTTL interface levels.    |
| 2                         | PCLK0               | Input  | Pulldown            | Non-inverting differential LVPECL clock input.                      |
| 3                         | nPCLK0              | Input  | Pullup/<br>Pulldown | Inverting differential LVPECL clock input.                          |
| 4                         | PCLK1               | Input  | Pulldown            | Non-inverting differential LVPECL clock input.                      |
| 5                         | nPCLK1              | Input  | Pullup/<br>Pulldown | Inverting differential LVPECL clock input.                          |
| 6                         | SEL_OUT             | Input  | Pullup              | Select pin. See Table 1B. LVCMOS/LVTTL interface levels.            |
| 7, 18                     | V <sub>CC</sub>     | Power  |                     | Power supply pins.  |
| 8                         | V <sub>CC_TAP</sub> | Power  |                     | Power supply pin. See Table 1A.                                     |
| 9, 13, 23                 | V <sub>EE</sub>     | Power  |                     | Negative supply pins.   |
| 10, 14, 15,<br>16, 17, 24 | nc                  | Unused |                     | No connect.   |
| 11,<br>12                 | F_SEL1,<br>F_SEL0   | Input  | Pullup              | Clock select inputs. See Table 4A. LVCMOS / LVTTL interface levels. |
| 19, 20                    | nQ1, Q1             | Output |                     | Differential output pair. LVPECL or LVDS interface levels.          |
| 21, 22                    | nQ0, Q0             | Output |                     | Differential output pair. LVPECL or LVDS interface levels.          |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 3. Pin Characteristics**

| Symbol                | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C <sub>IN</sub>       | Input Capacitance       |                 |         | 2       |         | pF    |
| R <sub>PULLUP</sub>   | Input Pullup Resistor   |                 |         | 51      |         | kΩ    |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor |                 |         | 51      |         | kΩ    |

## Function Tables

**Table 4A. Clock Input Function Table**

| Input  |        | Divide       |
|--------|--------|--------------|
| F_SEL1 | F_SEL0 |              |
| 0      | 0      | 2            |
| 0      | 1      | 4            |
| 1      | 0      | 8            |
| 1      | 1      | 16 (default) |

**Table 4B. CLK\_SEL Function Table**

| Inputs  |                         |
|---------|-------------------------|
| CLK_SEL | PCLK[0:1], nPCLK[0:1]   |
| 0       | PCLK0, nPCLK0 (default) |
| 1       | PCLK1, nPCLK1           |

NOTE: CLK\_SEL is an asynchronous control.

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item   | Rating                   |
|--|--------------------------|
| Supply Voltage, $V_{CC}$                                       | 4.6V                     |
| Inputs, $V_I$  | -0.5V to $V_{CC} + 0.5V$ |
| Outputs, $I_O$ (LVPECL)<br>Continuous Current<br>Surge Current | 50mA<br>100mA            |
| Outputs, $I_O$ (LVDS)<br>Continuous Current<br>Surge Current   | 10mA<br>15mA             |
| Package Thermal Impedance, $\theta_{JA}$                       | 49.5°C/W (0 mps)         |
| Storage Temperature, $T_{STG}$                                 | -65°C to 150°C           |

## DC Electrical Characteristics

**Table 5A. LVPECL Power Supply DC Characteristics,  $V_{CC} = V_{CC\_TAP} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

| Symbol        | Parameter            | Test Conditions | Minimum | Typical | Maximum | Units |
|---------------|----------------------|-----------------|---------|---------|---------|-------|
| $V_{CC}$      | Power Supply Voltage |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{CC\_TAP}$ | Power Supply Voltage |                 | 3.135   | 3.3     | 3.465   | V     |
| $I_{EE}$      | Power Supply Current |                 |         |         | 65      | mA    |

**Table 5B. LVPECL Power Supply DC Characteristics,  $V_{CC} = V_{CC\_TAP} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

| Symbol        | Parameter            | Test Conditions | Minimum | Typical | Maximum | Units |
|---------------|----------------------|-----------------|---------|---------|---------|-------|
| $V_{CC}$      | Power Supply Voltage |                 | 2.375   | 2.5     | 2.625   | V     |
| $V_{CC\_TAP}$ | Power Supply Voltage |                 | 2.375   | 2.5     | 2.625   | V     |
| $I_{EE}$      | Power Supply Current |                 |         |         | 60      | mA    |

**Table 5C. LVDS Power Supply DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{CC\_TAP} = \text{Float}$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

| Symbol   | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|-------------------------|-----------------|---------|---------|---------|-------|
| $V_{CC}$ | Positive Supply Voltage |                 | 3.135   | 3.3     | 3.465   | V     |
| $I_{EE}$ | Power Supply Current    |                 |         |         | 95      | mA    |

**Table 5D. LVDS Power Supply DC Characteristics,  $V_{CC} = V_{CC\_TAP} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

| Symbol        | Parameter            | Test Conditions | Minimum | Typical | Maximum | Units |
|---------------|----------------------|-----------------|---------|---------|---------|-------|
| $V_{CC}$      | Power Supply Voltage |                 | 2.375   | 2.5     | 2.625   | V     |
| $V_{CC\_TAP}$ | Power Supply Voltage |                 | 2.375   | 2.5     | 2.625   | V     |
| $I_{EE}$      | Power Supply Current |                 |         |         | 90      | mA    |

**Table 5E. LVCMOS/LVTTL DC Characteristics,  $V_{CC} = V_{CC\_TAP} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

| Symbol   | Parameter          |                     | Test Conditions                               | Minimum | Typical | Maximum        | Units   |
|----------|--------------------|---------------------|---|---------|---------|----------------|---------|
| $V_{IH}$ | Input High Voltage |                     | $V_{CC} = 3.465V$                             | 2.2     |         | $V_{CC} + 0.3$ | V       |
|          |                    |                     | $V_{CC} = 2.625V$                             | 1.7     |         | $V_{CC} + 0.3$ | V       |
| $V_{IL}$ | Input Low Voltage  |                     | $V_{CC} = 3.465V$                             | -0.3    |         | 0.8            | V       |
|          |                    |                     | $V_{CC} = 2.625V$                             | -0.3    |         | 0.7            | V       |
| $I_{IH}$ | Input High Current | CLK_SEL             | $V_{CC} = V_{IN} = 3.465V$ or $2.625V$        |         |         | 150            | $\mu A$ |
|          |                    | F_SEL[1:0], SEL_OUT | $V_{CC} = V_{IN} = 3.465V$ or $2.625V$        |         |         | 10             | $\mu A$ |
| $I_{IL}$ | Input Low Current  | CLK_SEL             | $V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$ | -10     |         |                | $\mu A$ |
|          |                    | F_SEL[1:0], SEL_OUT | $V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$ | -150    |         |                | $\mu A$ |

**Table 5F. LVPECL DC Characteristics,  $V_{CC} = V_{CC\_TAP} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

| Symbol      | Parameter                            |                              | Test Conditions                               | Minimum        | Typical | Maximum         | Units   |
|-------------|--------------------------------------|------------------------------|---|----------------|---------|-----------------|---------|
| $I_{IH}$    | Input High Current                   | PCLK0, nPCLK0, PCLK1, nPCLK1 | $V_{CC} = V_{IN} = 3.465V$ or $2.625V$        |                |         | 150             | $\mu A$ |
| $I_{IL}$    | Input Low Current                    | PCLK0, PCLK1                 | $V_{CC} = 3.465V$ or $2.625V$                 | -10            |         |                 | $\mu A$ |
|             |                                      | nPCLK0, nPCLK1               | $V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$ | -150           |         |                 | $\mu A$ |
| $V_{PP}$    | Peak-to-Peak Voltage; NOTE 1         |                              |   | 0.15           |         | 1.3             | V       |
| $V_{CMR}$   | Common Mode Input Voltage; NOTE 1, 2 |                              |   | $V_{EE} + 0.5$ |         | $V_{CC} - 0.85$ | V       |
| $V_{OH}$    | Output High Voltage; NOTE 3          |                              |   | $V_{CC} - 1.4$ |         | $V_{CC} - 0.8$  | V       |
| $V_{OL}$    | Output Low Voltage; NOTE 3           |                              |   | $V_{CC} - 2.0$ |         | $V_{CC} - 1.6$  | V       |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing    |                              |   | 0.6            |         | 1.0             | V       |

NOTE 1:  $V_{IL}$  should not be less than -0.3V.

NOTE 2: Common mode input voltage is defined as  $V_{IH}$ .

NOTE 3: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

**Table 5G. LVDS DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{CC\_TAP} = \text{Float}$ ,  $V_{EE} = 0V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

| Symbol          | Parameter                   | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|-----------------------------|-----------------|---------|---------|---------|-------|
| $V_{OD}$        | Differential Output Voltage | SEL_OUT = 0     | 247     |         | 454     | mV    |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change   | SEL_OUT = 0     |         |         | 50      | mV    |
| $V_{OS}$        | Offset Voltage              | SEL_OUT = 0     | 1.125   |         | 1.375   | V     |
| $\Delta V_{OS}$ | $V_{OS}$ Magnitude Change   | SEL_OUT = 0     |         |         | 50      | mV    |

**Table 5H. LVDS DC Characteristics,  $V_{CC} = V_{CC\_TAP} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

| Symbol          | Parameter                   | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|-----------------------------|-----------------|---------|---------|---------|-------|
| $V_{OD}$        | Differential Output Voltage | SEL_OUT = 0     | 247     |         | 454     | mV    |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change   | SEL_OUT = 0     |         |         | 50      | mV    |
| $V_{OS}$        | Offset Voltage              | SEL_OUT = 0     | 1.1     |         | 1.375   | V     |
| $\Delta V_{OS}$ | $V_{OS}$ Magnitude Change   | SEL_OUT = 0     |         |         | 50      | mV    |

## AC Electrical Characteristics

**Table 6A. LVPECL AC Characteristics**,  $V_{CC} = V_{CC\_TAP} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$ 

| Symbol            | Parameter                              | Test Conditions    | Minimum | Typical | Maximum | Units |
|-------------------|--|--------------------|---------|---------|---------|-------|
| $f_{IN}$          | Input Frequency                        |                    |         |         | 2.5     | GHz   |
| $f_{OUT}$         | Output Frequency                       | $F\_SEL[1:0] = 00$ |         |         | 1.25    | GHz   |
|                   |  | $F\_SEL[1:0] = 01$ |         |         | 625     | MHz   |
|                   |  | $F\_SEL[1:0] = 10$ |         |         | 312.5   | MHz   |
|                   |  | $F\_SEL[1:0] = 11$ |         |         | 156.25  | MHz   |
| $t_{PLH}$         | Propagation Delay, Low-to-High; NOTE 1 |                    | 0.8     |         | 1.6     | ns    |
| $t_{sk(i)}$       | Input Skew                             |                    |         |         | 60      | ps    |
| $t_{sk(o)}$       | Output Skew; NOTE 2, 3                 |                    |         |         | 25      | ps    |
| $t_{sk(pp)}$      | Part-to-Part Skew; NOTE 2; 4           |                    |         |         | 650     | ps    |
| $t_R / t_F$       | Output Rise/Fall Time                  | 20% to 80%         | 90      |         | 250     | ps    |
| odc               | Output Duty Cycle                      |                    | 47      |         | 53      | %     |
| $MUX_{ISOLATION}$ | MUX Isolation; NOTE 5                  |                    |         | >100    |         | dB    |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: This parameter is defined according with JEDEC Standard 65.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential output crossing point.

NOTE 5: Q, nQ outputs measured differentially. See *MUX Isolation diagram* in the Parameter Measurement Information Section.

**Table 6B. LVPECL AC Characteristics**,  $V_{CC} = V_{CC\_TAP} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$ 

| Symbol            | Parameter                              | Test Conditions    | Minimum | Typical | Maximum | Units |
|-------------------|--|--------------------|---------|---------|---------|-------|
| $f_{IN}$          | Input Frequency                        |                    |         |         | 2.5     | GHz   |
| $f_{OUT}$         | Output Frequency                       | $F\_SEL[1:0] = 00$ |         |         | 1.25    | GHz   |
|                   |  | $F\_SEL[1:0] = 01$ |         |         | 625     | MHz   |
|                   |  | $F\_SEL[1:0] = 10$ |         |         | 312.5   | MHz   |
|                   |  | $F\_SEL[1:0] = 11$ |         |         | 156.25  | MHz   |
| $t_{PLH}$         | Propagation Delay, Low-to-High; NOTE 1 |                    | 0.8     |         | 1.6     | ns    |
| $t_{sk(i)}$       | Input Skew                             |                    |         |         | 60      | ps    |
| $t_{sk(o)}$       | Output Skew; NOTE 2, 3                 |                    |         |         | 25      | ps    |
| $t_{sk(pp)}$      | Part-to-Part Skew; NOTE 2; 4           |                    |         |         | 650     | ps    |
| $t_R / t_F$       | Output Rise/Fall Time                  | 20% to 80%         | 90      |         | 250     | ps    |
| odc               | Output Duty Cycle                      |                    | 47      |         | 53      | %     |
| $MUX_{ISOLATION}$ | MUX Isolation                          |                    |         | >100    |         | dB    |

For NOTES, see Table 6A above.

**Table 6C. LVDS AC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{CC\_TAP} = \text{Float}$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

| Symbol            | Parameter                              | Test Conditions    | Minimum | Typical | Maximum | Units |
|-------------------|--|--------------------|---------|---------|---------|-------|
| $f_{IN}$          | Input Frequency                        |                    |         |         | 2.5     | GHz   |
| $f_{OUT}$         | Output Frequency                       | $F\_SEL[1:0] = 00$ |         |         | 1.25    | GHz   |
|                   |  | $F\_SEL[1:0] = 01$ |         |         | 625     | MHz   |
|                   |  | $F\_SEL[1:0] = 10$ |         |         | 312.5   | MHz   |
|                   |  | $F\_SEL[1:0] = 11$ |         |         | 156.25  | MHz   |
| $t_{PLH}$         | Propagation Delay, Low-to-High; NOTE 1 |                    | 0.8     |         | 1.6     | ns    |
| $t_{sk(i)}$       | Input Skew                             |                    |         |         | 75      | ps    |
| $t_{sk(o)}$       | Output Skew; NOTE 2, 3                 |                    |         |         | 25      | ps    |
| $t_{sk(pp)}$      | Part-to-Part Skew; NOTE 2; 4           |                    |         |         | 650     | ps    |
| $t_R / t_F$       | Output Rise/Fall Time                  | 20% to 80%         | 70      |         | 250     | ps    |
| odc               | Output Duty Cycle                      |                    | 46      |         | 54      | %     |
| $MUX_{ISOLATION}$ | MUX Isolation                          |                    |         | >100    |         | dB    |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: This parameter is defined according with JEDEC Standard 65.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential output crossing point.

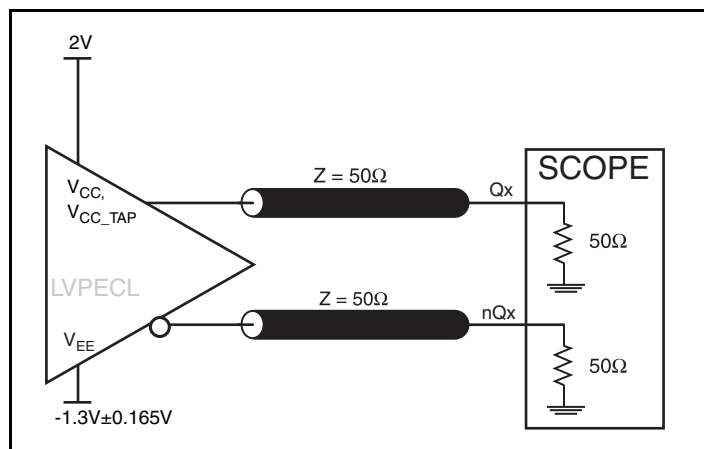
NOTE 5: Q, nQ outputs measured differentially. See *MUX Isolation diagram* in the Parameter Measurement Information Section..

**Table 6D. LVDS AC Characteristics,  $V_{CC} = V_{CC\_TAP} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

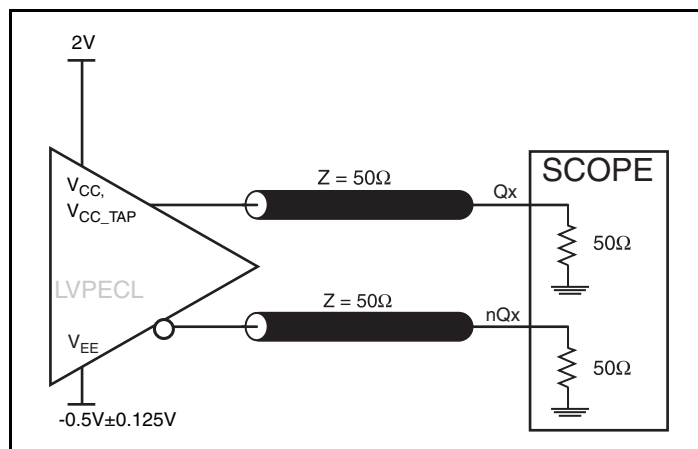
| Symbol            | Parameter                              | Test Conditions    | Minimum | Typical | Maximum | Units |
|-------------------|--|--------------------|---------|---------|---------|-------|
| $f_{IN}$          | Input Frequency                        |                    |         |         | 2.5     | GHz   |
| $f_{OUT}$         | Output Frequency                       | $F\_SEL[1:0] = 00$ |         |         | 1.25    | GHz   |
|                   |  | $F\_SEL[1:0] = 01$ |         |         | 625     | MHz   |
|                   |  | $F\_SEL[1:0] = 10$ |         |         | 312.5   | MHz   |
|                   |  | $F\_SEL[1:0] = 11$ |         |         | 156.25  | MHz   |
| $t_{PLH}$         | Propagation Delay, Low-to-High; NOTE 1 |                    | 0.8     |         | 1.6     | ns    |
| $t_{sk(i)}$       | Input Skew                             |                    |         |         | 75      | ps    |
| $t_{sk(o)}$       | Output Skew; NOTE 2, 3                 |                    |         |         | 25      | ps    |
| $t_{sk(pp)}$      | Part-to-Part Skew; NOTE 2; 4           |                    |         |         | 650     | ps    |
| $t_R / t_F$       | Output Rise/Fall Time                  | 20% to 80%         | 70      |         | 250     | ps    |
| odc               | Output Duty Cycle                      |                    | 46      |         | 54      | %     |
| $MUX_{ISOLATION}$ | MUX Isolation                          |                    |         | >100    |         | dB    |

For NOTES, see Table 6C above.

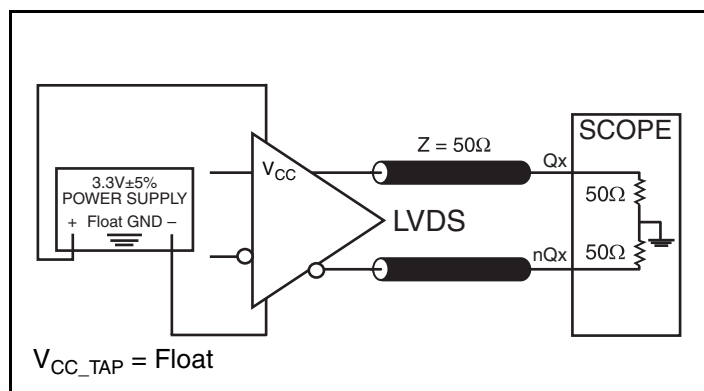
## Parameter Measurement Information



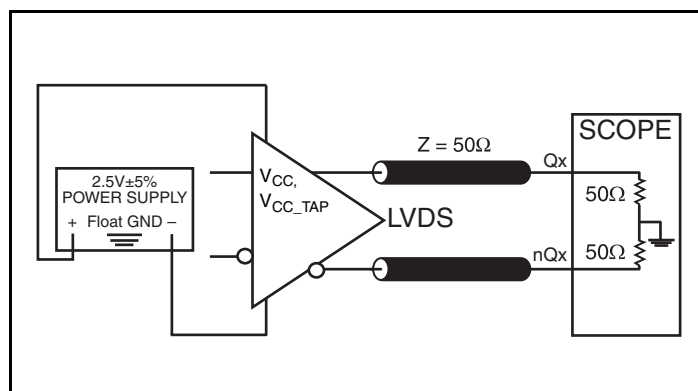
3.3V LVPECL Output Load AC Test Circuit



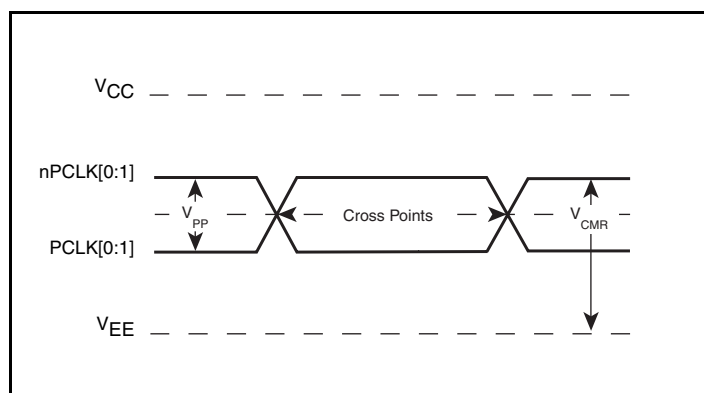
2.5V LVPECL Output Load AC Test Circuit



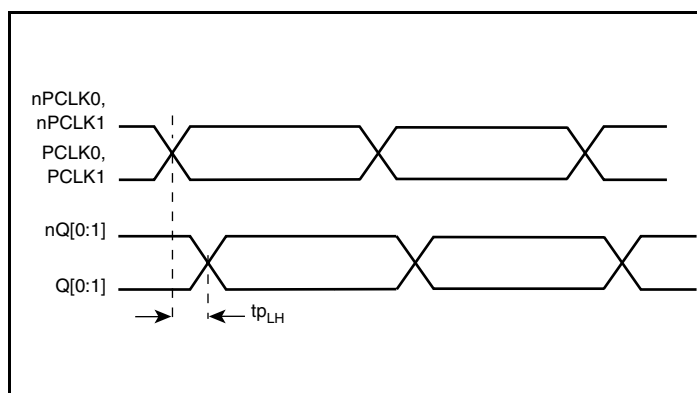
3.3V LVDS Output Load AC Test Circuit



2.5V LVDS Output Load AC Test Circuit

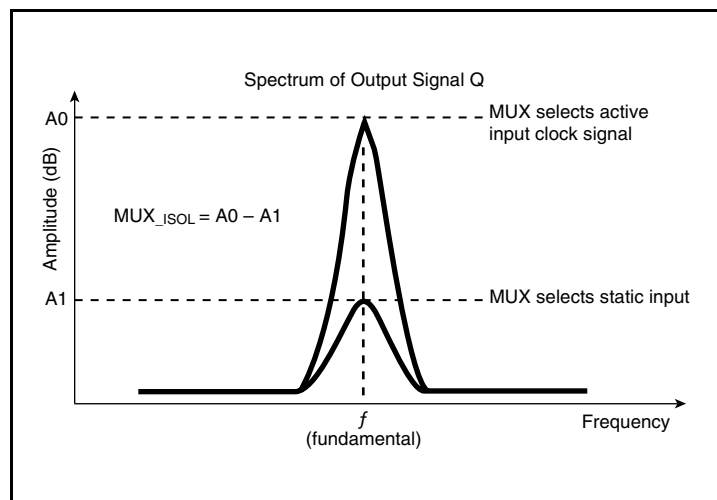


Differential Input Level

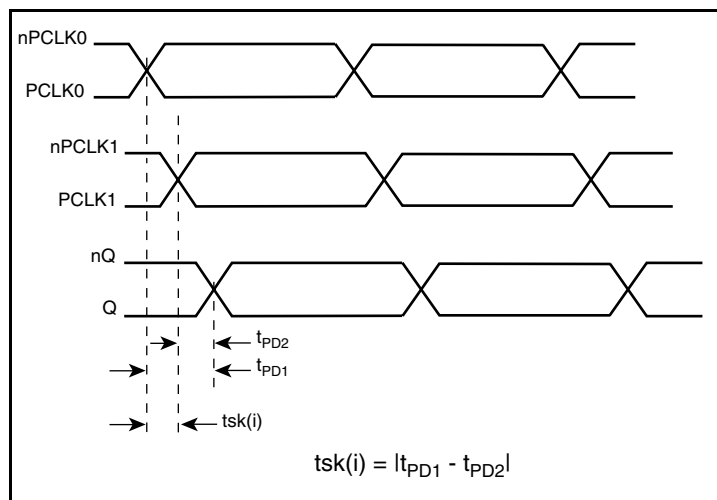


Propagation Delay

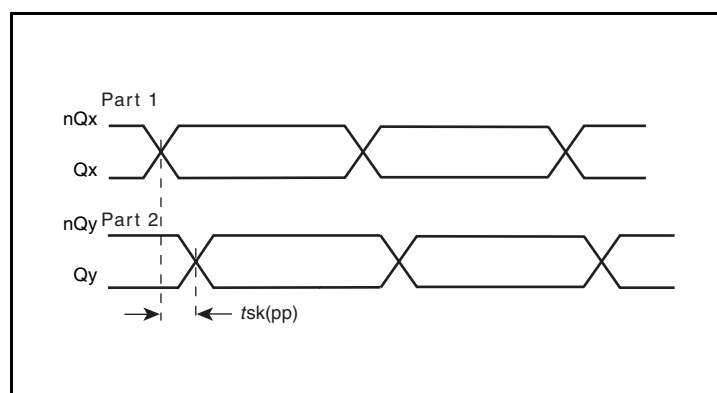
## Parameter Measurement Information, continued



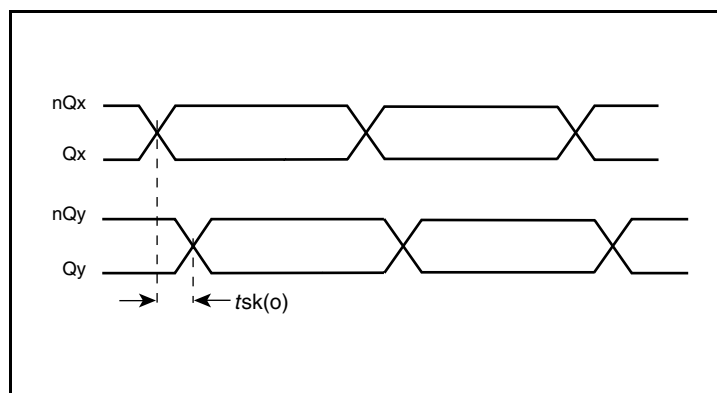
**MUX Isolation**



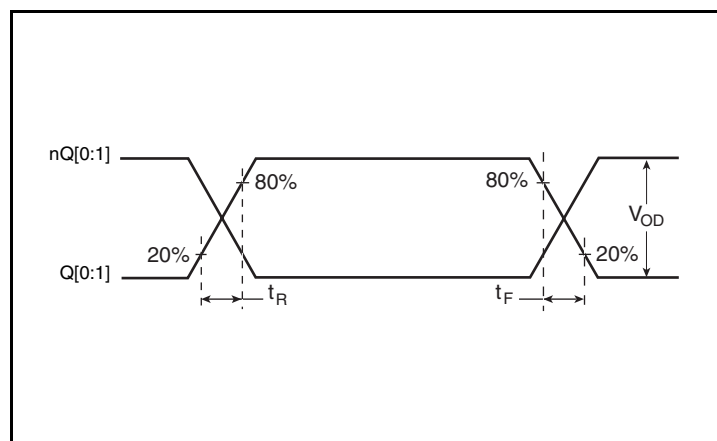
**Input Skew**



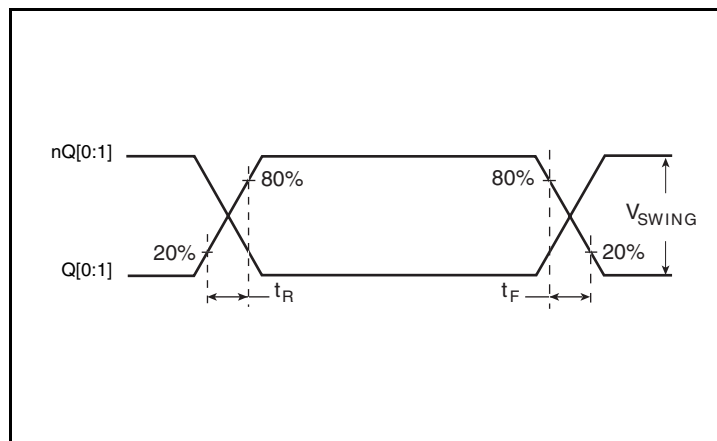
**Part-to-Part Skew**



**Output Skew**



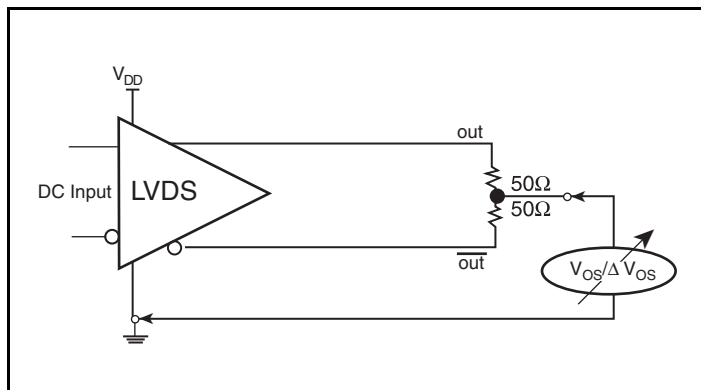
**LVDS Output Rise/Fall Time**



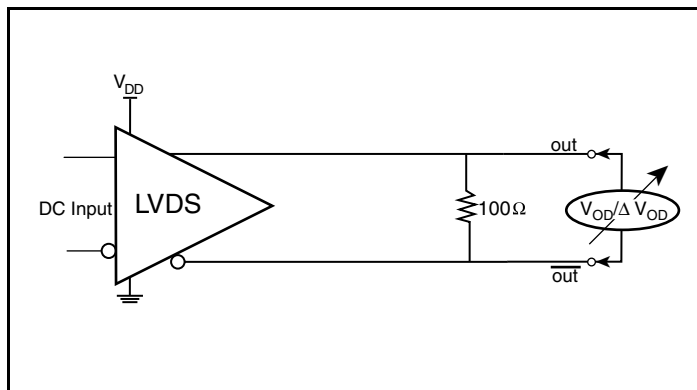
**LVPECL Output Rise/Fall Time**



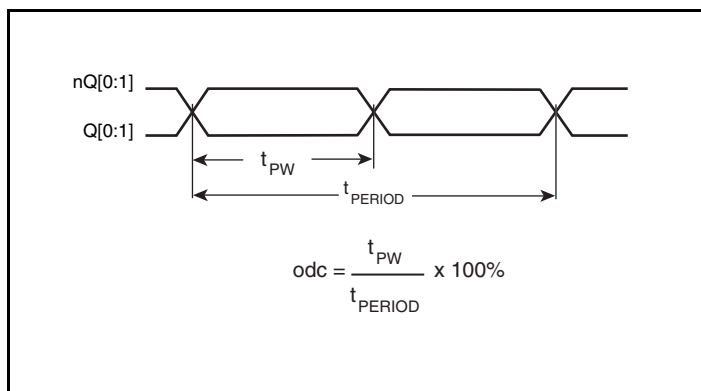
## Parameter Measurement Information, continued



Offset Voltage Setup



Differential Output Voltage Setup



Output Duty Cycle/Pulse Width/Period

## Applications Information

### Recommendations for Unused Input and Output Pins

#### Inputs:

##### PCLK/nPCLK Inputs

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from PCLK to ground.

##### LVCN00 Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

#### Outputs:

##### LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

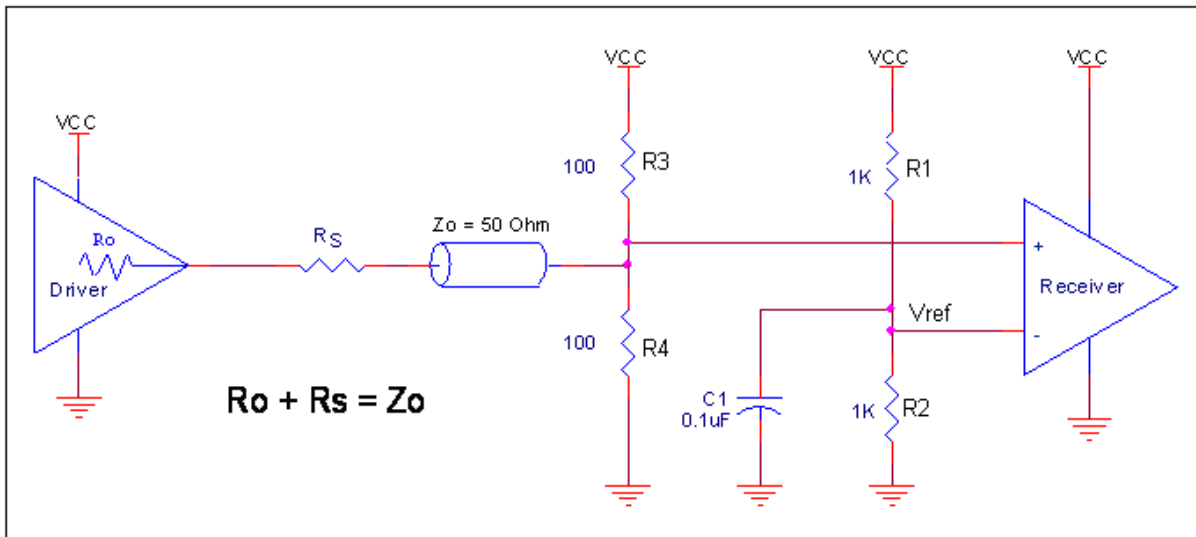
##### LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100 $\Omega$  across. If they are left floating, there should be no trace attached.

### Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{CC}/2$  is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is 2.5V and  $V_{CC} = 3.3V$ , R1 and R2 value should be adjusted to set  $V_{REF}$  at 1.25V. The values below are for when both the single ended swing and  $V_{CC}$  are at the same voltage. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission

line impedance. For most 50 $\Omega$  applications, R3 and R4 can be 100 $\Omega$ . The values of the resistors can be increased to reduce the loading for slower and weaker LVCN00 driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCN00 signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however  $V_{IL}$  cannot be less than -0.3V and  $V_{IH}$  cannot be more than  $V_{CC} + 0.3V$ . Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.



**Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels**

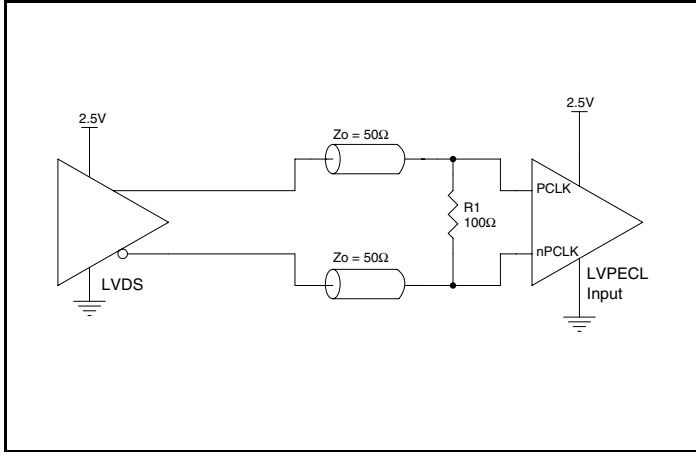
The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



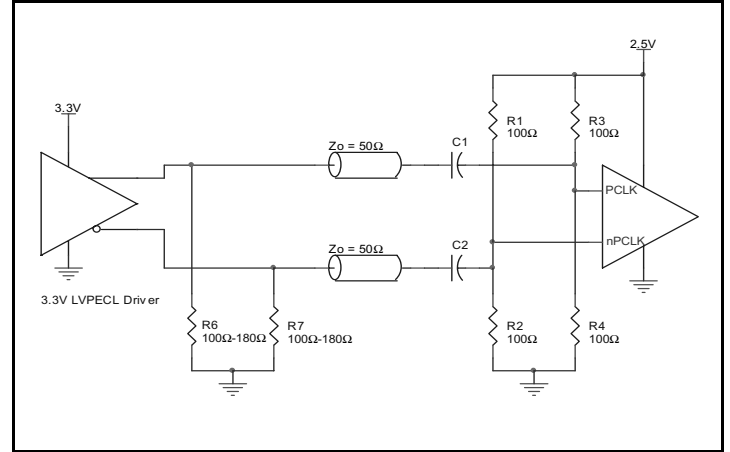
## 2.5V LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS and other differential signals. The differential signals must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. *Figures 3A to 3C* show interface examples for the PCLK/nPCLK input driven by the most common driver types. The

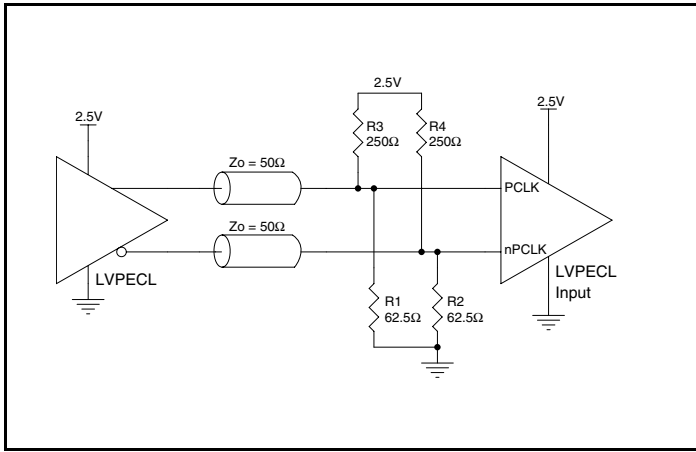
input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



**Figure 3A. PCLK/nPCLK Input Driven by a 2.5V LVDS Driver**



**Figure 3B. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple**



**Figure 3C. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver**

## LVDS Driver Termination

A general LVDS interface is shown in *Figure 4*. Standard termination for LVDS type output structure requires both a 100Ω parallel resistor at the receiver and a 100Ω differential transmission line environment. In order to avoid any transmission line reflection issues, the 100Ω resistor must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard

termination schematic as shown in *Figure 4* can be used with either type of output structure. If using a non-standard termination, it is recommended to contact IDT and confirm if the output is a current source or a voltage source type structure. In addition, since these outputs are LVDS compatible, the amplitude and common mode input range of the input receivers should be verified for compatibility with the output.

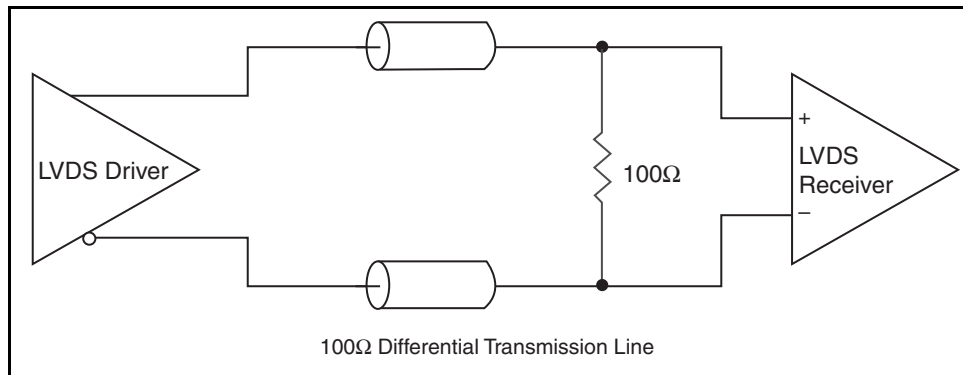


Figure 4. Typical LVDS Driver Termination

## Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

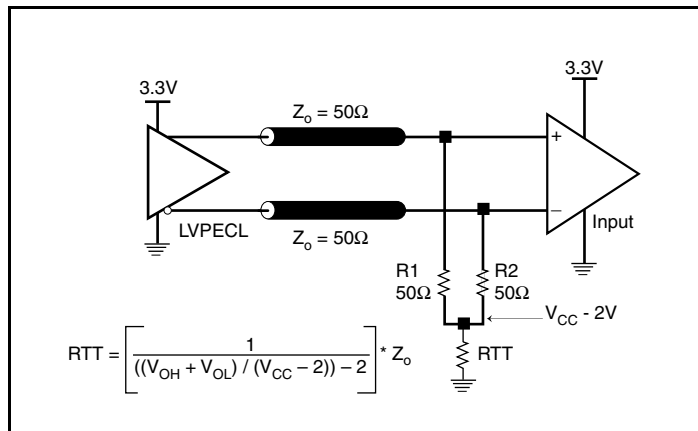


Figure 5A. 3.3V LVPECL Output Termination

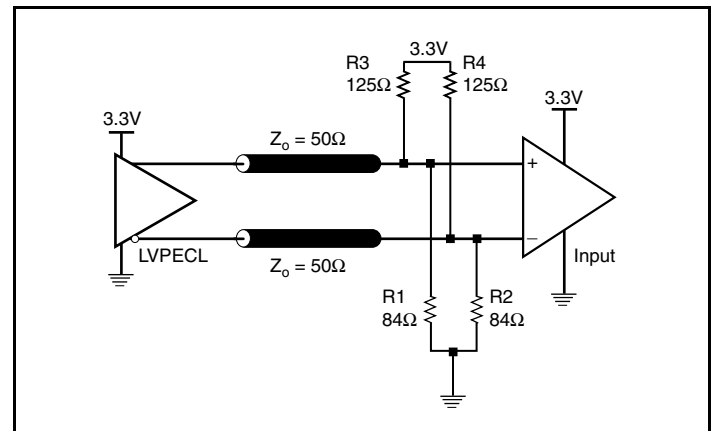


Figure 5B. 3.3V LVPECL Output Termination

## Termination for 2.5V LVPECL Outputs

Figure 6A and Figure 5B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating  $50\Omega$  to  $V_{CC} - 2V$ . For  $V_{CC} = 2.5V$ , the  $V_{CC} - 2V$  is very close to ground

level. The  $R3$  in Figure 6B can be eliminated and the termination is shown in Figure 6C.

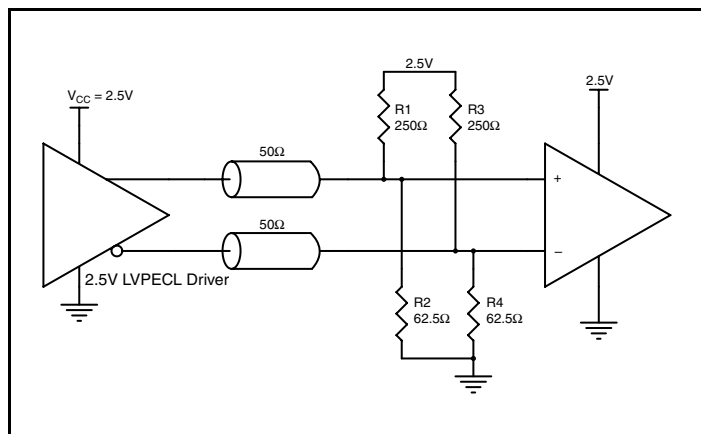


Figure 6A. 2.5V LVPECL Driver Termination Example

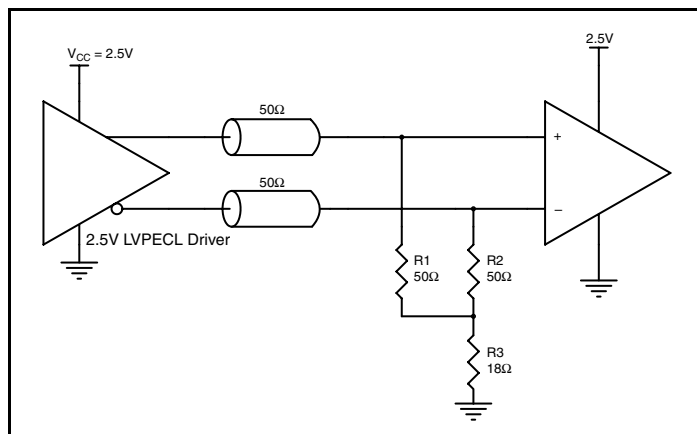


Figure 6B. 2.5V LVPECL Driver Termination Example

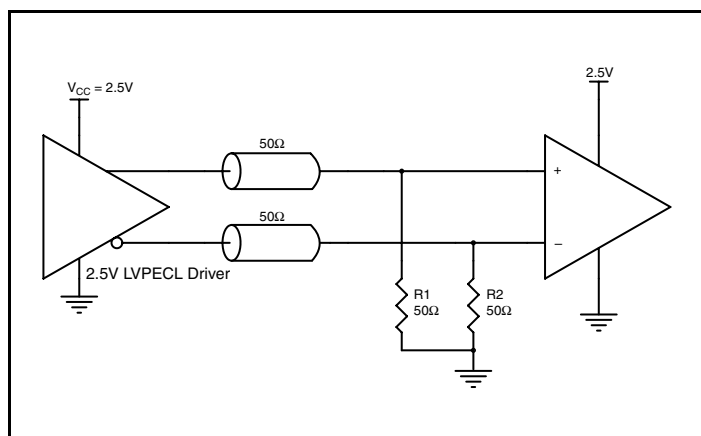


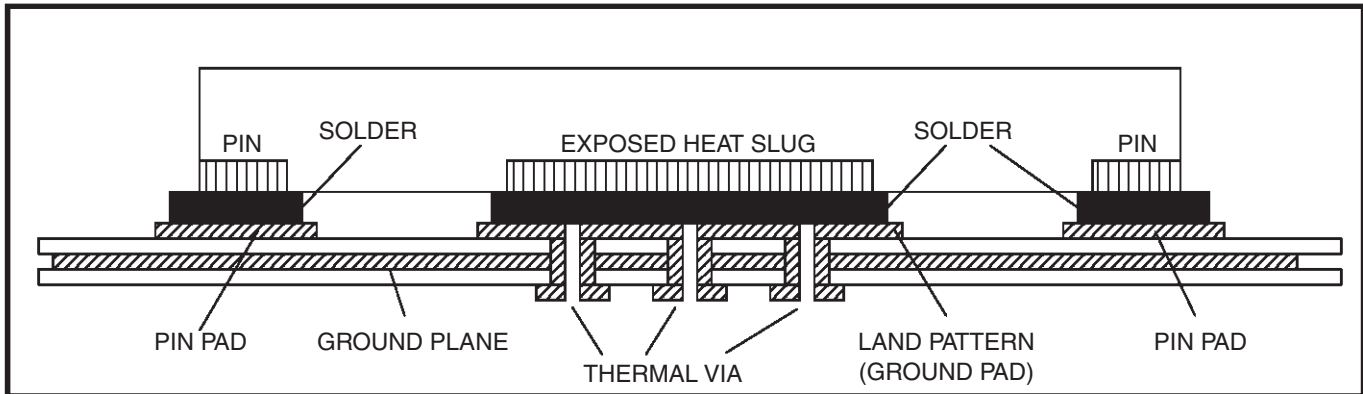
Figure 6C. 2.5V LVPECL Driver Termination Example

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 7*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.



**Figure 7. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**

## LVPECL Power Considerations

This section provides information on power dissipation and junction temperature for the ICS879S2162I-02. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS879S216I-02 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 65mA = 225.225mW$
- Power (outputs)<sub>MAX</sub> = **32mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $2 * 32mW = 64mW$

**Total Power**<sub>MAX</sub> (3.465, with all outputs switching) =  $225.225mW + 64mW = 289.225mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 49.5°C/W per Table 7 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.289W * 49.5^\circ C/W = 99.3^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 7. Thermal Resistance  $\theta_{JA}$  for 24 Lead VFQFN, Forced Convection**

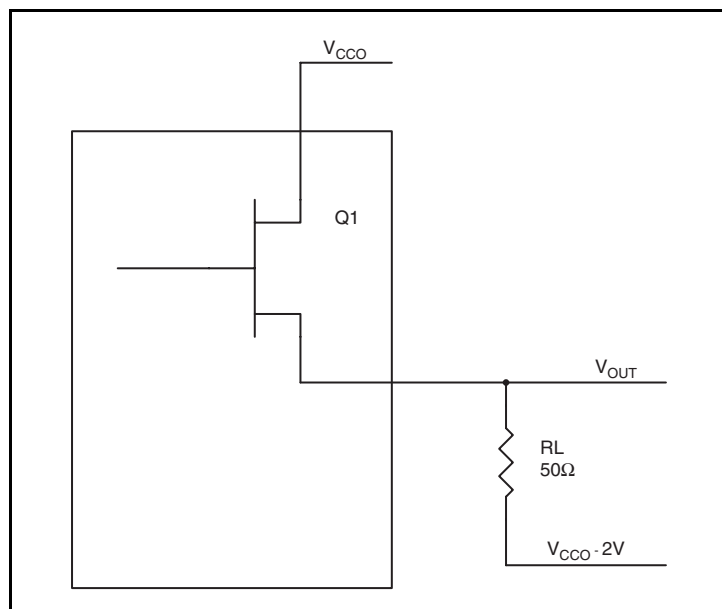
| $\theta_{JA}$ by Velocity                   |          |          |          |
|---|----------|----------|----------|
| Meters per Second                           | 0        | 1        | 2.5      |
| Multi-Layer PCB, JEDEC Standard Test Boards | 49.5°C/W | 43.3°C/W | 38.8°C/W |



### 3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 8*.



**Figure 8. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CC} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} - 0.8V$   
 $(V_{CC\_MAX} - V_{OH\_MAX}) = 0.8V$
- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} - 1.6V$   
 $(V_{CC\_MAX} - V_{OL\_MAX}) = 1.6V$

$Pd\_H$  is power dissipation when the output drives high.

$Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - 0.8V)/50\Omega] * 0.8V = 19.2mW$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - 1.6V)/50\Omega] * 1.6V = 12.8mW$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = 32mW$$

## LVDS Power Considerations

This section provides information on power dissipation and junction temperature for the ICS879S2162I-02. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS879S2162I-02 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 95mA = 329.175mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd_{total} + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd_{total}$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 49.5°C/W per Table 8 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.329W * 49.5^\circ C/W = 101.3^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 8. Thermal Resistance  $\theta_{JA}$  for 24 Lead VFQFN, Forced Convection**

| $\theta_{JA}$ by Velocity                   |          |          |          |
|---|----------|----------|----------|
| Meters per Second                           | 0        | 1        | 2.5      |
| Multi-Layer PCB, JEDEC Standard Test Boards | 49.5°C/W | 43.3°C/W | 38.8°C/W |

## Reliability Information

**Table 9.  $\theta_{JA}$  vs. Air Flow Table for a 24 Lead VFQFN**

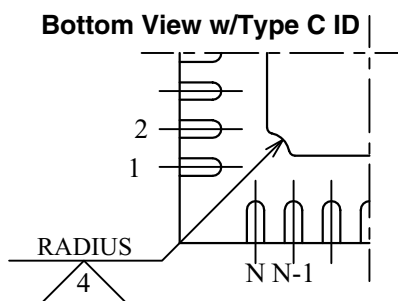
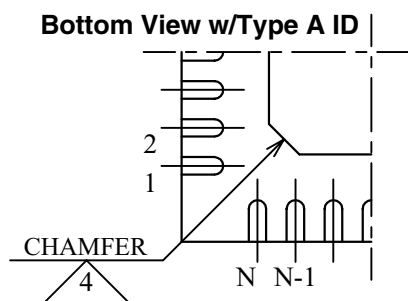
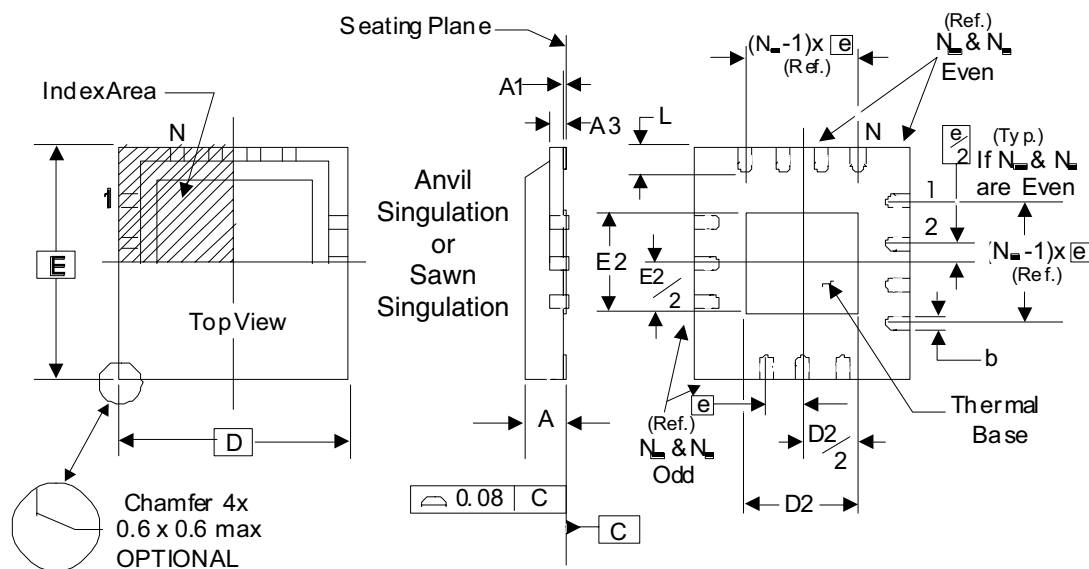
| $\theta_{JA}$ vs. Air Flow                  |          |          |          |
|---|----------|----------|----------|
| Meters per Second                           | 0        | 1        | 2.5      |
| Multi-Layer PCB, JEDEC Standard Test Boards | 49.5°C/W | 43.3°C/W | 38.8°C/W |

## Transistor Count

The transistor count for ICS879S216I-02 is: 1039

# Package Outline and Package Dimensions

## Package Outline - K Suffix for 24 Lead VFQFN



There are 2 methods of indicating pin 1 corner at the back of the VFQFN package are:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

**Table 10. Package Dimensions**

| JEDEC Variation: VEED-2/-4<br>All Dimensions in Millimeters |                |         |
|---|----------------|---------|
| Symbol  | Minimum        | Maximum |
| <b>N</b>  | 24             |         |
| <b>A</b>  | 0.80           | 1.0     |
| <b>A1</b>   | 0              | 0.05    |
| <b>A3</b>   | 0.25 Reference |         |
| <b>b</b>  | 0.18           | 0.30    |
| <b>e</b>  | 0.50 Basic     |         |
| <b>D, E</b>   | 4              |         |
| <b>D2, E2</b>   | 2.30           | 2.55    |
| <b>L</b>  | 0.30           | 0.50    |
| <b>N<sub>D</sub> N<sub>E</sub></b>                          | 6              |         |

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 10.

## Ordering Information

Table 11. Ordering Information

| Part/Order Number | Marking | Package                   | Shipping Packaging | Temperature   |
|-------------------|---------|---------------------------|--------------------|---------------|
| 879S216AKI-02LF   | 6AI02L  | "Lead-Free" 24 Lead VFQFN | Tray               | -40°C to 85°C |
| 879S216AKI-02LFT  | 6AI02L  | "Lead-Free" 24 Lead VFQFN | 2500 Tape & Reel   | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.



## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.