Low Skew, 1-to-9 LVCMOS / LVTTL Clock Multiplier

87950I

PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES NOVEMBER 2, 2016 **DATA SHEET**

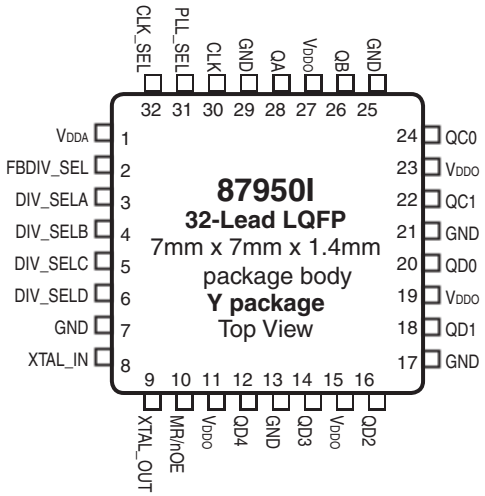
General Description

The 87950I is a low voltage, low skew 1-9 LVCMOS/LVTTL Clock Generator. With output frequencies up to 250MHz the 87950I is targeted for high performance clock applications. Along with a fully integrated PLL the 87950I contains frequency configurable outputs.

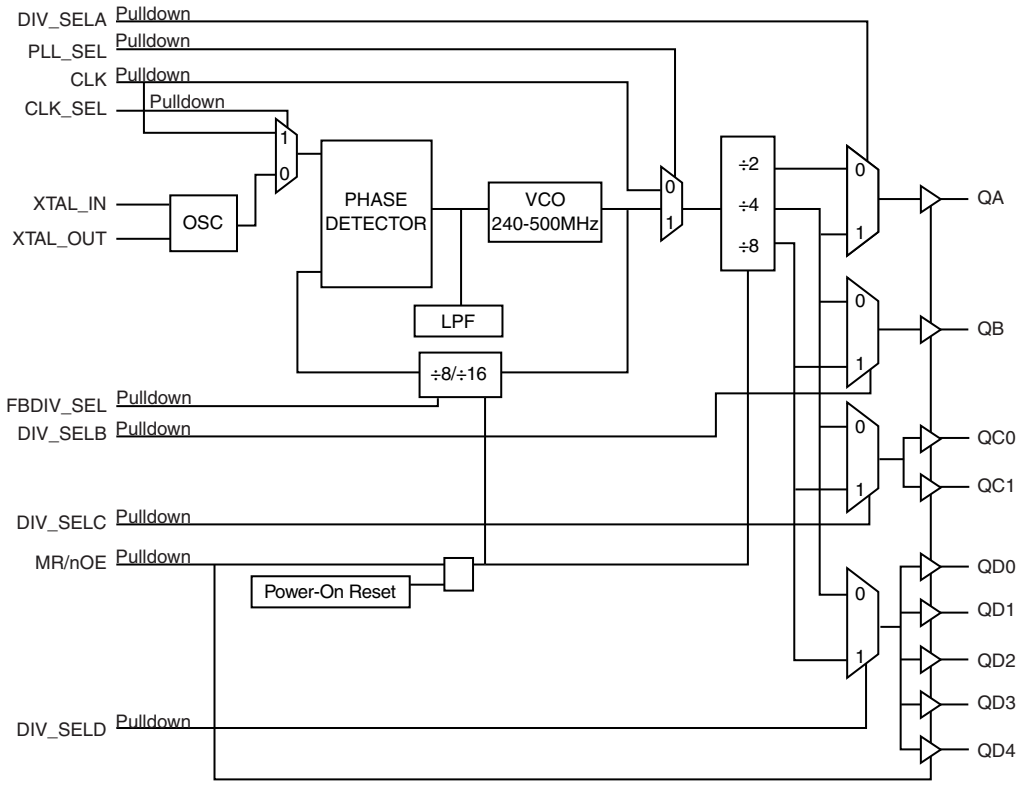
Features

- Fully integrated PLL
- 9 single ended 3.3V LVCMOS/LVTTL outputs
- Selectable CLK or single ended crystal inputs
- Maximum output frequency: 250MHz
- Maximum VCO range: 240MHz to 500MHz
- Cycle-to-cycle jitter: ±100 (typical)
- Output skew: 375ps (maximum) all outputs @ same frequency
- 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package
- For functional replacement part use 87973i

Pin Assignment



Block Diagram



© 2019 Renesas Electronics Corporation

Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{DDA}	Power		Analog supply pin.
2	FBDIV_SEL	Input	Pulldown	Selects divide value for Bank feedback output as described in Table 3E. LVCMOS / LVTTL interface levels.
3	DIV_SELA	Input	Pulldown	Selects divide value for Bank A output as described in Table 3D. LVCMOS / LVTTL interface levels.
4	DIV_SELB	Input	Pulldown	Selects divide value for Bank B output as described in Table 3D. LVCMOS / LVTTL interface levels.
5	DIV_SELC	Input	Pulldown	Selects divide value for Bank C outputs as described in Table 3D. LVCMOS / LVTTL interface levels.
6	DIV_SELD	Input	Pulldown	Selects divide value for Bank D outputs as described in Table 3D. LVCMOS / LVTTL interface levels.
7, 13, 17, 21, 25, 29	GND	Power		Power supply ground.
8, 9	XTAL_IN, XTAL_ OUT	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
10	MR/nOE	Input	Pulldown	Active High Master Reset. Active Low Output Enable. When logic HIGH, the internal dividers are reset and the outputs are tri-stated (HiZ). When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
11, 15, 19, 23, 27	V_{DDO}	Power		Output supply pins.
12, 14, 16, 18, 20	QD4, QD3, QD2, QD1, QD0	Output		Bank D clock outputs. 7Ω typical output impedance. LVCMOS / LVTTL interface levels.
22, 24	QC1, QC0	Output		Bank C clock outputs. 7Ω typical output impedance. LVCMOS / LVTTL interface levels.
26	QB	Output		Bank B clock output. 7Ω typical output impedance. LVCMOS / LVTTL interface levels.
28	QA	Output		Bank A clock output. 7Ω typical output impedance. LVCMOS / LVTTL interface levels.
30	CLK	Input	Pulldown	LVCMOS / LVTTL phase detector reference clock input.
31	PLL_SEL	Input	Pulldown	Selects between the PLL and the reference clock as the input to the dividers. When HIGH, selects PLL. When LOW, selects the reference clock. LVCMOS / LVTTL interface levels.
32	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK. When LOW, selects XTAL_IN, XTAL _OUT. LVCMOS / LVTTL interface levels.

NOTE: refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DDA}, V_{DDO} = 3.47V		25		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance		5	7	12	Ω

© 2019 Renesas Electronics Corporation

TABLE 3A. OUTPUT CONTROL PIN FUNCTION TABLE

Inputs	Outputs			
MR/nOE	QA	QB	QC0, QC1	QD0:QD4
1	HiZ	HiZ	HiZ	HiZ
0	Enabled	Enabled	Enabled	Enabled

TABLE 3B. OPERATING MODE FUNCTION TABLE

Inputs	Operating Mode
PLL_SEL	
0	Bypass
1	PLL

TABLE 3C. PLL INPUT FUNCTION TABLE

Inputs	
CLK_SEL	PLL Input
0	XTAL Oscillator
1	CLK

TABLE 3D. PROGRAMMABLE OUTPUT FREQUENCY FUNCTION TABLE FOR FBDIV-SEL

Inputs	
FBDIV_SEL	Function
1	÷8
0	÷16

© 2019 Renesas Electronics Corporation

Table 3E. Programmable Output Frequency Function Table

Inputs				Outputs			
DIV_SELA	DIV_SELB	DIV_SELC	DIV_SELD	QA	QB	QCx	QDx
0	0	0	0	VCO/2	VCO/4	VCO/4	VCO/4
0	0	0	1	VCO/2	VCO/4	VCO/4	VCO/8
0	0	1	0	VCO/2	VCO/4	VCO/8	VCO/4
0	0	1	1	VCO/2	VCO/4	VCO/8	VCO/8
0	1	0	0	VCO/2	VCO/8	VCO/4	VCO/4
0	1	0	1	VCO/2	VCO/8	VCO/4	VCO/8
0	1	1	0	VCO/2	VCO/8	VCO/8	VCO/4
0	1	1	1	VCO/2	VCO/8	VCO/8	VCO/8
1	0	0	0	VCO/4	VCO/4	VCO/4	VCO/4
1	0	0	1	VCO/4	VCO/4	VCO/4	VCO/8
1	0	1	0	VCO/4	VCO/4	VCO/8	VCO/4
1	0	1	1	VCO/4	VCO/4	VCO/8	VCO/8
1	1	0	0	VCO/4	VCO/8	VCO/4	VCO/4
1	1	0	1	VCO/4	VCO/8	VCO/4	VCO/8
1	1	1	0	VCO/4	VCO/8	VCO/8	VCO/4
1	1	1	1	VCO/4	VCO/8	VCO/8	VCO/8

Table 3F. Input Reference vs. Output Frequency Relationship

Inputs				Outputs							
DIV_SELA	DIV_SELB	DIV_SELC	DIV_SELD	FBDIV_SEL = 1				FBDIV_SEL = 0			
				QA	QB	QCx	QDx	QA	QB	QCx	QDx
0	0	0	0	4x	2x	2x	2x	8x	4x	4x	4x
0	0	0	1	4x	2x	2x	x	8x	4x	4x	2x
0	0	1	0	4x	2x	x	2x	8x	4x	2x	4x
0	0	1	1	4x	2x	x	x	8x	4x	2x	2x
0	1	0	0	4x	x	2x	2x	8x	2x	4x	4x
0	1	0	1	4x	x	2x	x	8x	2x	4x	2x
0	1	1	0	4x	x	x	2x	8x	2x	2x	4x
0	1	1	1	4x	x	x	x	8x	2x	2x	2x
1	0	0	0	2x	2x	2x	2x	4x	4x	4x	4x
1	0	0	1	2x	2x	2x	x	4x	4x	4x	2x
1	0	1	0	2x	2x	x	2x	4x	4x	2x	4x
1	0	1	1	2x	2x	x	x	4x	4x	2x	2x
1	1	0	0	2x	x	2x	2x	4x	2x	4x	4x
1	1	0	1	2x	x	2x	x	4x	2x	4x	2x
1	1	1	0	2x	x	x	2x	4x	2x	2x	4x
1	1	1	1	2x	x	x	x	4x	2x	2x	2x

© 2019 Renesas Electronics Corporation

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DDA} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	42.1°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DDA}	Analog Supply Current				15	mA
I_{DDO}	Output Supply Current				115	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IN}	Input Current	$V_{DDA} = V_{IN} = 3.465V$			±120	µA
V_{OH}	Output High Voltage; NOTE 1		2.6			V
V_{OL}	Output Low Voltage; NOTE 1				0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$.

Table 5. Crystal Characteristics, $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		15		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

Table 6. PLL Input Reference Characteristics, $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Reference Frequency; NOTE 1		15		62.5	MHz

NOTE 1: Maximum and minimum input reference is limited by the VCO lock range and the feedback divider for the CLK input.

© 2019 Renesas Electronics Corporation

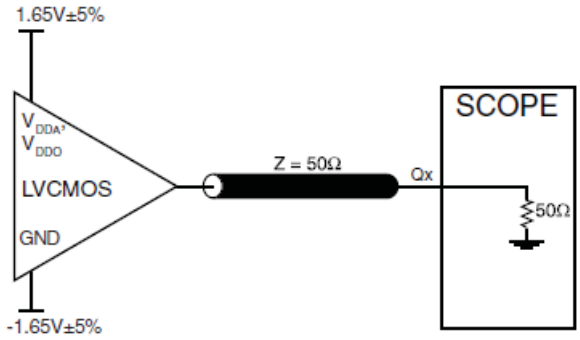
TABLE 7. AC CHARACTERISTICS, $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		÷2			250	MHz
			÷4			125	MHz
			÷8			62.5	MHz
f_{VCO}	PLL VCO Lock Range			240		500	MHz
tsk(o)	Output Skew; NOTE 1, 4	Same Frequency				375	ps
		Different Frequency	QA f_{MAX} < 150MHz			500	ps
			QA f_{MAX} > 150MHz			750	ps
tjit(cc)	Cycle-to-Cycle Jitter; NOTE 2, 4				±100		ps
t_L	PLL Lock Time; NOTE 4					10	mS
t_R / t_F	Output Rise/Fall Time		0.8V to 2V	0.1		1	ns
t_{PW}	Output Pulse Width; NOTE 3			$t_{PERIOD}/2$ - 1000		$t_{PERIOD}/2$ + 1000	ps
t_{PZL}, t_{PZH}	Output Enable Time					6	ns
t_{PLZ}, t_{PHZ}	Output Disable Time					7	ns

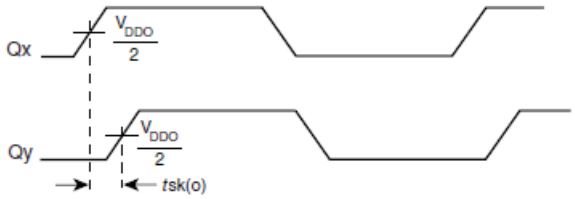
All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 2: Jitter performance using Xtal inputs.
NOTE 3: Measured using CLK.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

© 2019 Renesas Electronics Corporation

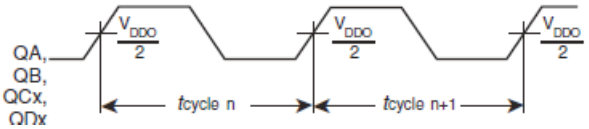
Parameter Measurement Information



3.3V Output Load AC Test Circuit



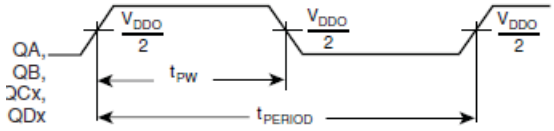
Output Skew



$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$

1000 Cycles

Cycle-to-Cycle Jitter



$odc = \frac{t_{PW}}{t_{PERIOD}}$

Output Pulse Width/Period

Output Rise/Fall Time

© 2019 Renesas Electronics Corporation

Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 87950I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DDO} and V_{DDA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA} pin.

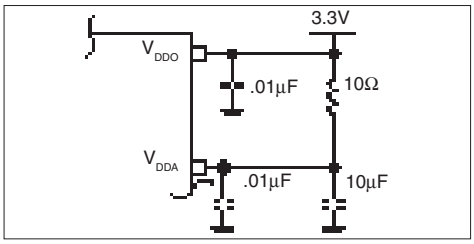


Figure 1. Power Supply Filtering

Crystal Input Interface

The 87950I has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. These same capacitor values will tune any 18pF parallel resonant crystal over the frequency range and other parameters specified in this data sheet. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

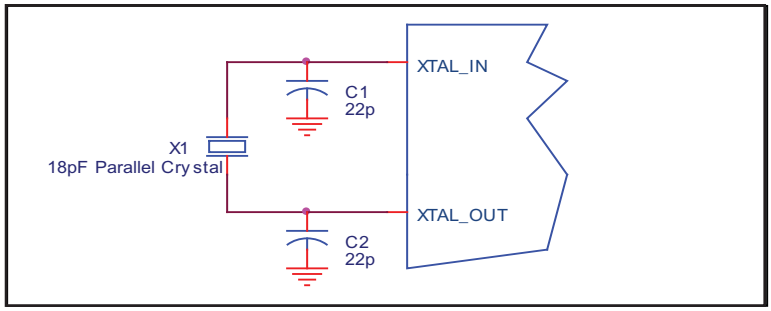


Figure 2. Crystal Input Interface

© 2019 Renesas Electronics Corporation

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for 32 Lead LQFP

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for 87950I is: 2674

© 2019 Renesas Electronics Corporation

Package Outline - Y Suffix for 32 Lead LQFP

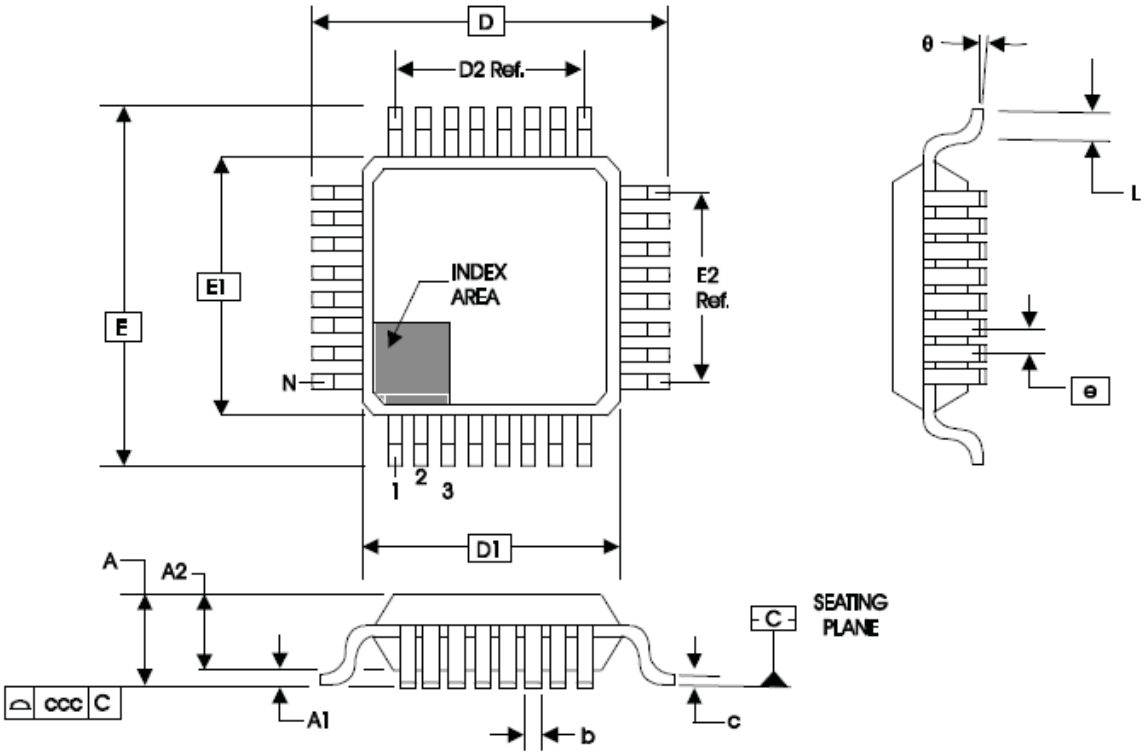


Table 9. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

© 2019 Renesas Electronics Corporation

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
87950BYILF	ICS87950BYIL	32 Lead “Lead-Free” LQFP	tray	-40°C to 85°C
87950BYILFT	ICS87950BYIL	32 Lead “Lead-Free” LQFP	1000 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

© 2019 Renesas Electronics Corporation

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	T5 T10	1 5 11	Features Section - added Lead-Free bullet. Crystal Characteristics Table - added Drive Level. Ordering Information Table - added Lead-Free part number and note. Changed XTAL1/2 naming convention to XTAL_IN/_OUT throughout the data-sheet.	6/14/05
B	T10	11	Ordering Information - Added Lead-Free Marking.	9/8/08
C	T10	11 13	Updated datasheet's header/footer with IDT from ICS. Removed ICS prefix from Part/Order Number column. Added Contact Page.	7/16/10
C	T10	11	Ordering Information - removed leaded devices, PDN CQ-13-02 Updated data sheet format	2/18/15
C		1	Product Discontinuation Notice - Last time buy expires November 2, 2016. PDN# CQ-15-05.	11/6/15

© 2019 Renesas Electronics Corporation

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2026 Renesas Electronics Corporation. All rights reserved.