ICS8752

Low Skew, 1-to-8
LVCMOS Clock Multiplier/Zero Delay Buffer

General Description

The ICS8752 is a low voltage, low skew LVCMOS clock generator. With output frequencies up to 240MHz, the ICS8752 is targeted for high performance clock applcations. Along with a fully integrated PLL, the ICS8752 contains frequency configurable outputs and an external feedback input for regenerating clocks with “zero delay”.

Dual clock inputs, CLK0 and CLK1, support redundant clock applications. The CLK_SEL input determines which reference clock is used. The output divider values of Bank A and B are controlled by the DIV_SELA0:1, and DIV_SELB0:1, respectively.

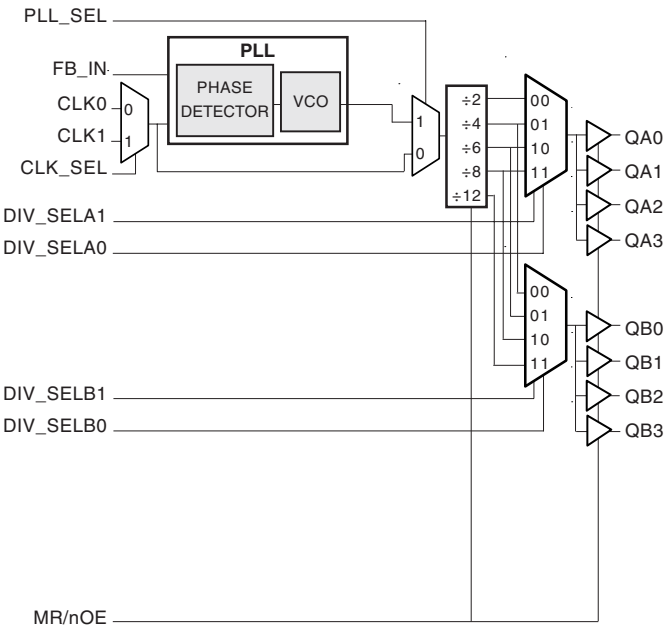
For test and system debug purposes, the PLL_SEL input allows the PLL to be bypassed. When HIGH, the MR/nOE input resets the internal dividers and forces the outputs to the high impedance state.

The low impedance LVCMOS outputs of the ICS8752 are designed to drive terminated transmission lines. The effective fanout of each output can be doubled by utilizing the ability of each output to drive two series terminated transmission lines.

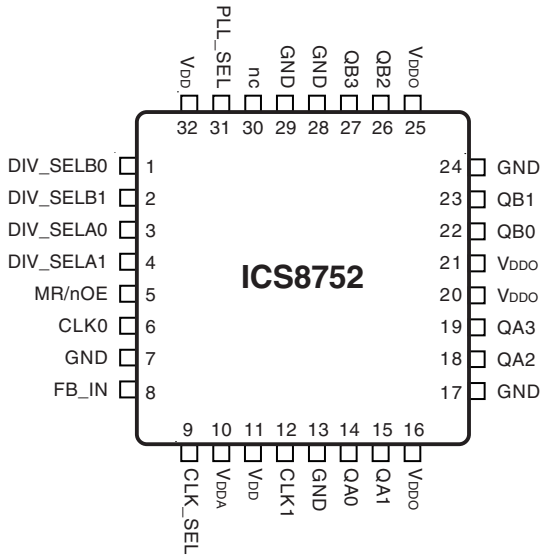
Features

- Fully integrated PLL
- Eight LVCMOS outputs, 7Ω typical output impedance
- Selectable LVCMOS CLK0 or CLK1 inputs for redundant clock applications
- Input/Output frequency range: 18.33MHz to 240MHz at V_{CC} = 3.3V ± 5%
- VCO range: 220MHz to 480MHz
- External feedback for “zero delay” clock regeneration
- Cycle-to-cycle jitter: 75ps (maximum), (all outputs are the same frequency)
- Output skew: 100ps (maximum)
- Bank skew: 55ps (maximum)
- Full 3.3V or 2.5V supply voltage
- 0°C to 70°C ambient operating temperature
- Available in both standard and lead-free RoHS-compliant packages

Block Diagram



Pin Assignment



32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y package
Top View

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TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	DIV_SELB0, DIV_SELB1	Input	Pulldown	Determines output divider values for Bank B as described in Table 3. LVCMOS / LVTTL interface levels.
3, 4	DIV_SELA0, DIV_SELA1	Input	Pulldown	Determines output divider values for Bank A as described in Table 3. LVCMOS / LVTTL interface levels.
5	MR/nOE	Input	Pulldown	When logic HIGH, the internal dividers are reset and the outputs are disabled. When logic LOW, the master reset is disabled and the outputs are enabled. LVCMOS / LVTTL interface levels.
6	CLK0	Input	Pulldown	Clock input. LVCMOS / LVTTL interface levels.
7, 13, 17, 24, 28, 29	GND	Power		Power supply ground.
8	FB_IN	Input	Pulldown	Feedback input to phase detector for generating clocks with "zero delay". LVCMOS / LVTTL interface levels.
9	CLK_SEL	Input	Pulldown	Clock select input. Selects between CLK0 or CLK1 as phase detector reference. When LOW, selects CLK0. When HIGH, selects CLK1. LVCMOS / LVTTL interface levels.
10	V_{DDA}	Power		Analog supply pin.
11, 32	V_{DD}	Power		Core supply pins.
12	CLK1	Input	Pulldown	Clock input. LVCMOS / LVTTL interface levels.
14, 15, 18, 19	QA0, QA1, QA2, QA3	Output		Bank A clock outputs. 7Ω typical output impedance. LVCMOS / LVTTL interface levels.
16, 20, 21, 25	V_{DDO}	Power		Output supply pins.
22, 23, 26, 27	QB0, QB1, QB2, QB3	Output		Bank B clock outputs. 7Ω typical output impedance. LVCMOS / LVTTL interface levels.
30	nc	Unused		No connect.
31	PLL_SEL	Input	Pullup	Selects between the PLL and CLK0 or CLK1 as the input to the dividers. When HIGH selects PLL. When LOW selects CLK0 or CLK1. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)	V_{DDA}, V_{DD}, V_{DDO} = 3.465V		23		pF
R_{OUT}	Output Impedance			7		Ω

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Table 3. Control Input Function Table

Inputs							Outputs	
MR/nOE	PLL_SEL	CLK_SEL	DIV_ SELA1	DIV_ SELA0	DIV_ SELB1	DIV_ SELB0	QAx	QBx
1	X	X	X	X	X	X	Hi-Z	Hi-Z
0	1	X	0	0	0	0	fVCO/2	fVCO/4
0	1	X	0	1	0	1	fVCO/4	fVCO/6
0	1	X	1	0	1	0	fVCO/6	fVCO/8
0	1	X	1	1	1	1	fVCO/8	fVCO/12
0	0	0	0	0	0	0	fCLK0/2	fCLK0/4
0	0	0	0	1	0	1	fCLK0/4	fCLK0/6
0	0	0	1	0	1	0	fCLK0/6	fCLK0/8
0	0	0	1	1	1	1	fCLK0/8	fCLK0/12
0	0	1	0	0	0	0	fCLK1/2	fCLK1/4
0	0	1	0	1	0	1	fCLK1/4	fCLK1/6
0	0	1	1	0	1	0	fCLK1/6	fCLK1/8
0	0	1	1	1	1	1	fCLK1/8	fCLK1/12

NOTE: For normal operation, MR/nOE is LOW. When MR/nOE is HIGH, all ouputs are disabled.

Table 4A. QA Output Frequency w/FB_IN = QB

Inputs									Outputs
FB_IN	DIV_ SELB1	DIV_ SELB0	QB Output Divider Mode (NOTE 2)	CLK0, CLK1 (MHz) (NOTE 1)		DIV_ SELA1	DIV_ SELA0	QA Output Divider Mode	QA Multiplier (NOTE 2)
				Minimum	Maximum				
QB	0	0	÷4	55	120	0	0	÷2	2
						0	1	÷4	1
						1	0	÷6	0.667
						1	1	÷8	0.5
QB	0	1	÷6	36.66	80	0	0	÷2	3
						0	1	÷4	1.5
						1	0	÷6	1
						1	1	÷8	0.75
QB	1	0	÷8	27.5	60	0	0	÷2	4
						0	1	÷4	2
						1	0	÷6	1.33
						1	1	÷8	1
QB	1	1	÷12	18.33	40	0	1	÷2	6
						0	1	÷4	3
						1	0	÷6	2
						1	1	÷8	1.5

NOTE 1: VCO frequency range is 220MHz to 480MHz.
NOTE 2: QA output frequency equal to CLKx frequency times the multiplier;
QB output frequency equal to CLKx.

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TABLE 4B. QB OUTPUT FREQUENCY W/FB_IN = QA

Inputs									Outputs
FB_IN	DIV_SELA1	DIV_SELA0	QA Output Divider Mode (NOTE 2)	CLK0, CLK1 (MHz) (NOTE 1)		DIV_SELB1	DIV_SELB0	QB Output Divider Mode	QB Multiplier (NOTE 2)
				Minimum	Maximum				
QA	0	0	÷2	110	240 (NOTE 3)	0	0	÷4	0.5
						0	1	÷6	0.333
						1	0	÷8	0.25
						1	1	÷12	0.167
QA	0	1	÷4	55	120	0	0	÷4	1
						0	1	÷6	0.667
						1	0	÷8	0.5
						1	1	÷12	0.333
QA	1	0	÷6	36.66	80	0	0	÷4	1.5
						0	1	÷6	1
						1	0	÷8	0.75
						1	1	÷12	0.5
QA	1	1	÷8	27.5	60	0	1	÷4	2
						0	1	÷6	1.333
						1	0	÷8	1
						1	1	÷12	0.667

NOTE 1: VCO frequency range is 220MHz to 480MHz.
NOTE 2: QB output frequency equal to CLKx frequency times the multiplier;
QA output frequency equal to CLKx.
NOTE 3: Maximum frequency of 240MHz valid for V_{CC} = 3.3V ± 5% only.

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Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 5A. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				105	mA
I_{DDA}	Analog Supply Current				15	mA
I_{DDO}	Output Supply Current				20	mA

Table 5B. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO} = 2.5V \pm 5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				100	mA
I_{DDA}	Analog Supply Current				15	mA
I_{DDO}	Output Supply Current				20	mA

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TABLE 5B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$ OR $2.5V±5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		$V_{DD} = 3.3V$	2		$V_{DD} + 0.3$	V
			$V_{DD} = 2.5V$	1.7		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		$V_{DD} = 3.3V$	-0.3		0.8	V
			$V_{DD} = 2.5V$	-0.3		0.7	V
I_{IH}	Input High Current	DIV_ SELx0, DIV_SELx1, CLK0, CLK1, FB_IN, CLK_SEL, MR/nOE	$V_{DD} = V_{IN} = 3.465V$ or 2.625V			150	µA
		PLL_SEL	$V_{DD} = V_{IN} = 3.465V$ or 2.625V			5	µA
I_{IL}	Input Low Current	DIV_ SELx0, DIV_SELx1, CLK0, CLK1, FB_IN, CLK_SEL, MR/nOE	$V_{DD} = 3.465V$ or 2.625V, $V_{IN} = 0V$	-5			µA
		PLL_SEL	$V_{DD} = 3.465V$ or 2.625V, $V_{IN} = 0V$	-150			µA
V_{OH}	Output High Voltage; NOTE 1		$V_{DDO} = V_{IN} = 3.465V$	2.6			V
			$V_{DDO} = V_{IN} = 2.625V$	1.8			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement Information section, "Output Load Test Circuit" diagrams.

TABLE 6A. PLL INPUT REFERENCE CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Reference Frequency NOTE: Input reference frequency is limited by the divider selection and the VCO lock range.		20		240	MHz

TABLE 6B. PLL INPUT REFERENCE CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 2.5V±5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Reference Frequency NOTE: Input reference frequency is limited by the divider selection and the VCO lock range.		20		120	MHz

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TABLE 7A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency (PLL Mode)		÷2	110		240	MHz
			÷4	55		120	MHz
			÷6	36.67		80	MHz
			÷8	27.5		60	MHz
			÷12	18.33		40	MHz
f_{VCO}	PLL VCO Lock Range			220		480	MHz
t(Ø)	Static Phase Offset; NOTE 1		fVCO = 400MHz, Feedback ÷ 8	-30	70	170	ps
*t*sk(b)	Bank Skew; NOTE 2, 4		Measured on rising edge at $V_{DDO}/2$			55	ps
*t*sk(o)	Output Skew; NOTE 3, 4		Measured on rising edge at $V_{DDO}/2$			100	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 4	Different Frequencies on Different Banks				400	ps
		All Outputs at Same Frequency				75	ps
t_L	PLL Lock Time					1	mS
t_R / t_F	Output Rise/Fall Time		20% to 80%	400		950	ps
odc	Output Duty Cycle			47	50	53	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Defined as the time difference between the input clock and the average feedback input signal, when the PLL is locked and the input reference frequency is stable.
NOTE 2: Defined as skew within a bank of outputs at the same supply voltages and with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

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TABLE 7B. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency (PLL Mode)		÷2	110		240	MHz
			÷4	55		120	MHz
			÷6	36.67		80	MHz
			÷8	27.5		60	MHz
			÷12	18.33		40	MHz
f_{VCO}	PLL VCO Lock Range			220		480	MHz
t(Ø)	Static Phase Offset; NOTE 1		fVCO = 400MHz Feedback ÷ 8	-90	50	190	ps
*t*sk(b)	Bank Skew; NOTE 2, 4		Measured on rising edge at $V_{DDO}/2$			55	ps
*t*sk(o)	Output Skew; NOTE 3, 4		Measured on rising edge at $V_{DDO}/2$			90	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 4	Different Frequencies on Different Banks				400	ps
		All Outputs at Same Frequency				75	ps
t_L	PLL Lock Time					1	mS
t_R / t_F	Output Rise/Fall Time		20% to 80%	400		950	ps
odc	Output Duty Cycle			45	50	55	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Defined as the time difference between the input clock and the average feedback input signal, when the PLL is locked and the input reference frequency is stable.
NOTE 2: Defined as skew within a bank of outputs at the same supply voltages and with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

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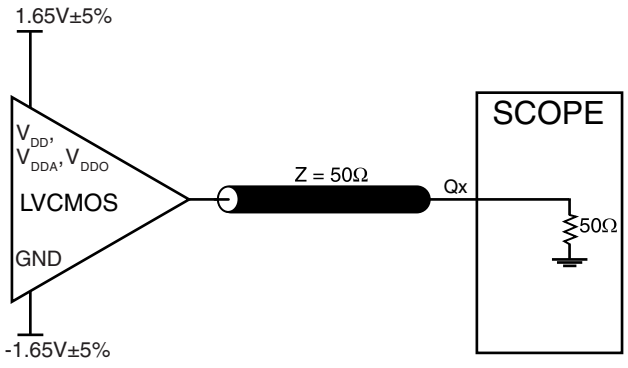
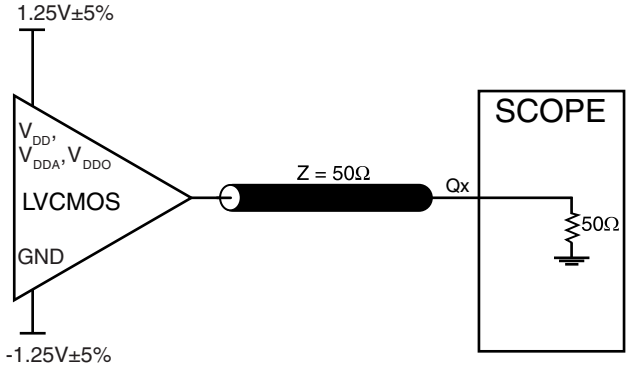
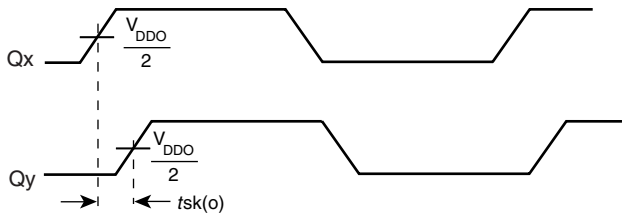
PARAMETER MEASUREMENT INFORMATION



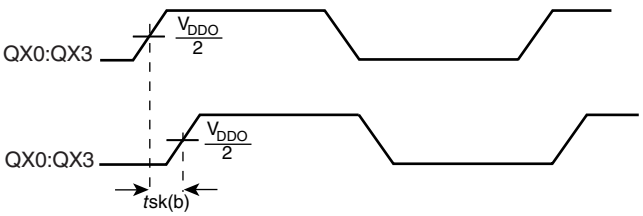
3.3V OUTPUT LOAD AC TEST CIRCUIT
(Where X denotes outputs in the same Bank)



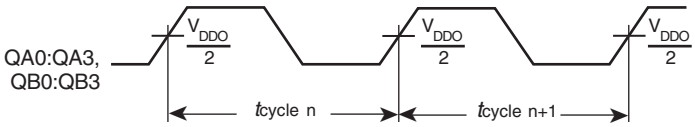
2.5V OUTPUT LOAD AC TEST CIRCUIT



OUTPUT SKEW

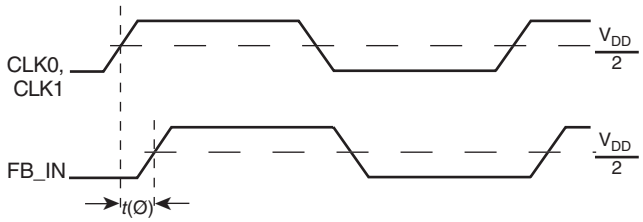


BANK SKEW

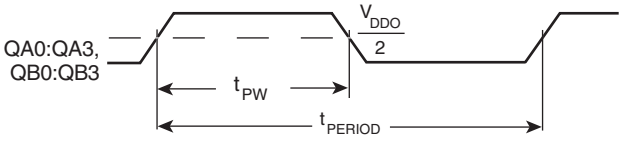


$t$jit(cc) = $t$cycle n – $t$cycle n+1
1000 Cycles

CYCLE-TO-CYCLE JITTER

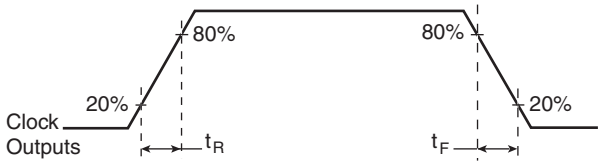


STATIC PHASE OFFSET



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYLCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

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APPLICATION INFORMATION

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CLK INPUT:
For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

LVCMOS CONTROL PINS:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUT:
All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 32 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT
The transistor count for ICS8752 is: 1546

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Package Outline - Y Suffix for 32 Lead LQFP

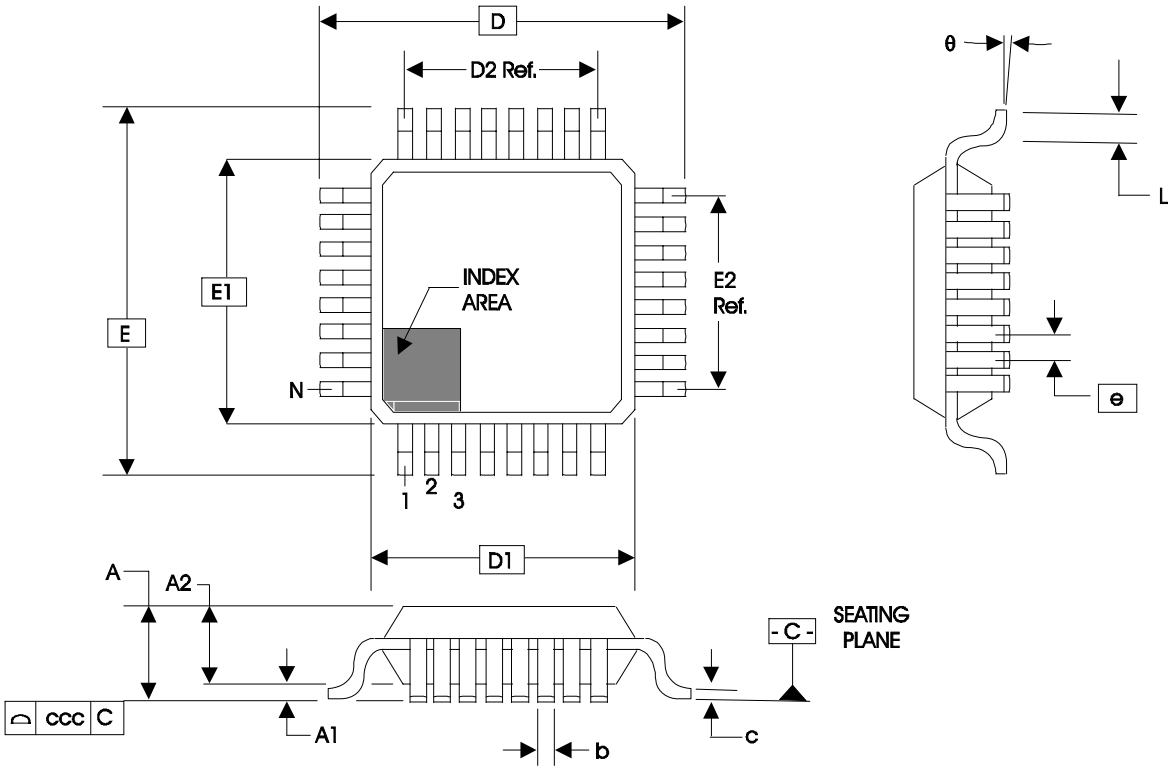

Table 8. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

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TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8752CY	ICS8752CY	32 Lead LQFP	tray	0°C to 70°C
8752CYT	ICS8752CY	32 Lead LQFP	1000 tape & reel	0°C to 70°C
8752CYLF	ICS8752CYLF	32 Lead "Lead-Free" LQFP	tray	0°C to 70°C
8752CYLFT	ICS8752CYLF	32 Lead "Lead-Free" LQFP	1000 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T1	2	Pin Descriptions Table. Revised MR/nOE description.	8/19/02
B	T2 T9	1 2 12	Features Section - delete bullet, "Industrial temperature available upon request." Added Lead-Free bullet. Pin Characteristics table - changed C_{IN} 4pF max. to 4pF typical. Ordering Information Table -added Lead-Free part number and note. Updated data sheet format.	3/31/05
B	T1	2	Pin Description Table - correct Pin 5, MR/nOE.	5/2/05
B	T9	10 12	Added *Recommendations for Unused Input and Output Pins.* Ordering Information Table - added lead-free marking.	10/19/05
C	T9	12 14	Updated datasheet's header/footer with IDT from ICS. Removed ""ICS"" prefix from Part/Order Number column. Added Contact Page.	7/2/10

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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