

### GENERAL DESCRIPTION

The 874003DI-02 is a high performance Differential-to-LVDS Jitter Attenuator designed for use in PCI Express™ systems. In some PCI Express systems, such as those found in desktop PCs, the PCI Express clocks are generated from a low bandwidth, high phase noise PLL frequency synthesizer. In these systems, a jitter attenuator may be required to attenuate high frequency random and deterministic jitter components from the PLL synthesizer and from the system board. The 874003DI-02 has a bandwidth of 3MHz. The 3MHz provides an intermediate bandwidth that can easily track triangular spread profiles, while providing good jitter attenuation. The 874003DI-02 uses IDT's 3<sup>rd</sup> Generation FemtoClock™ PLL technology to achieve the lowest possible phase noise. The device is packaged in a 20 Lead TSSOP package, making it ideal for use in space constrained applications such as PCI Express add-in cards.

### FEATURES

- Three differential LVDS output pairs
- One differential clock input
- CLK and nCLK supports the following input types: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Output frequency range: 98MHz - 320MHz
- Input frequency range: 98MHz - 128MHz
- VCO range: 490MHz - 640MHz
- Cycle-to-cycle jitter: 30ps (maximum)
- Supports PCI-Express Spread-Spectrum Clocking
- 3MHz PLL loop bandwidth
- 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

F\_SEL[2:0] FUNCTION TABLE

Inputs			Outputs	
F_SEL2	F_SEL1	F_SEL0	QA0, nQA0:QA1, nQA1	QB0, nQB0
0	0	0	÷2 (default)	÷2 (default)
1	0	0	÷5	÷2
0	1	0	÷4	÷2
1	1	0	÷2	÷4
0	0	1	÷2	÷5
1	0	1	÷5	÷4
0	1	1	÷4	÷5
1	1	1	÷4	÷4

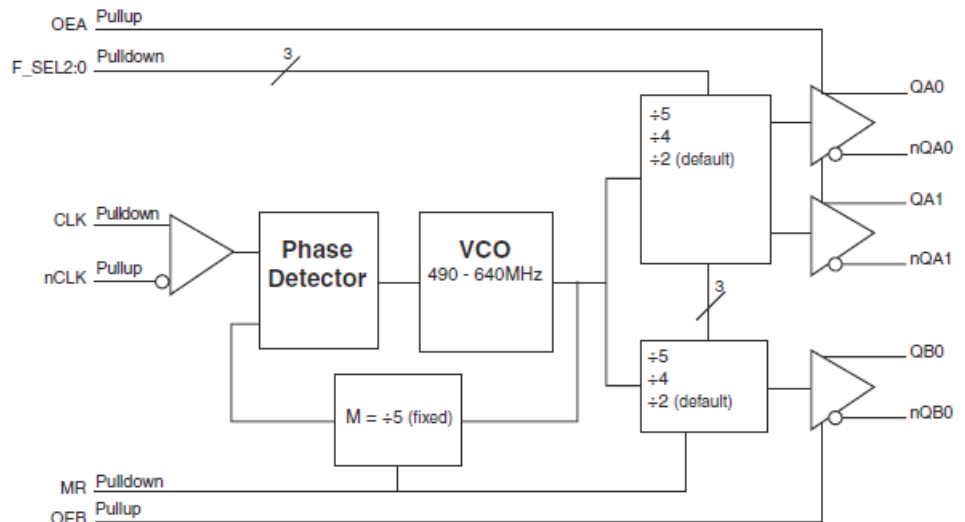
### BLOCK DIAGRAM

### PIN ASSIGNMENT

QA1	1	20	nQA1
VDD0	2	19	VDD0
QA0	3	18	QB0
nQA0	4	17	nQB0
MR	5	16	F_SEL2
F_SEL0	6	15	OEB
nc	7	14	GND
VDDA	8	13	nCLK
F_SEL1	9	12	CLK
VDD	10	11	OEA

**874003DI-02**  
**20-Lead TSSOP**

6.5mm x 4.4mm x 0.92mm  
package body  
**G Package**  
Top View



**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1, 20	QA1, nQA1	Output		Differential output pair. LVDS interface levels.
2, 19	V <sub>DDO</sub>	Power		Output supply pins.
3, 4	QA0, nQA0	Output		Differential output pair. LVDS interface levels.
5	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs (Qx) to go low and the inverted outputs (nQx) to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
6, 9, 16	F_SEL0, F_SEL1, F_SEL2	Input	Pulldown	Frequency select pin for QAx/nQAx and QB0/nQB0 outputs. LVCMOS/LVTTL interface levels.
7	nc	Unused		No connect.
8	V <sub>DDA</sub>	Power		Analog supply pin.
10	V <sub>DD</sub>	Power		Core supply pin.
11	OEA	Input	Pullup	Output enable pin for QA pins. When HIGH, the QAx/nQAx outputs are active. When LOW, the QAx/nQAx outputs are in a high impedance state. LVCMOS/LVTTL interface levels.
12	CLK	Input	Pulldown	Non-inverting differential clock input.
13	nCLK	Input	Pullup	Inverting differential clock input.
14	GND	Power		Power supply ground.
15	OEB	Input	Pullup	Output enable pin for QB0 pins. When HIGH, the QB0/nQB0 outputs are active. When LOW, the QB0/nQB0 outputs are in a high impedance state. LVCMOS/LVTTL interface levels.
17, 18	nQB0, QB0	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

**TABLE 3A. OEA OUTPUT ENABLE FUNCTION TABLE**

Inputs	Outputs
OEA	QA0/nQA0, QA1/nQA1
0	High Impedance
1	Enabled

**TABLE 3B. OEB OUTPUT ENABLE FUNCTION TABLE**

Inputs	Outputs
OEB	QB0/nQB0
0	High Impedance
1	Enabled

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	73.2°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		$V_{DD} - 0.15$	3.3	$V_{DD}$	V
$V_{DDO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$	Power Supply Current				80	mA
$I_{DDA}$	Analog Supply Current				15	mA
$I_{DDO}$	Output Supply Current				75	mA

**TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$I_{IH}$	Input High Current	OEA, OEB	$V_{DD} = V_{IN} = 3.465V$		5	$\mu A$
		F_SEL0, F_SEL1 F_SEL2, MR	$V_{DD} = V_{IN} = 3.465V$		150	$\mu A$
$I_{IL}$	Input Low Current	OEA, OEB	$V_{DD} = 3.465V, V_{IN} = 0V$	-150		$\mu A$
		F_SEL0, F_SEL1 F_SEL2, MR	$V_{DD} = 3.465V, V_{IN} = 0V$	-5		$\mu A$

**TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	CLK	$V_{DD} = V_{IN} = 3.465V$		150	$\mu A$
		nCLK	$V_{DD} = V_{IN} = 3.465V$	5		$\mu A$
$I_{IL}$	Input Low Current	CLK	$V_{DD} = V_{IN} = 3.465V$		150	$\mu A$
		nCLK	$V_{DD} = V_{IN} = 3.465V$	-150		$\mu A$
$V_{PP}$	Peak-to-Peak Input Voltage; NOTE 1		0.15		1.3	V
$V_{CMB}$	Common Mode Input Voltage; NOTE 1, 2		GND + 0.5		$V_{DD} - 0.85$	V

NOTE 1:  $V_{IL}$  should not be less than -0.3V.

NOTE 2: Common mode voltage is defined as  $V_{IH}$ .

**TABLE 4D. LVDS DC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OD}$	Differential Output Voltage		275	375	485	mV
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change				50	mV
$V_{OS}$	Offset Voltage		1.2	1.35	1.5	V
$\Delta V_{OS}$	$V_{OS}$ Magnitude Change				50	mV

**TABLE 5. AC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency		98		320	MHz
$t_{jit(cc)}$	Cycle-to-Cycle Jitter, NOTE 1, 3				30	ps
$t_{sk(o)}$	Output Skew; NOTE 2				185	ps
$t_{sk(b)}$	Bank Skew; NOTE 1, 4   Bank A				65	ps
$t_r / t_f$	Output Rise/Fall Time	20% to 80%	250		700	ps
odc	Output Duty Cycle		47		53	%

$T_A$ , Ambient Temperature applied using forced air flow.

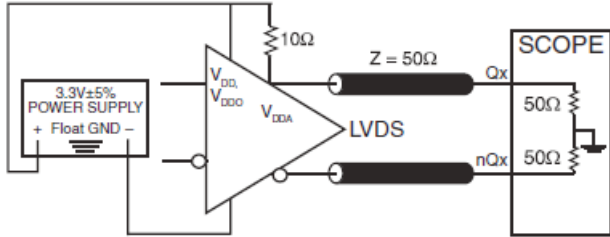
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 2: These parameters are guaranteed by characterization. Not tested in production.

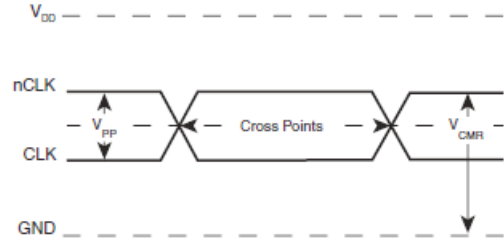
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

NOTE 4: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.

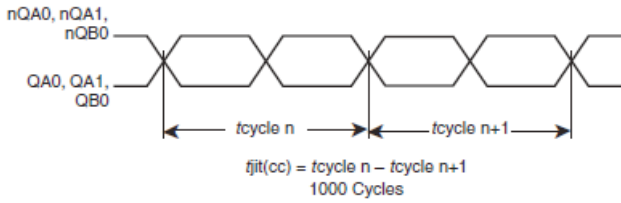
## PARAMETER MEASUREMENT INFORMATION



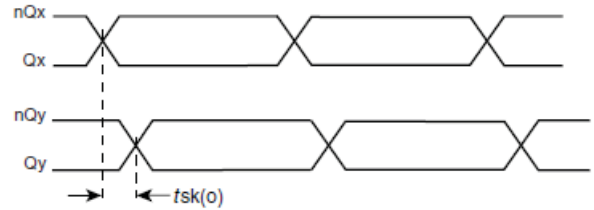
3.3V LVDS OUTPUT LOAD AC TEST CIRCUIT



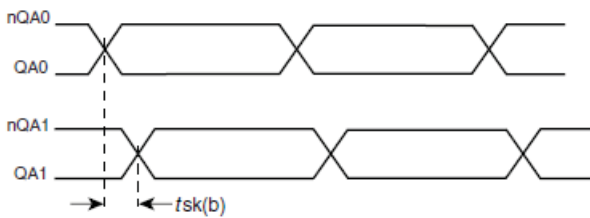
DIFFERENTIAL INPUT LEVEL



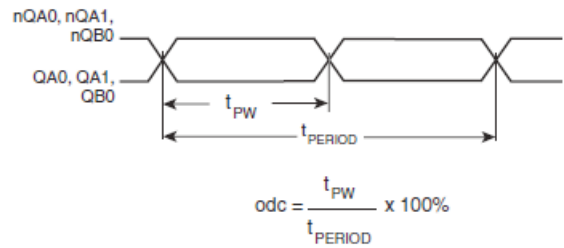
CYCLE-TO-CYCLE JITTER



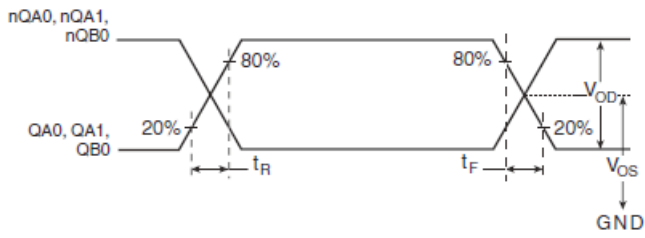
OUTPUT SKEW



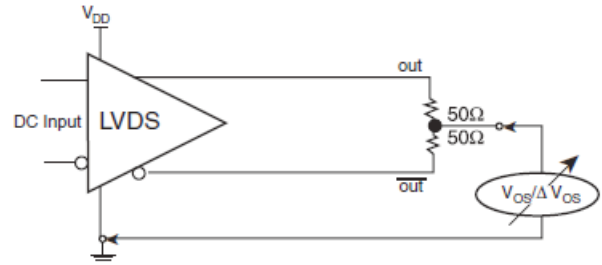
BANK SKEW



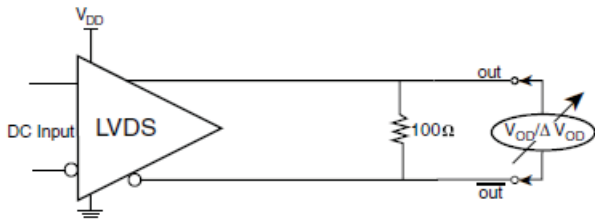
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME



OFFSET VOLTAGE SETUP



DIFFERENTIAL OUTPUT VOLTAGE SETUP

## APPLICATION INFORMATION

### POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 874003DI-02 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$ ,  $V_{DDA}$ , and  $V_{DDO}$  should be individually connected to the power supply plane through vias, and  $0.01\mu\text{F}$  bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic  $V_{DD}$  pin and also shows that  $V_{DDA}$  requires that an additional  $10\Omega$  resistor along with a  $10\mu\text{F}$  bypass capacitor be connected to the  $V_{DDA}$  pin.

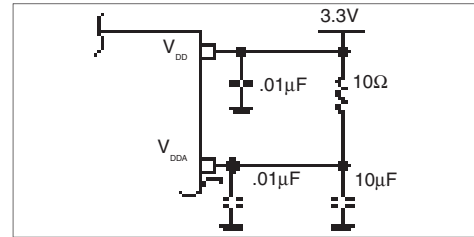


FIGURE 1. POWER SUPPLY FILTERING

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

*Figure 2* shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors  $R1$ ,  $R2$  and  $C1$ . This bias circuit should be located as close as possible to the input pin. The ratio

of  $R1$  and  $R2$  might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only  $2.5\text{V}$  and  $V_{DD} = 3.3\text{V}$ ,  $V_{REF}$  should be  $1.25\text{V}$  and  $R2/R1 = 0.609$ .

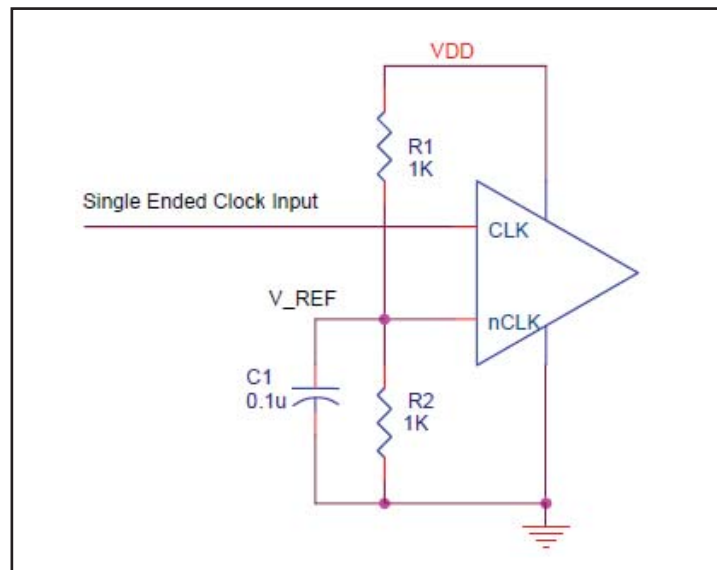
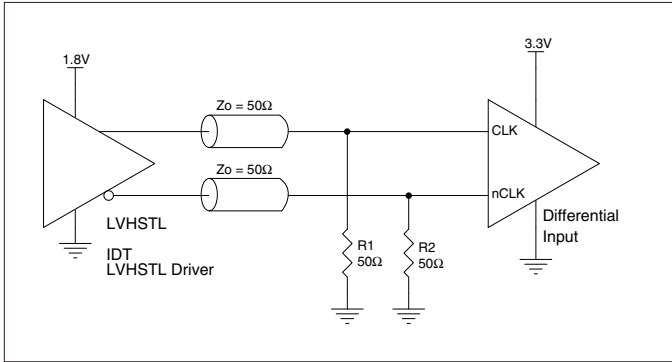


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

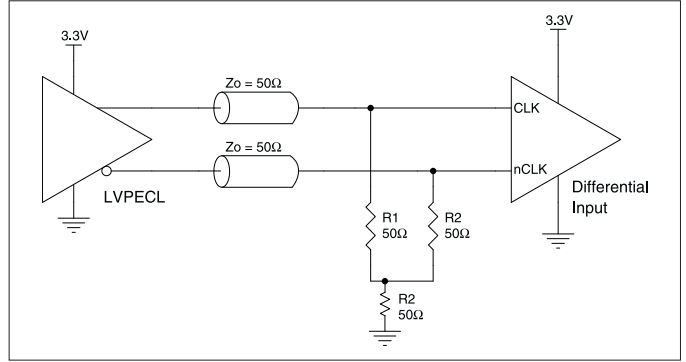
**DIFFERENTIAL CLOCK INPUT INTERFACE**

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 3A to 3F show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please

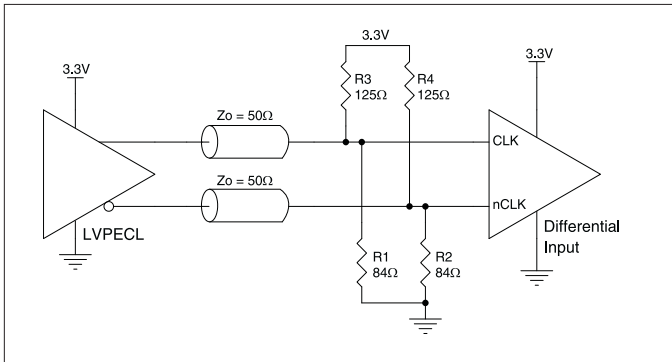
consult with the vendor of the driver component to confirm the driver termination requirements. For example in Figure 3A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



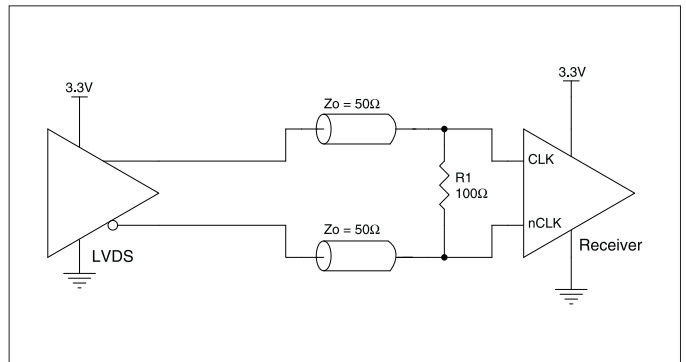
**FIGURE 3A. CLK/nCLK INPUT DRIVEN BY AN IDT OPEN EMITTER LVHSTL DRIVER**



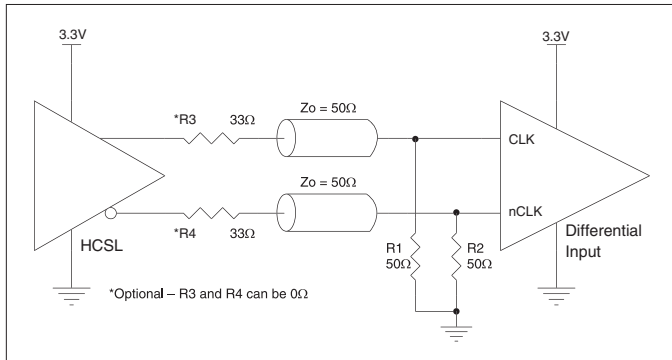
**FIGURE 3B. CLK/nCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER**



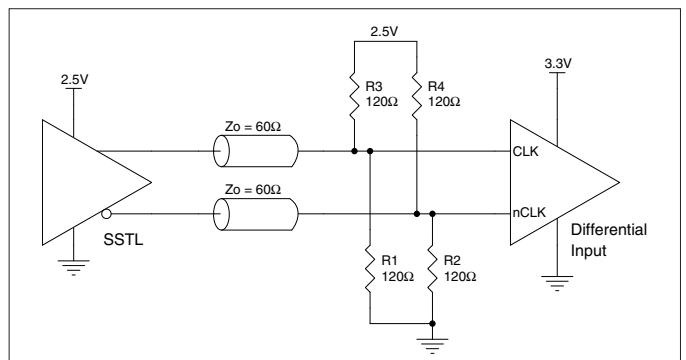
**FIGURE 3C. CLK/nCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER**



**FIGURE 3D. CLK/nCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER**



**FIGURE 3E. CLK/nCLK INPUT DRIVEN BY A 3.3V HCSL DRIVER**



**FIGURE 3F. CLK/nCLK INPUT DRIVEN BY A 2.5V SSTL DRIVER**



**RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS**

**INPUTS:  
LVCMOS CONTROL PINS**

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

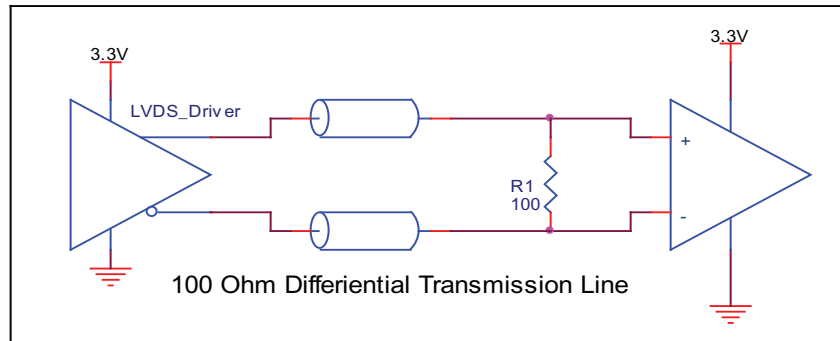
**OUTPUTS:  
LVDS OUTPUTS**

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

**LVDS DRIVER TERMINATION**

A general LVDS interface is shown in *Figure 4*. In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver

input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

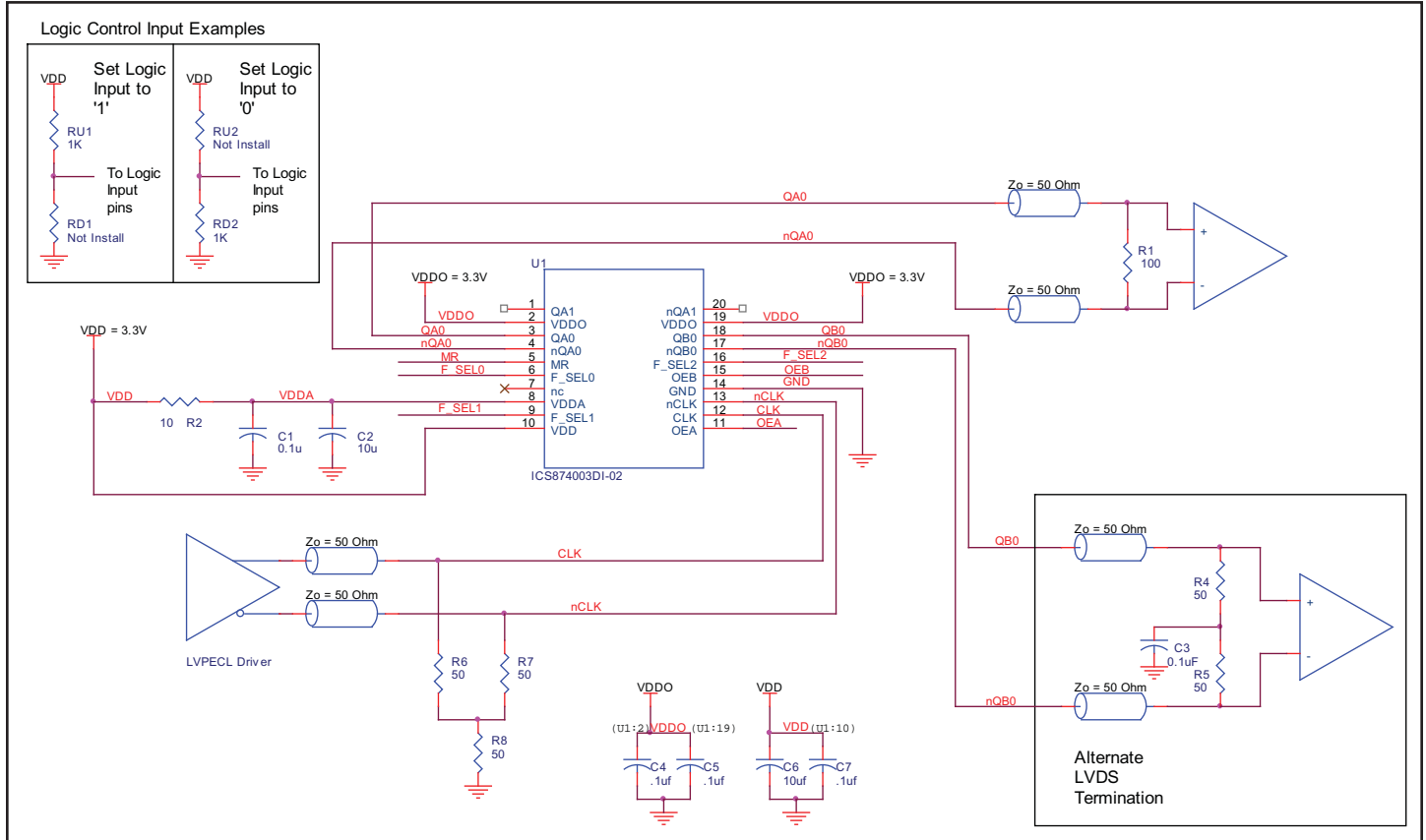


**FIGURE 4. TYPICAL LVDS DRIVER TERMINATION**

**SCHEMATIC EXAMPLE**

Figure 5 shows an example of 874003DI-02 application schematic. In this example, the device is operated at  $V_{DD} = V_{DDO} = 3.3V$ . The decoupling capacitors should be located as close as possible to

the power pin. The input is driven by a 3.3V LVPECL driver. Two examples of LVDS terminations are shown in this schematic.



**FIGURE 5. 874003DI-02 SCHEMATIC EXAMPLE**

## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 874003DI-02. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 874003DI-02 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX}) = 3.465V * (80mA + 15mA) = 329.175mW$
- Power (outputs)<sub>MAX</sub> =  $V_{DDO\_MAX} * I_{DDO\_MAX} = 3.465V * 75mA = 259.87mW$

**Total Power<sub>MAX</sub> = 329.2mW + 259.9mW = 589.1mW**

### 2. Junction Temperature.

Junction temperature, T<sub>j</sub>, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C.

The equation for T<sub>j</sub> is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

T<sub>j</sub> = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

Pd<sub>total</sub> = Total Device Power Dissipation (example calculation is in section 1 above)

T<sub>A</sub> = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below. Therefore, T<sub>j</sub> for an ambient temperature of 85°C with all outputs switching is:

$85^\circ C + 0.589W * 66.6^\circ C/W = 124.2^\circ C$ . This is below the limit of 125°C.

This calculation is only an example. T<sub>j</sub> will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 6. THERMAL RESISTANCE  $\theta_{JA}$  FOR 20-LEAD TSSOP, FORCED CONVECTION**

<b><math>\theta_{JA}</math> by Velocity (Linear Feet per Minute)</b>			
	<b>0</b>	<b>200</b>	<b>500</b>
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W
<b>NOTE:</b> Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

## RELIABILITY INFORMATION

TABLE 6.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 20 LEAD TSSOP

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for 874003DI-02 is: 1408

PACKAGE OUTLINE - G SUFFIX FOR 20 LEAD TSSOP

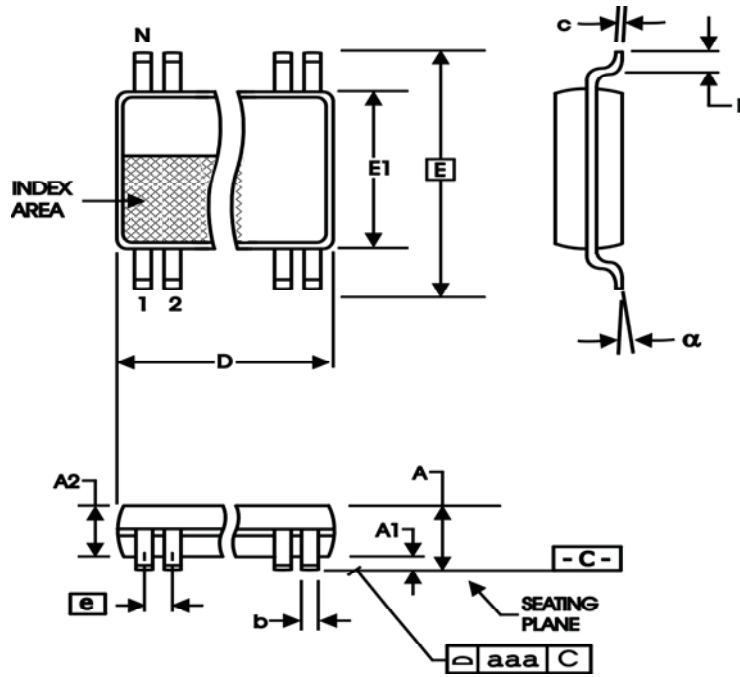


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MIN	MAX
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
$\alpha$	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

**TABLE 8. ORDERING INFORMATION**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
874003DGI-02LF	ICS4003DI02L	20 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
874003DGI-02LFT	ICS4003DI02L	20 Lead "Lead-Free" TSSOP	tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

**REVISION HISTORY**

Rev	Table	Page	Description of Change	Date
A	Funtion T	1 1 8	Corrected typo 'QA0, nQA0:QA1, nQA1'. Removed HiPerClockS logo. Removed HiPerClockS references from drawings.	5/1/13
A	T8	14	Ordering Information - removed leaded devices. Updated data sheet format.	7/17/15
A		1	Product Discontinuation Notice - Last time buy expires September 7, 2016. PDN N-16-02.	3/11/16





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