

## General Description

The ICS874003-02 is a high performance Differential-to- LVDS Jitter Attenuator designed for use in PCI Express systems. In some PCI Express systems, such as those found in desktop PCs, the PCI Express clocks are generated from a low bandwidth, high phase noise PLL frequency synthesizer. In these systems, a jitter attenuator may be required to attenuate high frequency random and deterministic jitter components from the PLL synthesizer and from the system board. The ICS874003-02 has a bandwidth of 400kHz which is designed to provide good jitter attenuation.

The ICS874003-02 uses IDT's 3<sup>RD</sup> Generation Femtoclock® PLL technology to achieve the lowest possible phase noise. The device is packaged in a 20 lead TSSOP package, making it ideal for use in space constrained applications such as PCI Express add-in cards.

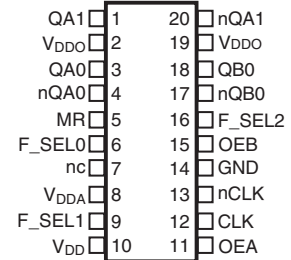
## Features

- Three differential LVDS output pairs
- One differential clock input
- CLK, nCLK supports the following input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- Input frequency range: 98MHz to 128MHz
- Output frequency range: 98MHz to 320MHz
- VCO range: 490MHz - 640MHz
- Cycle-to-cycle jitter: 35ps (maximum)
- For PCI Express Spread Spectrum Clocking support use the ICS874003-05
- Full 3.3V supply mode
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

### F\_SEL[2:0] Function Table

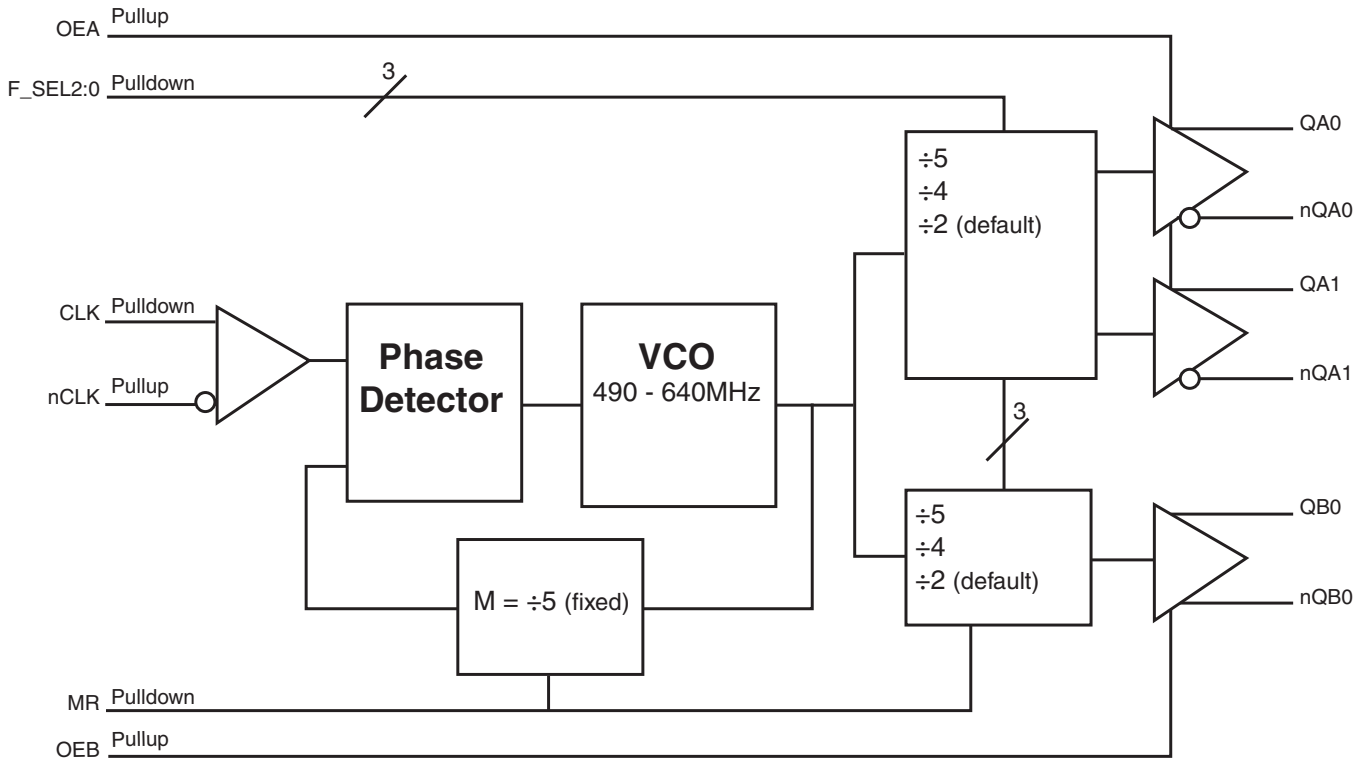
Inputs			Outputs	
F_SEL2	F_SEL1	F_SEL0	QA[0:1], nQA[0:1]	QB0, nQB0
0	0	0	÷2	÷2
1	0	0	÷5	÷2
0	1	0	÷4	÷2
1	1	0	÷2	÷4
0	0	1	÷2	÷5
1	0	1	÷5	÷4
0	1	1	÷4	÷5
1	1	1	÷4	÷4

## Pin Assignment



**ICS874003-02**  
**20-Lead TSSOP**  
**6.5mm x 4.4mm x 0.925mm package body**  
**G Package**  
**Top View**

## Block Diagram



### Table 1. Pin Descriptions

Number	Name	Type		Description
1, 20	QA1, nQA1	Output		Differential output pair. LVDS interface levels.
2, 19	V <sub>DDO</sub>	Power		Output supply pins.
3, 4	QA0, nQA0	Output		Differential output pair. LVDS interface levels.
5	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs (Qx) to go low and the inverted outputs (nQx) to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
6, 9, 16	F_SEL0, F_SEL1, F_SEL2	Input	Pulldown	Frequency select pin for QAx, nQAx and QB0, nQB0 outputs. LVCMOS/LVTTL interface levels.
7	nc	Unused		No connect.
8	V <sub>DDA</sub>	Power		Analog supply pin.
10	V <sub>DD</sub>	Power		Core supply pin.
11	OEA	Input	Pullup	Output enable pin for QA pins. When HIGH, the QAx, nQAx outputs are active. When LOW, the QAx, nQAx outputs are in a high impedance state. LVCMOS/LVTTL interface levels.
12	CLK	Input	Pulldown	Non-inverting differential clock input.
13	nCLK	Input	Pullup	Inverting differential clock input.
14	GND	Power		Power supply ground.
15	OEB	Input	Pullup	Output enable pin for QB0 pins. When HIGH, the QB0, nQB0 outputs are active. When LOW, the QB0, nQB0 outputs are in a high impedance state. LVCMOS/LVTTL interface levels.
17, 18	nQB0, QB0	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

### Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

## Function Table

### Table 3. Output Enable Function Table

Inputs		Outputs	
OEA	OEB	QA[0:1], nQA[0:1]	QB0, nQB0
0	0	Hi-Impedance	Hi-Impedance
1	1	Enabled	Enabled

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $I_O$ Continuous Current Surge Current	10mA 15mA
Package Thermal Impedance, $\theta_{JA}$	73.2°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 4A. LVDS Power Supply DC Characteristics,  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		$V_{DD} - 0.12$	3.3	$V_{DD}$	V
$V_{DDO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$	Power Supply Current				75	mA
$I_{DDA}$	Analog Supply Current				12	mA
$I_{DDO}$	Output Supply Current				75	mA

**Table 4B. LVCMOS/LVTTL DC Characteristics,  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$I_{IH}$	Input High Current	OEA, OEB	$V_{DD} = V_{IN} = 3.465V$		5	$\mu A$
		F_SEL0, F_SEL1, F_SEL2, MR	$V_{DD} = V_{IN} = 3.465V$		150	$\mu A$
$I_{IL}$	Input Low Current	OEA, OEB	$V_{DD} = 3.465V, V_{IN} = 0V$	-150		$\mu A$
		F_SEL0, F_SEL1, F_SEL2, MR	$V_{DD} = 3.465V, V_{IN} = 0V$	-5		$\mu A$

**Table 4C. Differential DC Characteristics,  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	CLK	$V_{DD} = V_{IN} = 3.465V$		150	$\mu A$
		nCLK	$V_{DD} = V_{IN} = 3.465V$		5	$\mu A$
$I_{IL}$	Input Low Current	CLK	$V_{DD} = 3.465V, V_{IN} = 0V$	-5		$\mu A$
		nCLK	$V_{DD} = 3.465V, V_{IN} = 0V$	-150		$\mu A$
$V_{PP}$	Peak-to-Peak Voltage; NOTE 1		0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2		GND + 0.5		$V_{DD} - 0.85$	V

NOTE 1:  $V_{IL}$  should not be less than -0.3V.

NOTE 2: Common mode input voltage is defined as  $V_{IH}$ .

**Table 4D. LVDS DC Characteristics,  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OD}$	Differential Output Voltage		275	375	485	mV
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change				50	mV
$V_{OS}$	Offset Voltage		1.2	1.35	1.5	V
$\Delta V_{OS}$	$V_{OS}$ Magnitude Change				50	mV

**Table 5. AC Characteristics,  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency		98		320	MHz
$\overline{t}_{jit(cc)}$	Cycle-to-Cycle Jitter; NOTE 1				35	ps
$t_{sk(o)}$	Output Skew; NOTE 2, 3				145	ps
$t_{sk(b)}$	Bank Skew; NOTE 1, 4	Bank A			55	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	275		725	ps
odc	Output Duty Cycle		47		53	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

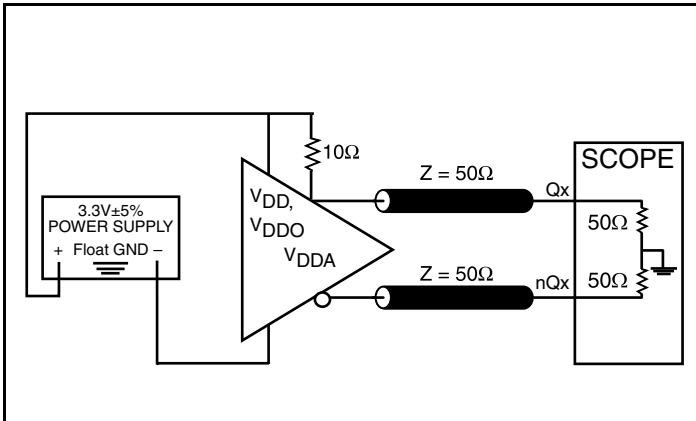
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

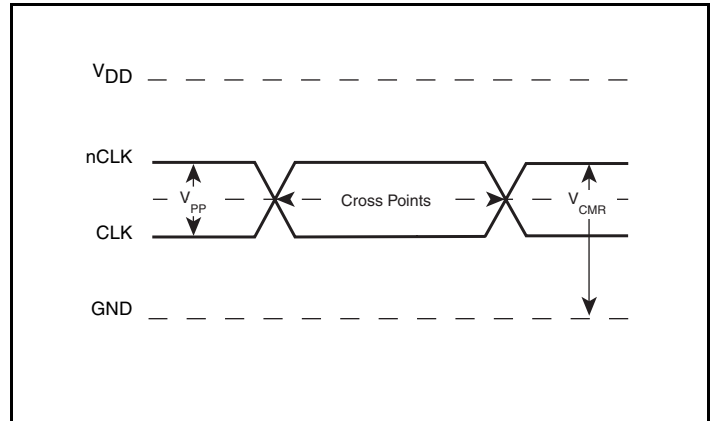
NOTE 3: These parameters are guaranteed by characterization. Not tested in production.

NOTE 4: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.

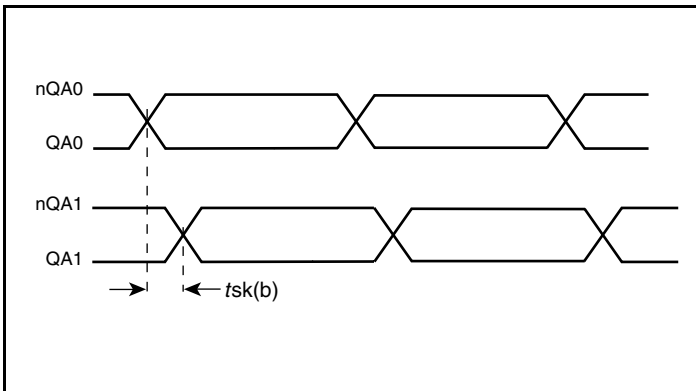
## Parameter Measurement Information



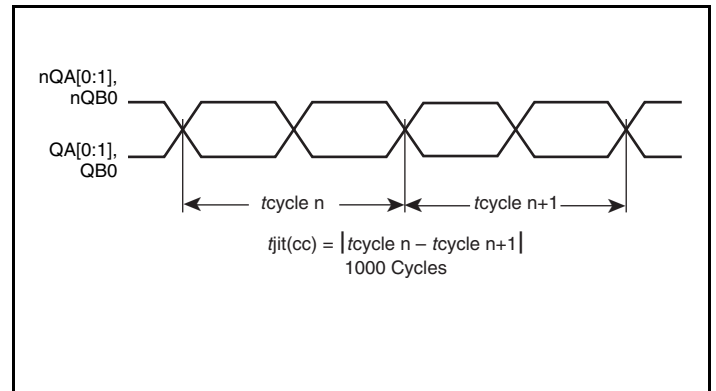
3.3V LVDS Output Load AC Test Circuit



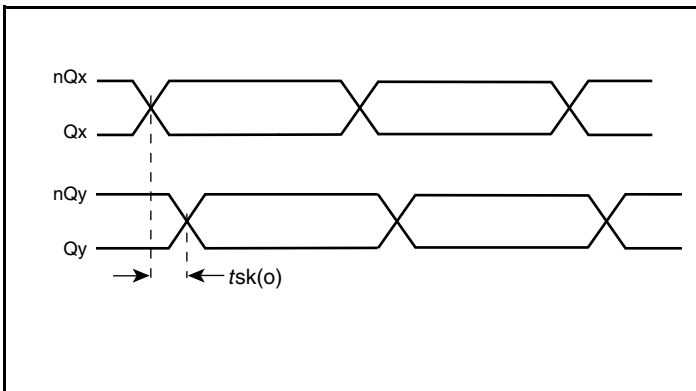
Differential Input Level



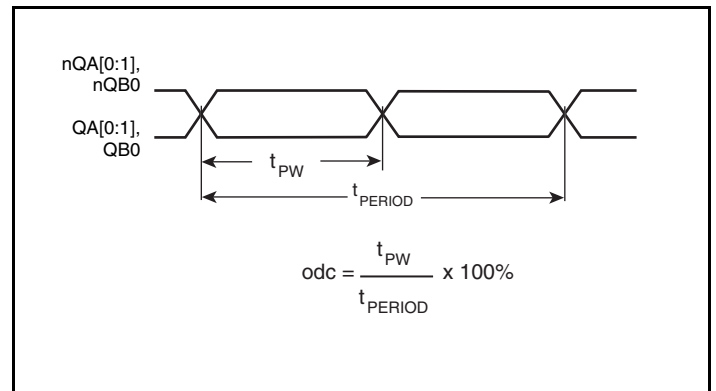
Bank Skew



Cycle-to-Cycle Jitter

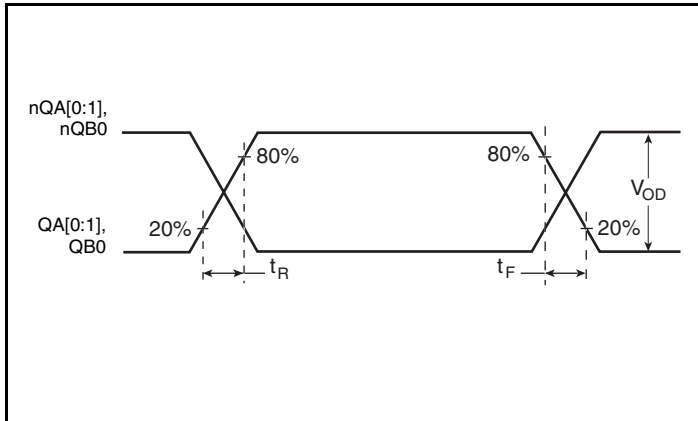


Output Skew

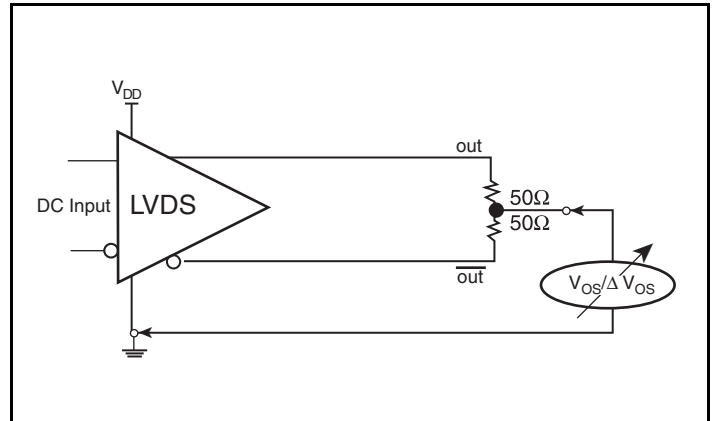


Output Duty Cycle/Pulse Width/Period

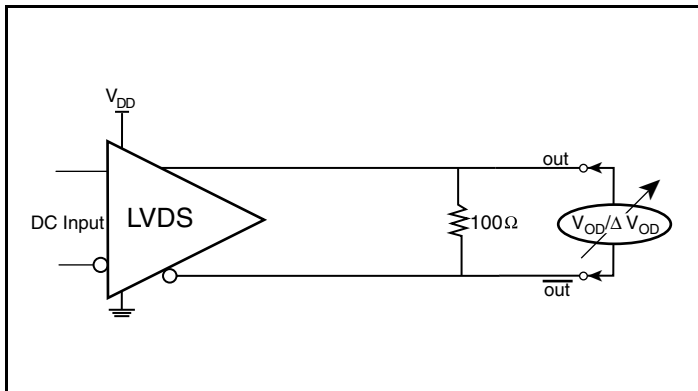
Parameter Measurement Information, continued



Output Rise/Fall Time



Offset Voltage Setup



Differential Output Voltage Setup

## Applications Information

### Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS874003-02 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$ ,  $V_{DDA}$  and  $V_{DDO}$  should be individually connected to the power supply plane through vias, and  $0.01\mu\text{F}$  bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic  $V_{DD}$  pin and also shows that  $V_{DDA}$  requires that an additional  $10\Omega$  resistor along with a  $10\mu\text{F}$  bypass capacitor be connected to the  $V_{DDA}$  pin.

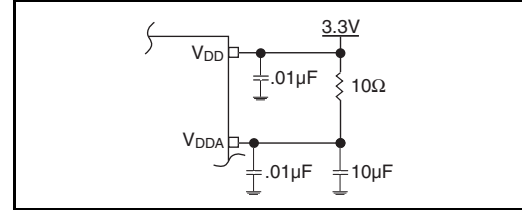


Figure 1. Power Supply Filtering

### Wiring the Differential Input to Accept Single-Ended Levels

*Figure 1* shows how a differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors  $R1$  and  $R2$ . The bypass capacitor ( $C1$ ) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of  $R1$  and  $R2$  might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is  $2.5\text{V}$  and  $V_{DD} = 3.3\text{V}$ ,  $R1$  and  $R2$  value should be adjusted to set  $V_{REF}$  at  $1.25\text{V}$ . The values below are for when both the single ended swing and  $V_{DD}$  are at the same voltage. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First,  $R3$  and  $R4$  in parallel should equal the transmission

line impedance. For most  $50\Omega$  applications,  $R3$  and  $R4$  can be  $100\Omega$ . The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however  $V_{IL}$  cannot be less than  $-0.3\text{V}$  and  $V_{IH}$  cannot be more than  $V_{DD} + 0.3\text{V}$ . Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

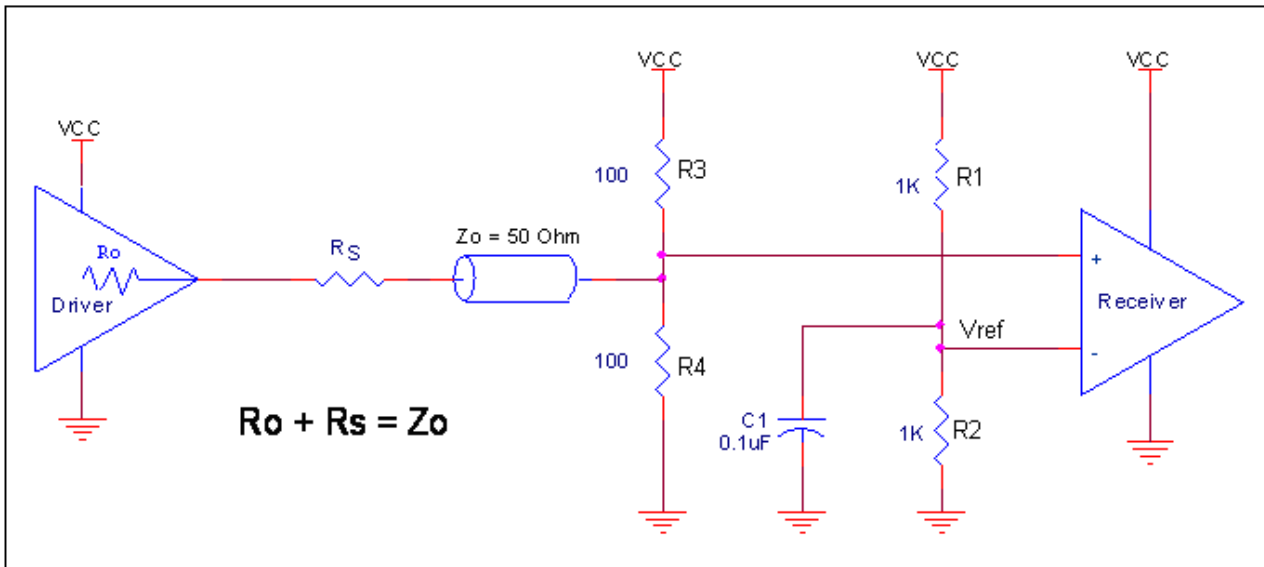


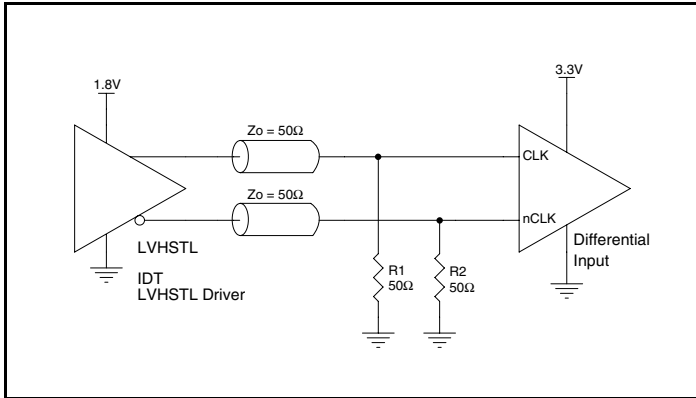
Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels



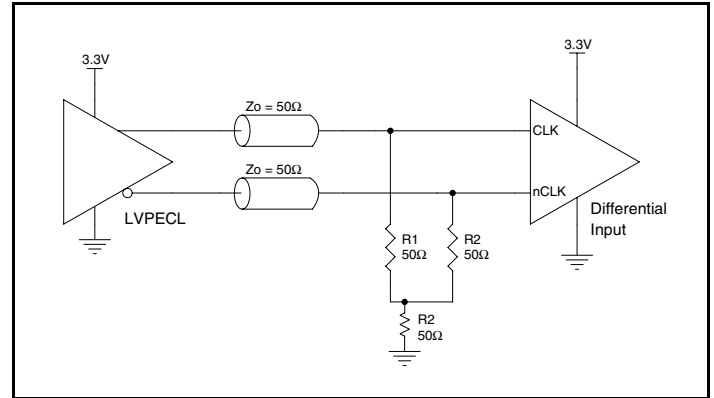
## Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. The differential signal must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 3A to 3F show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

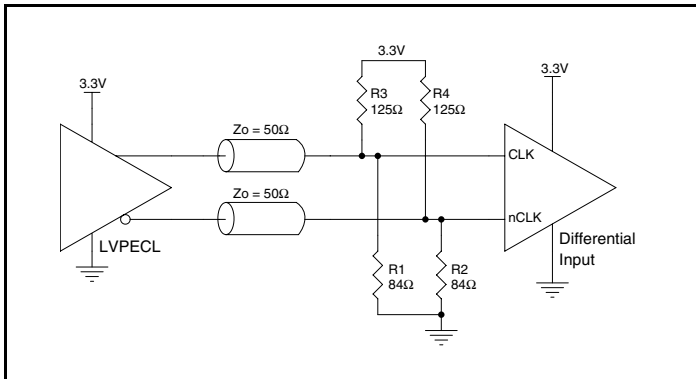
Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



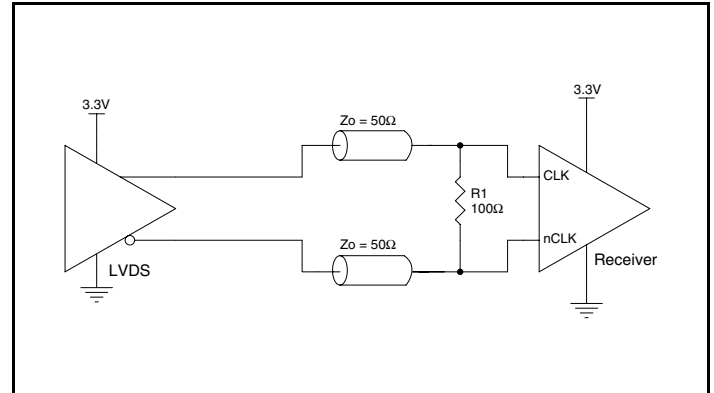
**Figure 3A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver**



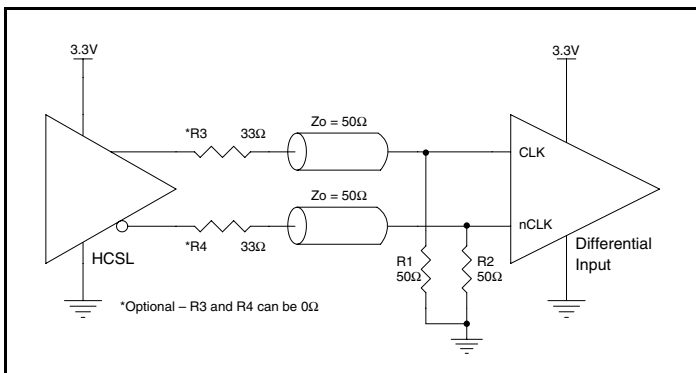
**Figure 3B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



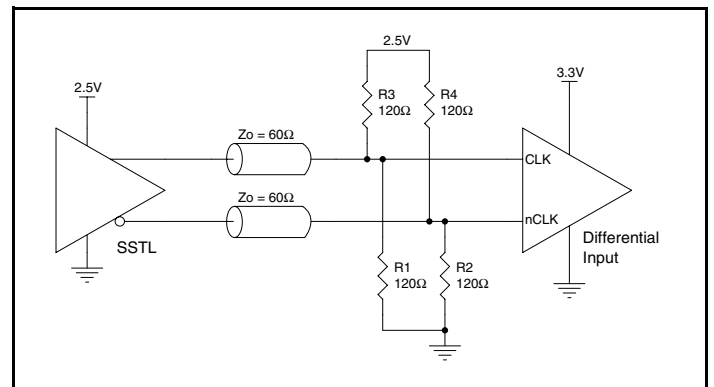
**Figure 3C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



**Figure 3D. CLK/nCLK Input Driven by a 3.3V LVDS Driver**



**Figure 3E. CLK/nCLK Input Driven by a 3.3V HCSL Driver**



**Figure 3F. CLK/nCLK Input Driven by a 2.5V SSTL Driver**

## Recommendations for Unused Input and Output Pins

### Inputs:

#### LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

### Outputs:

#### LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100 $\Omega$  across. If they are left floating, there should be no trace attached.

## LVDS Driver Termination

A general LVDS interface is shown in *Figure 4*. Standard termination for LVDS type output structure requires both a 100 $\Omega$  parallel resistor at the receiver and a 100 $\Omega$  differential transmission line environment. In order to avoid any transmission line reflection issues, the 100 $\Omega$  resistor must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard

termination schematic as shown in Figure 4 can be used with either type of output structure. If using a non-standard termination, it is recommended to contact IDT and confirm if the output is a current source or a voltage source type structure. In addition, since these outputs are LVDS compatible, the amplitude and common mode input range of the input receivers should be verified for compatibility with the output.

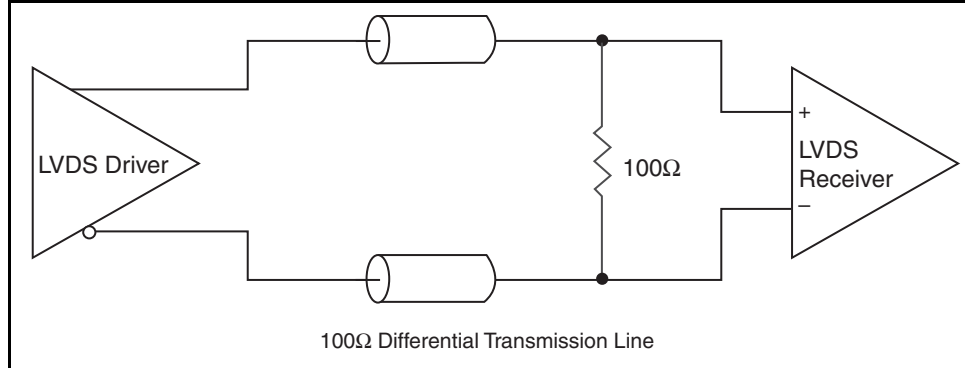


Figure 4. Typical LVDS Driver Termination

## Power Considerations

This section provides information on power dissipation and junction temperature for the ICS874003-02. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS74003-02 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX}) = 3.465V * (75mA + 12mA) = \mathbf{301.45mW}$
- Power (outputs)<sub>MAX</sub> =  $V_{DDO\_MAX} * I_{DDO\_MAX} = 3.465V * 75mA = \mathbf{259.87mW}$

**Total Power<sub>MAX</sub> = 301.45mW + 259.87mW = 561.32mW**

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### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ\text{C} + 0.561\text{W} * 66.6^\circ\text{C/W} = 107.3^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 6. Thermal Resistance  $\theta_{JA}$  for 20 Lead TSSOP, Forced Convection**

Linear Feet per Minute	$\theta_{JA}$ by Velocity		
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

## Reliability Information

Table 7.  $\theta_{JA}$  vs. Air Flow Table for a 20 Lead TSSOP

$\theta_{JA}$ by Velocity			
Linear Feet per Minute	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

## Transistor Count

The transistor count for ICS874003-02 is: 1408

## Package Outline and Package Dimensions

Package Outline - G Suffix for 20 Lead TSSOP

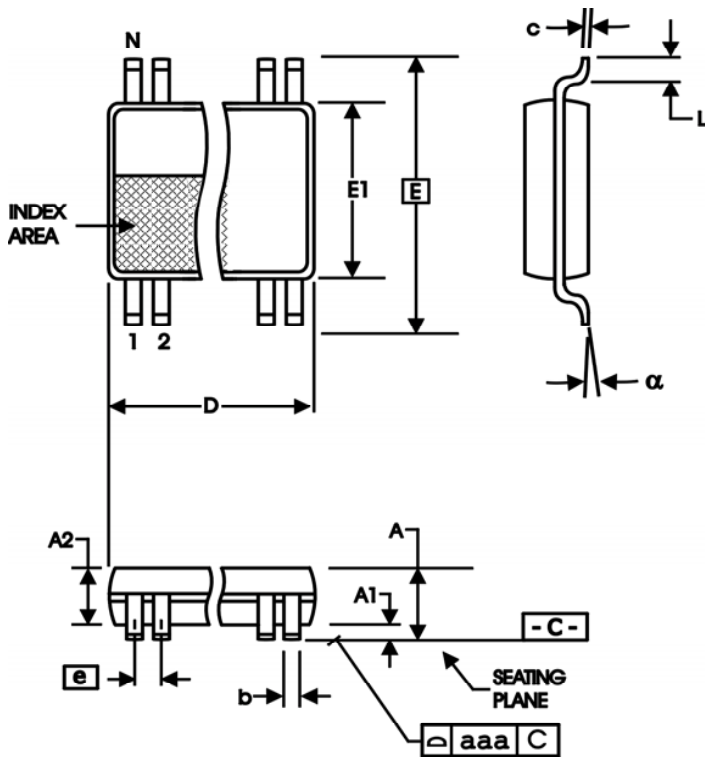


Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	20	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
$\alpha$	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

## Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
874003AG-02	ICS874003A02	20 Lead TSSOP	Tube	0°C to 70°C
874003AG-02T	ICS874003A02	20 Lead TSSOP	2500 Tape & Reel	0°C to 70°C
874003AG-02LF	ICS74003A02L	"Lead-Free" 20 Lead TSSOP	Tube	0°C to 70°C
874003AG-02LFT	ICS74003A02L	"Lead-Free" 20 Lead TSSOP	2500 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

## Revision History Sheet

Rev	Table	Page	Description of Change	Date
B		1	Updated General Description and Features section.	9/14/10
	T1	3	Pin Description Table - corrected MR description	
	T4C	5	Differential DC Characteristics Table - updated notes. Added Units to I <sub>IH</sub> /I <sub>IL</sub> rows.	
	T5	5	Corrected I <sub>IH</sub> (nCLK) spec from 5uA min to 5uA max. Corrected I <sub>IL</sub> CLK from 150uA max to -5uA min.	
		5	AC Characteristics Table - added thermal note, corrected NOTE 2.	
		6 - 7	Parameter Measurement Information - corrected Bank Skew labels, corrected Output Rise/Fall Time diagram.	
		8	Updated <i>Wiring the Differential Input to Accept Single-ended Levels</i> .	
		9	Updated <i>Differential Clock Input Interface</i> .	
		10	Updated <i>LVDS Driver Termination</i> .	
		13	Ordering Information Table - deleted "ICS" prefix in Part/Order column, added "ICS" prefix to marking column. Converted datasheet format.	



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(Rev.1.0 Mar 2020)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

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