700MHz, Differential-to-3.3V LVPECL Zero Delay Clock Generator

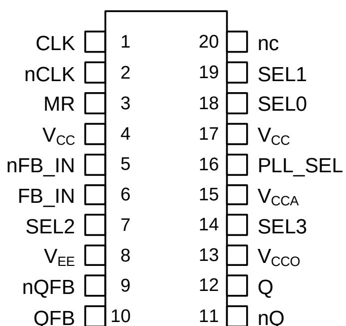
General Description

The 8735BI-21 is a highly versatile 1:1 Differential-to-3.3V LVPECL clock generator. The CLK, nCLK pair can accept most standard differential input levels. The 8735BI-21 has a fully integrated PLL and can be configured as zero delay buffer, multiplier or divider, and has an output frequency range of 31.25MHz to 700MHz. The reference divider, feedback divider and output divider are each programmable, thereby allowing for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8. The external feedback allows the device to achieve “zero delay” between the input clock and the output clocks. The PLL_SEL pin can be used to bypass the PLL for system test and debug purposes. In bypass mode, the reference clock is routed around the PLL and into the internal output dividers.

Features

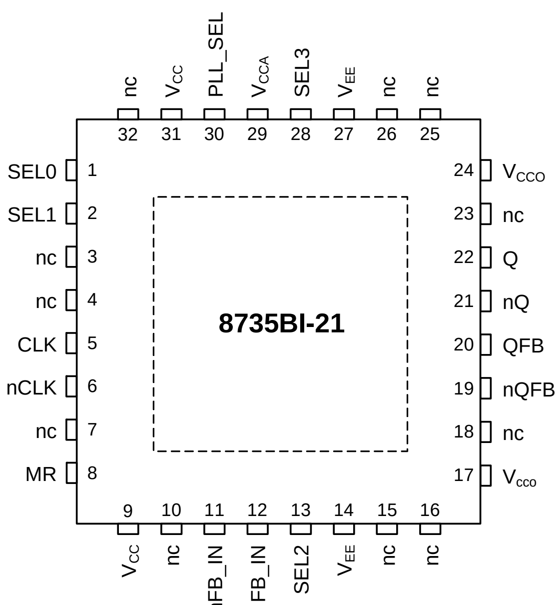
- One differential 3.3V LVPECL output pair, one differential feedback output pair
- Differential CLK, nCLK input pair
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, HCSL
- Output frequency range: 31.25MHz to 700MHz
- Input frequency range: 31.25MHz to 700MHz
- VCO range: 250MHz to 700MHz
- Programmable dividers allow for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8
- External feedback for “zero delay” clock regeneration with configurable frequencies
- Cycle-to-cycle jitter: 50ps (maximum)
- 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Available in RoHS compliant package

Pin Assignment



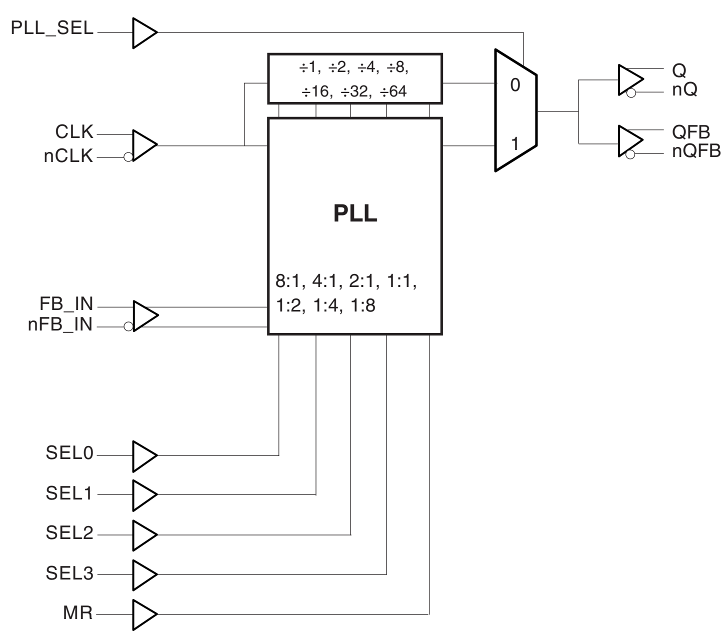
8735BI-21

20-pin, 7.5mm x 12.8mm X 2.3MM SOIC Package



32-pin, 5mm x 5mm X 0.925MM VFQFN Package

Block Diagram



Pin Descriptions and Characteristics

Table 1. Pin Descriptions[1]

Name	Type		Description
CLK	Input	Pulldown	Non-inverting differential clock input.
nCLK	Input	Pullup	Inverting differential clock input.
nFB_IN	Input	Pullup	Feedback input to phase detector for regenerating clocks with “zero delay”. Connect to nQFB.
FB_IN	Input	Pulldown	Feedback input to phase detector for regenerating clocks with “zero delay”. Connect to QFB.
MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Q and QFB to go low and the inverted outputs nQ and nQFB to go high. When LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
SEL0, SEL1, SEL2, SEL3	Input	Pulldown	Determines output divider values in Table 3. LVCMOS / LVTTL interface levels.
PLL_SEL	Input	Pullup	Selects between the PLL and reference clock as the input to the dividers. When LOW, selects reference clock. When HIGH, selects PLL. LVCMOS / LVTTL interface levels.
nQ, Q	Output		Differential feedback outputs. LVPECL interface levels.
nQFB, QFB	Output		Differential feedback outputs. LVPECL interface levels.
V_{EE}	Power		Negative supply.
V_{CC}	Power		Core supply.
V_{CCA}	Power		Analog supply.
V_{CCO}	Power		Output supply.

NOTE 1: *Pullup* and *Pulldown* refer to internal input resistors. See *Table 2*, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	IN, nIN		4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Table 3A. Control Input Function Table[1]

Inputs					Outputs PLL_SEL = 1 PLL Enable Mode
SEL3	SEL2	SEL1	SEL0	Reference Frequency Range (MHz)	Q, nQ; QFB, nQFB
0	0	0	0	250-700	÷ 1 (default)
0	0	0	1	125 - 350	÷ 1
0	0	1	0	62.5 - 175	÷ 1
0	0	1	1	31.25 - 87.5	÷ 1
0	1	0	0	250 - 700	÷ 2
0	1	0	1	125 - 350	÷ 2
0	1	1	0	62.5 - 175	÷ 2
0	1	1	1	250 - 700	÷ 4
1	0	0	0	125 - 350	÷ 4
1	0	0	1	250 - 700	÷ 8
1	0	1	0	125 - 350	x 2
1	0	1	1	62.5 - 175	x 2
1	1	0	0	31.25 - 87.5	x 2
1	1	0	1	62.5 - 175	x 4
1	1	1	0	31.25 - 87.5	x 4
1	1	1	1	31.25 - 87.5	x 8

NOTE 1: VCO frequency range for all configurations above is 250MHz to 700MHz.

Table 3B. PLL Bypass Function Table[1]

Inputs				Outputs PLL_SEL = 0 PLL Bypass Mode
SEL3	SEL2	SEL1	SEL0	Q, nQ; QFB, nQFB
0	0	0	0	÷ 4 (default)
0	0	0	1	÷ 4
0	0	1	0	÷ 4
0	0	1	1	÷ 8
0	1	0	0	÷ 8
0	1	0	1	÷ 8
0	1	1	0	÷ 16
0	1	1	1	÷ 16
1	0	0	0	÷ 32
1	0	0	1	÷ 64
1	0	1	0	÷ 2
1	0	1	1	÷ 2
1	1	0	0	÷ 4
1	1	0	1	÷ 1
1	1	1	0	÷ 2
1	1	1	1	÷ 1

NOTE 1: VCO frequency range for all configurations above is 250MHz to 700MHz.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Electrical Characteristics"* or *AC Electrical Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC_X}	4.6V
Inputs, V_{CC}	-0.5V to V_{CC} + 0.5V
Outputs, V_{CCO}	-0.5V to V_{CCO} + 0.5V
Junction Temperature, T_J	125°C
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				155	mA
I_{CCA}	Analog Supply Current				17	mA

Table 4B. LVCMOS/LVTTL Input DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

<table>
<tr><th>Symbol</th><th colspan="2">Parameter</th><th>Test Conditions</th><th>Minimum</th><th>Typical</th><th>Maximum</th><th>Units</th></tr>
<tr><td>V_{IH}</td><td colspan="2">Input High Voltage</td><td></td><td>2</td><td></td><td>V_{CC} + 0.3</td><td>V</td></tr>
<tr><td>V_{IL}</td><td colspan="2">Input Low Voltage</td><td></td><td>-0.3</td><td></td><td>0.8</td><td>V</td></tr>
<tr><td rowspan="2">I_{IH}</td><td rowspan="2">Input High Current</td><td>SEL0, SEL1, SEL2, SEL3, MR</td><td>$V_{CC} = V_{IN} = 3.465V$</td><td></td><td></td><td>150</td><td>µA</td></tr>
<tr><td>PLL_SEL</td><td>$V_{CC} = V_{IN} = 3.465V$</td><td></td><td></td><td>5</td><td>µA</td></tr>
<tr><td rowspan="2">I_{IL}</td><td rowspan="2">Input Low Current</td><td>SEL0, SEL1, SEL2, SEL3, MR</td><td>$V_{CC} = 3.465V$, $V_{IN} = 0V$</td><td>-5</td><td></td><td></td><td>µA</td></tr>
<tr><td>PLL_SEL</td><td>$V_{CC} = 3.465V$, $V_{IN} = 0V$</td><td>-150</td><td></td><td></td><td>µA</td></tr>
</table>

Table 4C. Differential Input DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, FB_IN	$V_{CC} = V_{IN} = 3.465V$			150	µA
		nCLK, nFB_IN	$V_{CC} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	CLK, FB_IN	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-5			µA
		nCLK, nFB_IN	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{PP}	Peak-to-Peak Voltage[1]			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage[2, 3]			V_{EE} + 0.5V		V_{CC} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.

NOTE 2: Common mode input voltage is defined as V_{IH}.

NOTE 3: For single ended applications, the maximum input voltage for CLK, nCLK is V_{CC} + 0.3V.

Table 4D. LVPECL DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage[1]		V_{CCO} – 1.4		V_{CCO} – 0.9	V
V_{OL}	Output Low Voltage[1]		V_{CCO} – 2.1		V_{CCO} – 1.7	V
V_{SWING}	Peak-to-Peak Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO} – 2V.

Table 5. Input Frequency Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, T_A = 0°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	CLK, nCLK	PLL_SEL = 1	31.25		700	MHz
			PLL_SEL = 0			700	MHz

AC Electrical Characteristics

Table 6. Input Frequency Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $T_A = 0°C$ to $85°C$[1]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				700	MHz
t_{PD}	Propagation Delay[2]	PLL_SEL = 0V, f ≤ 700MHz	2.8		4.9	ns
$t$sk(o)	Output Skew[3, 4]	PLL_SEL = 0V			35	ps
t(Ø)	Static Phase Offset[4, 5]	PLL_SEL = 3.3V	-100		200	ps
$t$jit(cc)	Cycle-to-Cycle Jitter[4, 6]				50	ps
$t$jit(θ)	Phase Jitter[4, 6, 7]				±80	ps
t_L	PLL Lock Time				1	ms
t_R / t_F	Output Rise/Fall Time	20% to 80% @ 50MHz	200		700	ps
odc	Output Duty Cycle	f_{OUT} ≤ 250MHz	47		53	%

NOTE 1: All parameters measured at f_{OUT} unless noted otherwise.

NOTE 2: Measured from the differential input crosspoint to the differential output crosspoint.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential crosspoint.

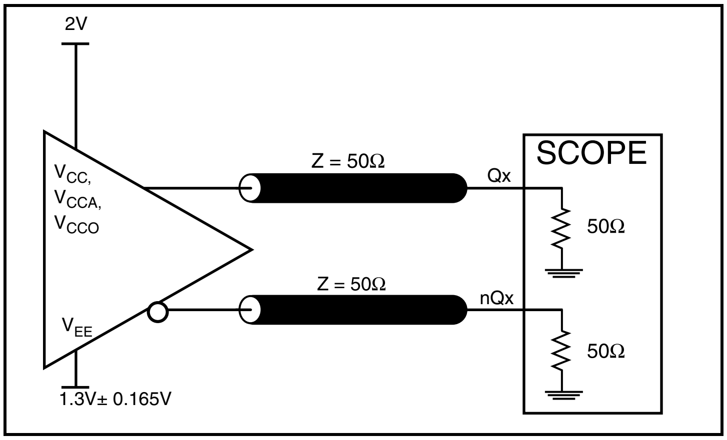
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 5: Defined as the time difference between the input reference clock and the averaged feedback input signal across all conditions, when the PLL is locked and the input reference frequency is stable.

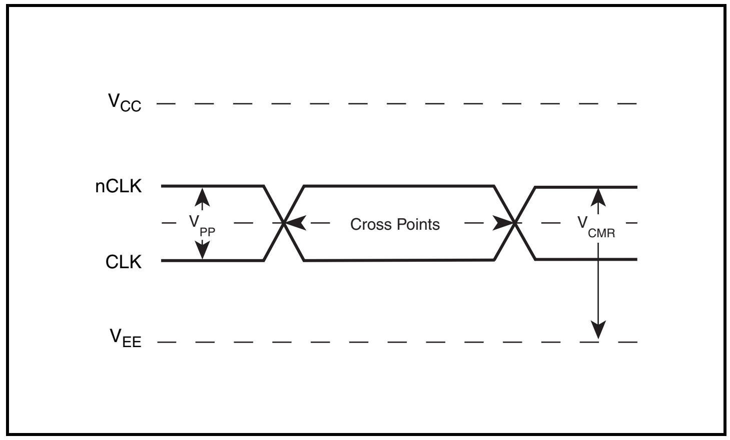
NOTE 6: Characterized at VCO frequency of 622MHz,.

NOTE 7: Phase jitter is dependent on the input source used.

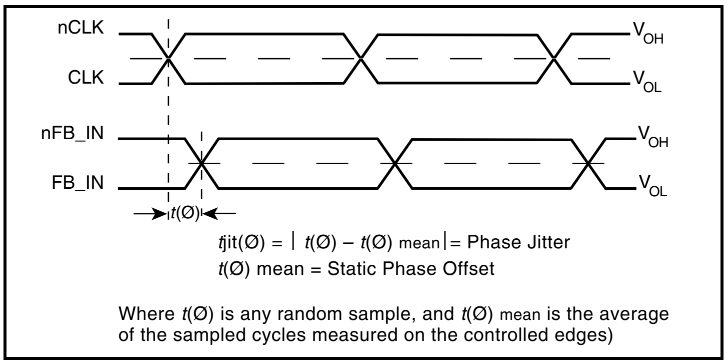
Parameter Measurement Information



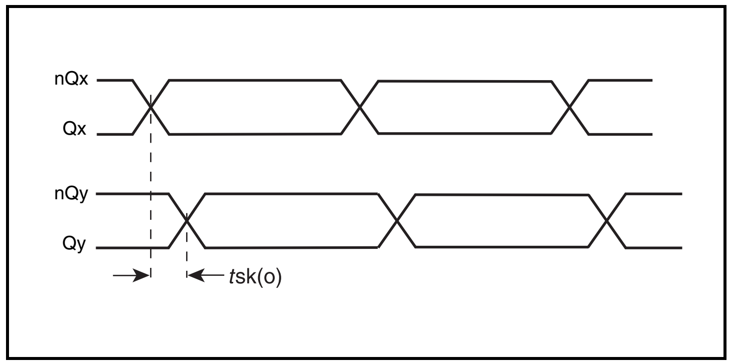
3.3V Output Load Test Circuit



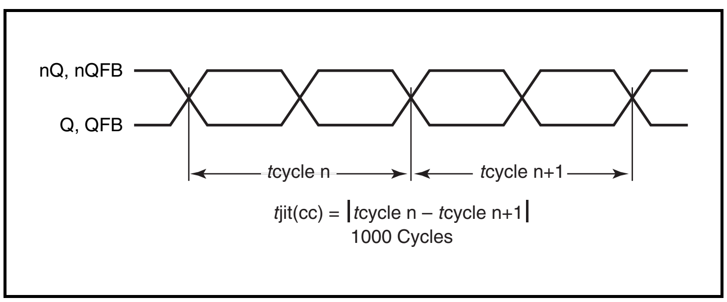
Differential Input Level



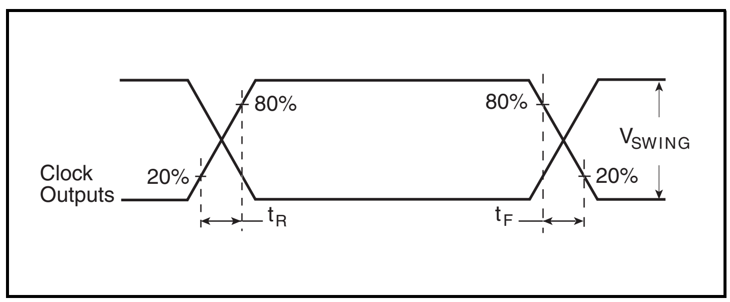
Phase Jitter and Static Phase Offset



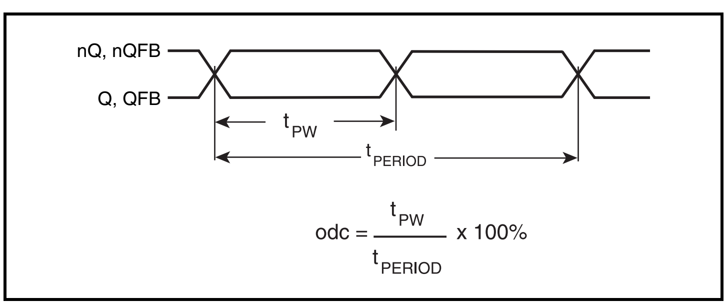
Output Skew



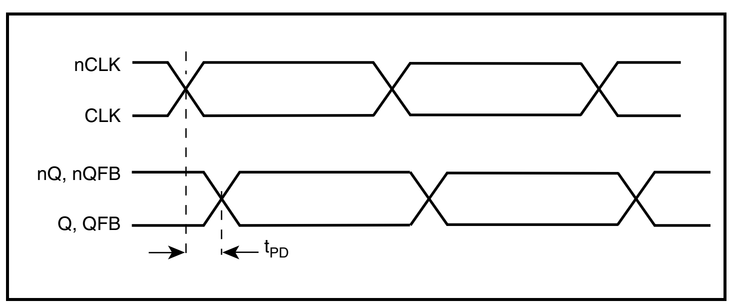
Cycle-to-Cycle Jitter



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period



Propagation Delay

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Suggested edge rate faster than 1V/ns. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

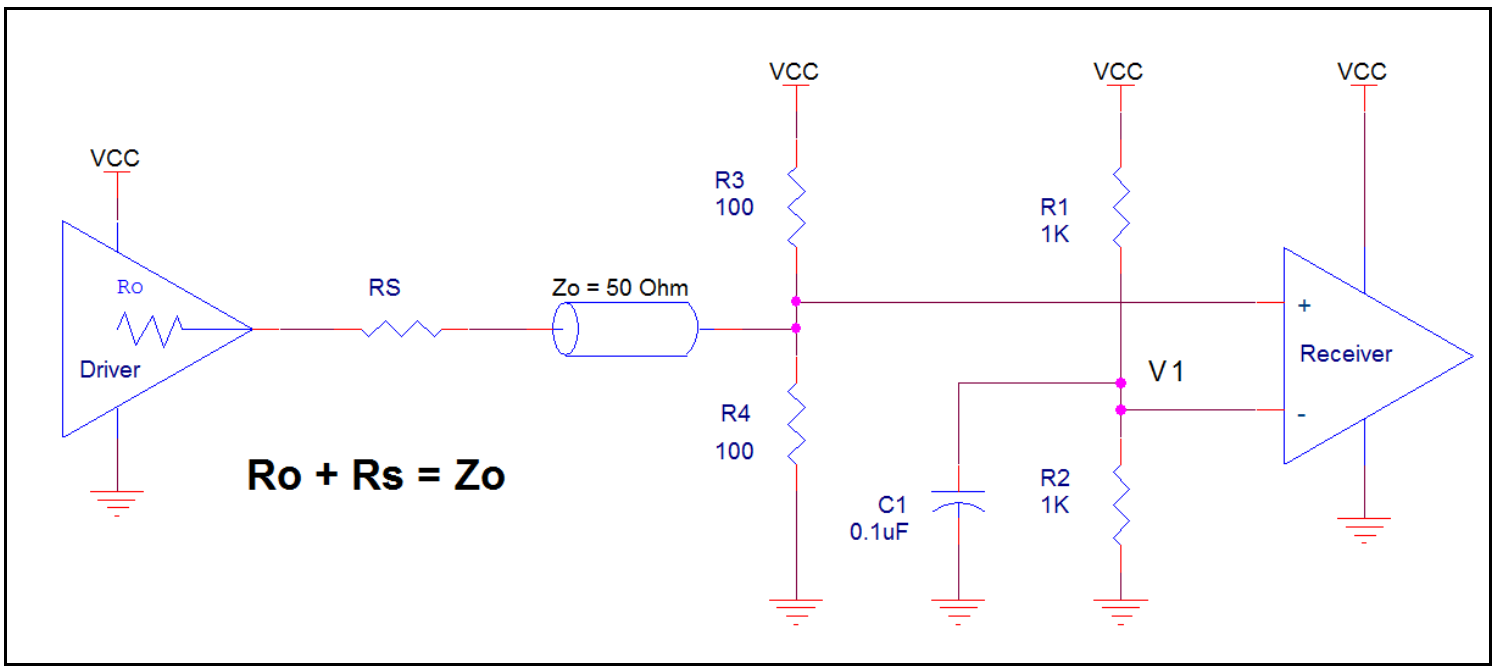


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

3.3V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figure 2A to Figure 2E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in *Figure 2A*, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

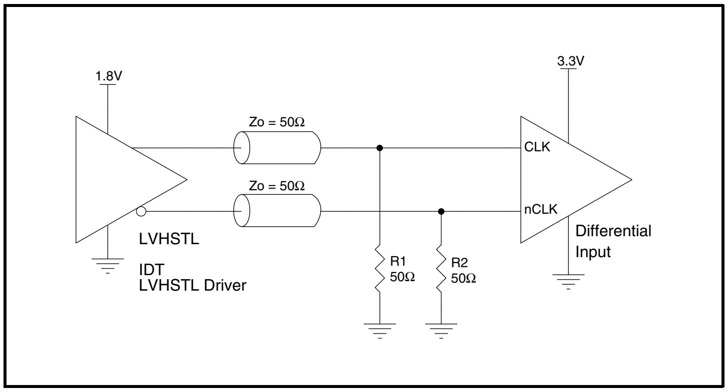


Figure 2A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

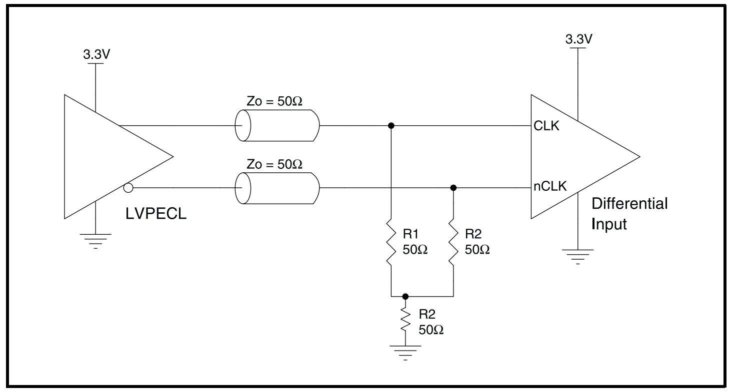


Figure 2D. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

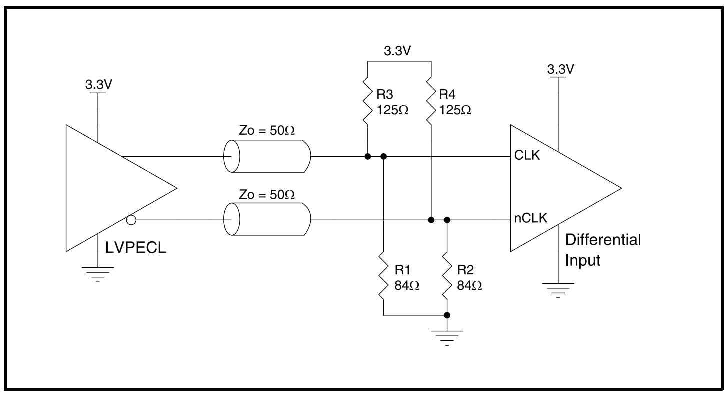


Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

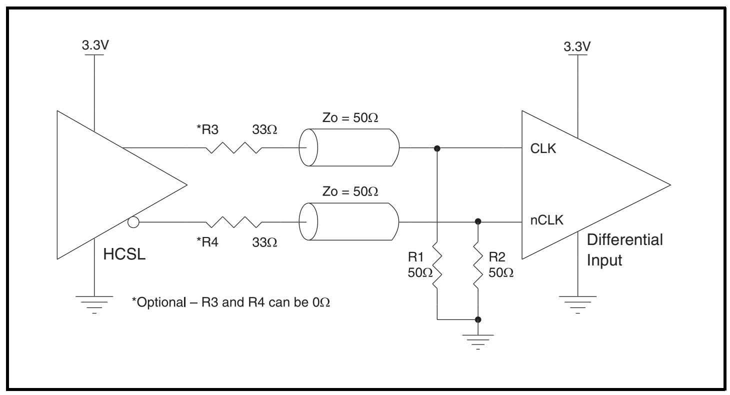


Figure 2E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

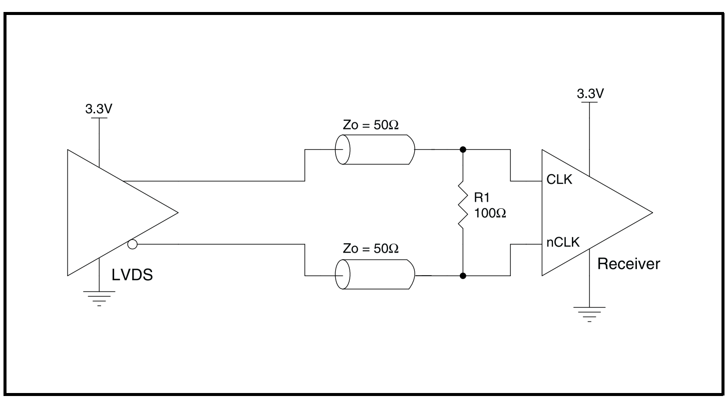


Figure 2C. Figure 2E.CLK/nCLK Input Driven by a 3.3V LVDS Driver

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential output is a low impedance follower output that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figure 3A and Figure 3B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

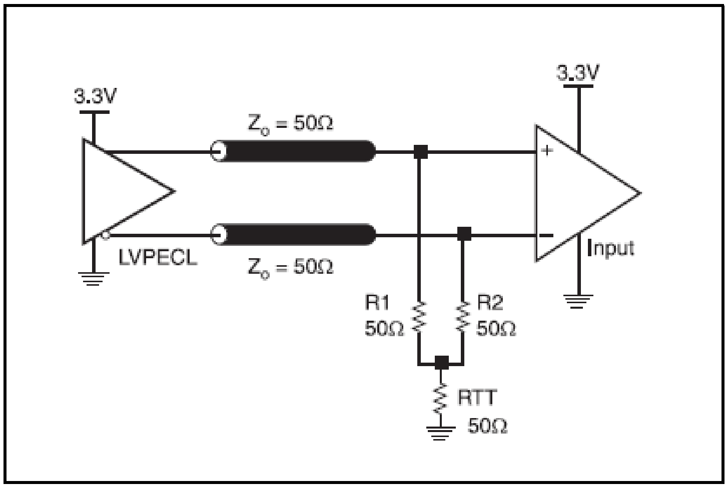


Figure 3A. 3.3V LVPECL Output Termination

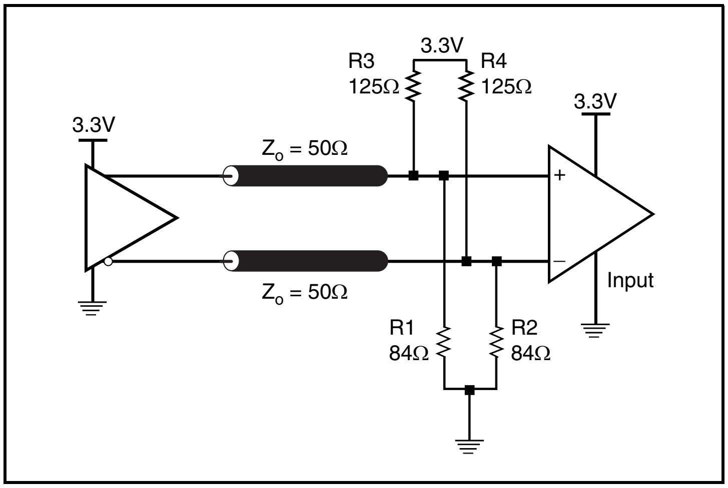


Figure 3B. 3.3V LVPECL Output Termination

Schematic Example

Figure 4 shows a schematic example of the 8735BI-21. In this example, the input is driven by an HCSL driver. The zero delay buffer is configured to operate at 155.52MHz input and 77.75MHz output. The logic control pins are configured as follows: SEL [3:0] = 0101; PLL_SEL = 1. The decoupling capacitors should be physically located near the power pin. For 8735BI-21.

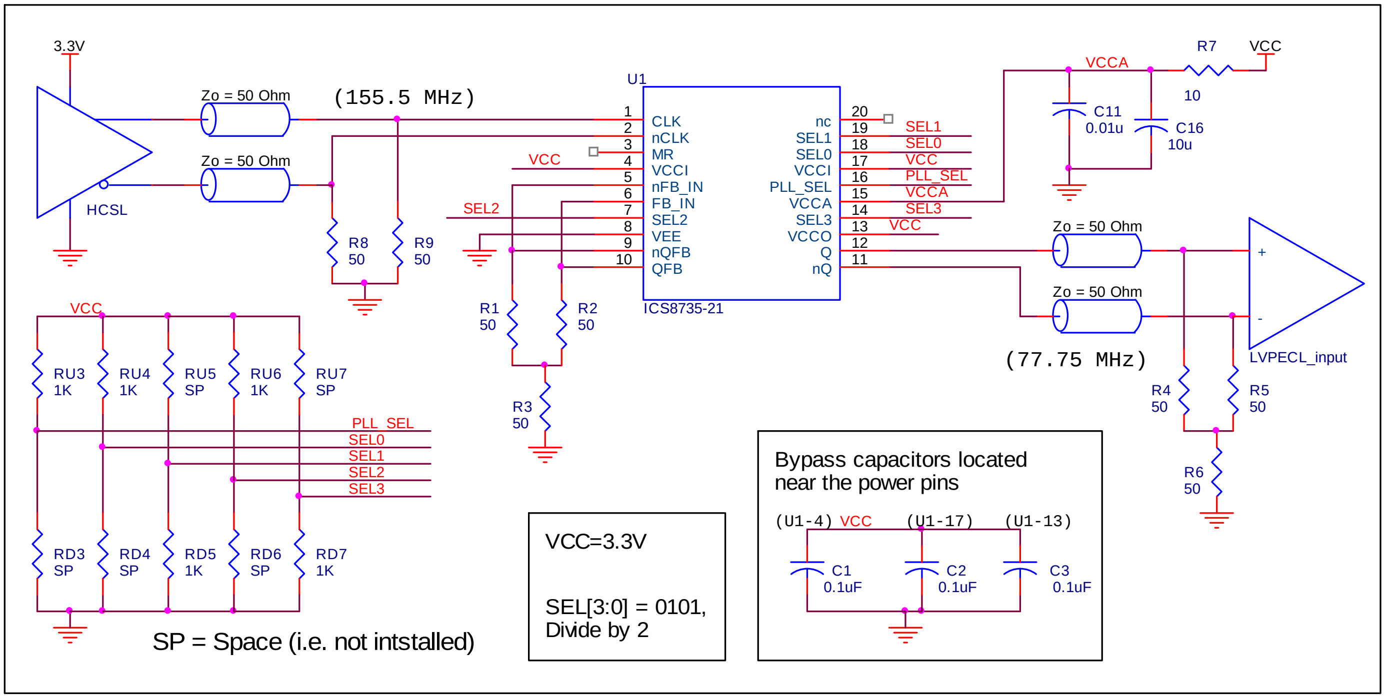


Figure 4. 8735BI-21 LVPECL Buffer Schematic Example

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor's Thermally/ Electrically Enhance Lead frame Base Package, Amkor Technology.

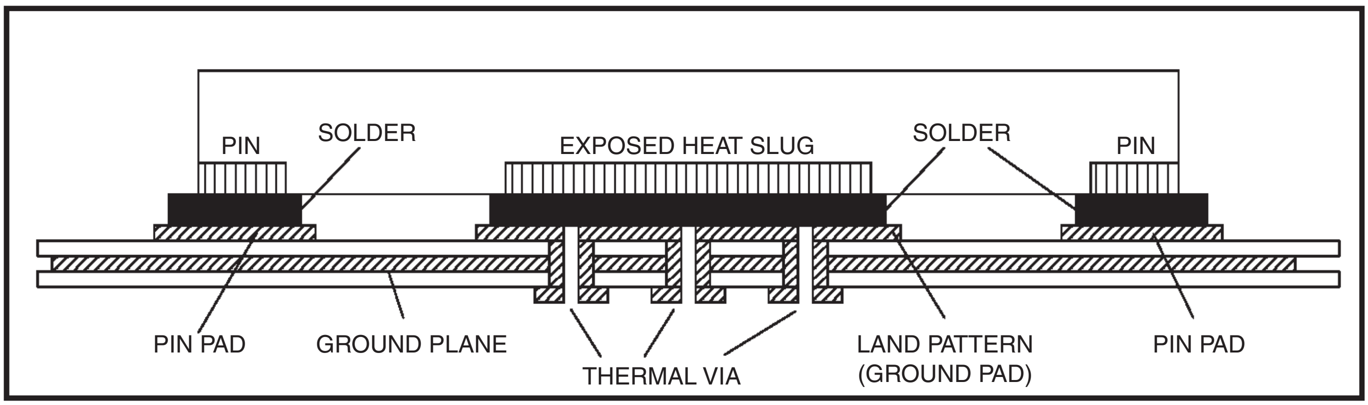


Figure 5. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the 8735BI-21.
Equations and example calculations are also provided.

Max I_{CC_MA} at worst case:
85°C = 133mA

1. Power Dissipation.

The total power dissipation for the 8735BI-21 is the sum of the core power plus the power dissipated due to loading.
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated due to loading.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{CC_MAX} = 3.465V * 155mA = **537mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded output pair**
  If all outputs are loaded, the total power is 2 * 30mW = **60mW**

Total Power$_{\_MAX}$ = (3.465V, with all outputs switching) = 537mW + 60mW = **597mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device.
The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 46.2°C/W per Table 7A, and 33.1°C/W per Table 7B below:

Therefore, Tj for an ambient temperature of 85°C with all outputs switching for **20-Lead SOIC** is:

85°C + 0.597W * 46.2°C/W = 112.6°C. This is below the limit of 125°C.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching for **32-Lead VFQFN** is:

85°C + 0.597W * 33.1°C/W = 104.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7A. Thermal Resistance θ_{JA} for 20 Lead SOIC, Forced Convection

θ_{JA} vs. Air Flow			
Linear Feet per Minute	**0**	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

Table 7B. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**3**
Multi-Layer PCB, JEDEC Standard Test Boards	33.1°C/W	28.1°C/W	25.4°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6*.

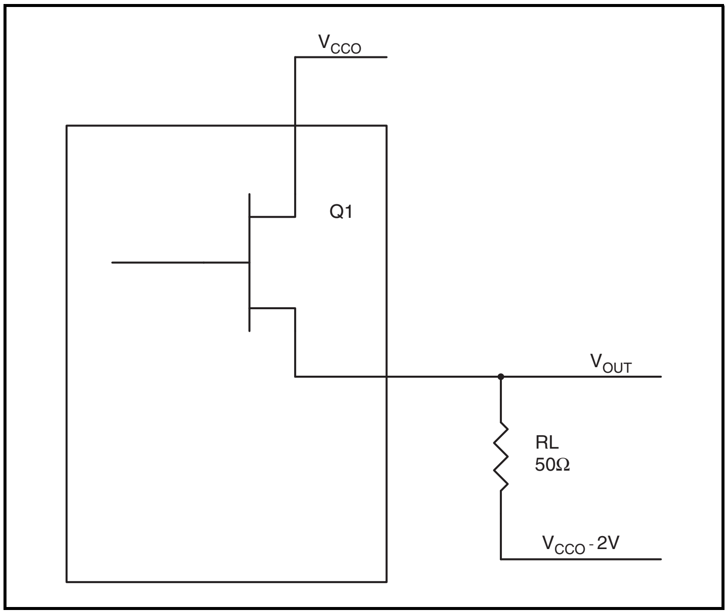


Figure 6. LVPECL Driver Circuit and Termination

To calculate power dissipation due to loading, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO} - 2V$.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} – 0.9V}$
  $(V_{CCO\_MAX} - V_{OH\_MAX})$ = **0.9V**
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} – 1.7V}$
  $(V_{CCO\_MAX} - V_{OL\_MAX})$ = **1.7V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

Pd_H = $[(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX})$ = $[(2V - 0.9V)/50\Omega] * 0.9V$ = **19.8mW**

Pd_L = $[(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX})$ = $[(2V - 1.7V)/50\Omega] * 1.7V$ = **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 8A. θ_{JA} vs. Air Flow Table for a 20 Lead SOIC

θ_{JA} vs. Air Flow			
Linear Feet per Minute	**0**	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

Table 8B. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**3**
Multi-Layer PCB, JEDEC Standard Test Boards	33.1°C/W	28.1°C/W	25.4°C/W

Transistor Count

The transistor count for 8735BI-21 is: 2969

Package Outline and Package Dimensions

Package Outline - M Suffix for 20 Lead SOIC

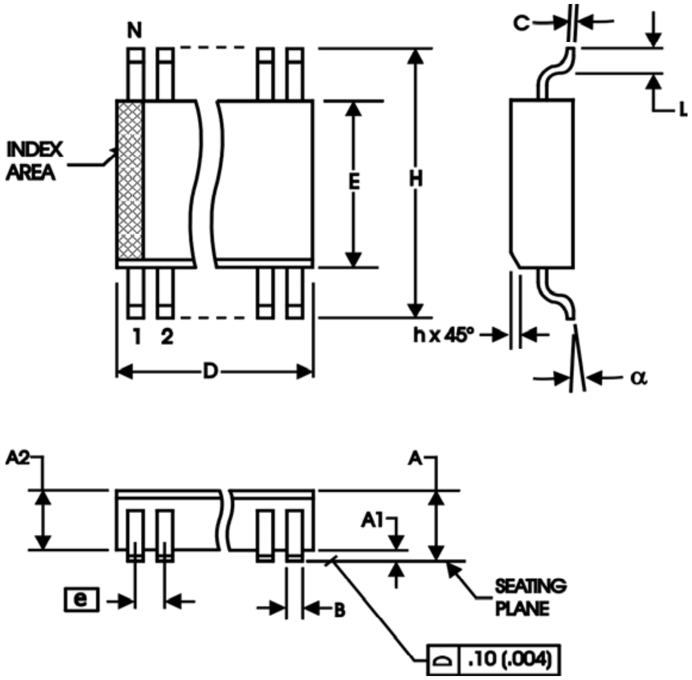
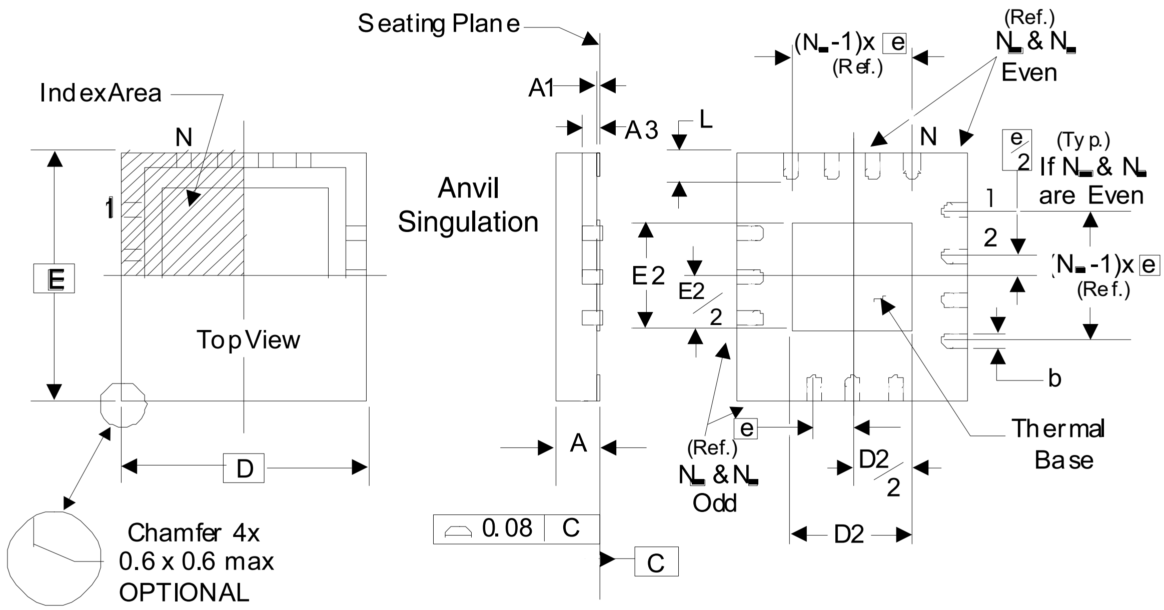


Table 9A. Package Dimensions for 20 Lead SOIC

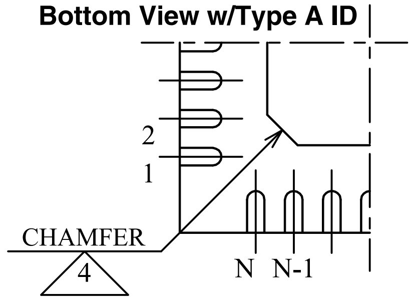
300 Millimeters All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	20	
A		2.65
A1	0.10	
A2	2.05	2.55
B	0.33	0.51
C	0.18	0.32
D	12.60	13.00
E	7.40	7.60
e	1.27 Basic	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0°	7°

Reference Document: JEDEC Publication 95, MS-013, MS-119

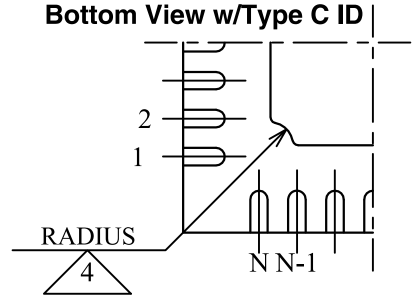
Package Outline - K Suffix for 32 Lead VFQFN



Bottom View w/Type A ID



Bottom View w/Type C ID



There are 2 methods of indicating pin 1 corner at the back of the VFQFN package:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

Table 9B. Package Dimensions

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A	0.80		1.00
A1	0		0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D & N_E			8
D & E		5.00 Basic	
D2 & E2	3.0		3.3
e		0.50 Basic	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pin-out are shown on the front page. The package dimensions are in *Table 9B*.

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8735BMI-21LF	8735BMI-21LF	20 Lead SOIC, Lead-Free	Tube	-40°C to 85°C
8735BMI-21LFT	8735BMI-21LF	20 Lead SOIC, Lead-Free	Tape & Reel	-40°C to 85°C
8735BKI-21LF	735BI21L	32 Lead VFQFN, Lead-Free	Tray	-40°C to 85°C
8735BKI-21LFT	735BI21L	32 Lead VFQFN, Lead-Free	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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Contact Information

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