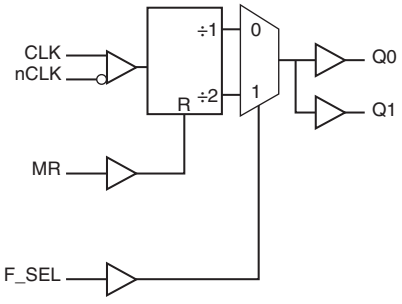
General Description

The 87021I is a high performance ÷1/÷2 Differential-to-LVCMOS/LVTTL Clock Generator and a member of the family of High Performance Clock Solutions from IDT. The CLK, nCLK pair can accept most standard differential input levels. Guaranteed part-to-part skew characteristics make the 87021I ideal for those clock distribution applications demanding well defined performance and repeatability.

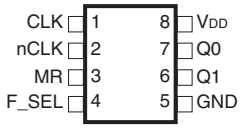
Features

- Two single-ended LVCMOS/LVTTL outputs
- One differential CLK, nCLK input pair
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum output frequency: 250MHz
- Additive phase jitter, RMS: 0.18ps (typical)
- Output skew: 50ps (maximum)
- Part-to-part skew: 450ps (maximum)
- Propagation delay: 3.4ns (maximum)
- Full 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Availalbe in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



87021I
8-Lead SOIC
3.90mm x 4.90mm x 1.375mm package body
M Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	CLK	Input	Pulldown	Non-inverting differential clock input.
2	nCLK	Input	Pullup	Inverting differential clock input.
3	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the outputs to go low. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels. See Table 3.
4	F_SEL	Input	Pulldown	Selects divider value for Qx outputs as described in Table 3. LVCMOS / LVTTL interface levels.
5	GND	Power		Power supply ground.
6	Q1	Output		Singled-ended output. LVCMOS/LVTTL interface levels.
7	Q0	Output		Singled-ended output. LVCMOS/LVTTL interface levels.
8	V_{DD}	Power		Positive supply pin.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD} = 3.465V		24		pF
		V_{DD} = 2.625V		16		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance	V_{DD} = 3.465V		9		Ω

TABLE 3. FUNCTION TABLE

MR	F_SEL	Divide Value
1	X	Reset: Q0, Q1 outputs low
0	0	÷1
0	1	÷2

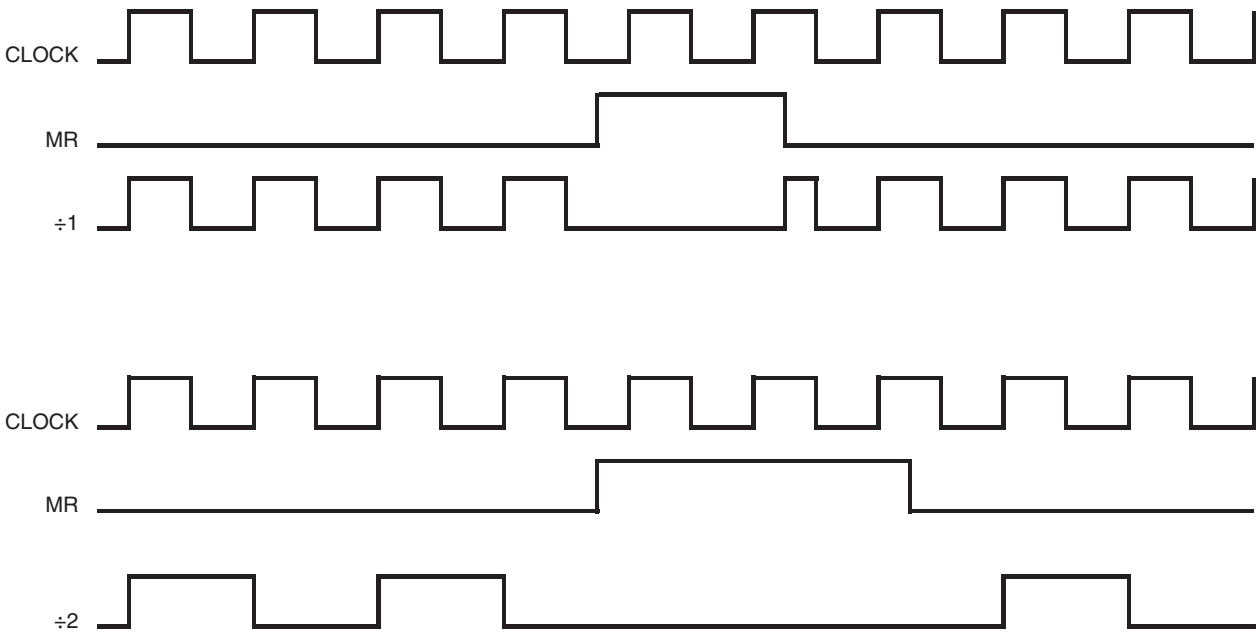


FIGURE 1. TIMING DIAGRAM

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	103°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				60	mA

Table 4B. Power Supply DC Characteristics, V_{DD} = 2.5V±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				35	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		1.3		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.7	V
I_{IH}	Input High Current	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1	V_{DD} = 3.465V	2.6			V
V_{OL}	Output Low Voltage; NOTE 1	V_{DD} = 3.465V or 2.625V			0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DD}/2. See Parameter Measurement Information section, "3.3V Output Load Test Circuit" diagram.

Table 4D. LVCMOS/LVTTL DC Characteristics, V_{DD} = 2.5V±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		1.1		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.5	V
I_{IH}	Input High Current	$V_{DD} = V_{IN}$ = 2.625V			150	µA
I_{IL}	Input Low Current	V_{DD} = 2.625V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1	V_{DD} = 2.625V	1.8			V
V_{OL}	Output Low Voltage; NOTE 1	V_{DD} = 2.625V			0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DD}/2. See Parameter Measurement Information section, "2.5V Output Load Test Circuit" diagram.

TABLE 4E. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = 3.3V±5% OR V_{DD} = 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
		nCLK	V_{DD} = V_{IN} = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	CLK	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
		nCLK	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.

TABLE 5A. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					250	MHz
t_{PD}	Propagation Delay; NOTE 1	CLK to Qx		2.1		3.4	ns
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section		250MHz, Integration Range: 12kHz – 20MHz		0.18		ps
tsk(pp)	Part-to-Part Skew; NOTE 2, 3					450	ps
*t*sk(o)	Output Skew; NOTE 3, 4					50	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	250		700	ps
odc	Output Duty Cycle;		Fout ≤ 133MHz	45		55	%
		NOTE 5	Fout > 133MHz	40		60	%

NOTE 1: Measured from the differential input crossing point to the output at V_{DD}/2.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DD}/2.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs at the same supply voltage and with equal load conditions.
NOTE 5: Output Duty Cycle assuming 50% input duty cycle.

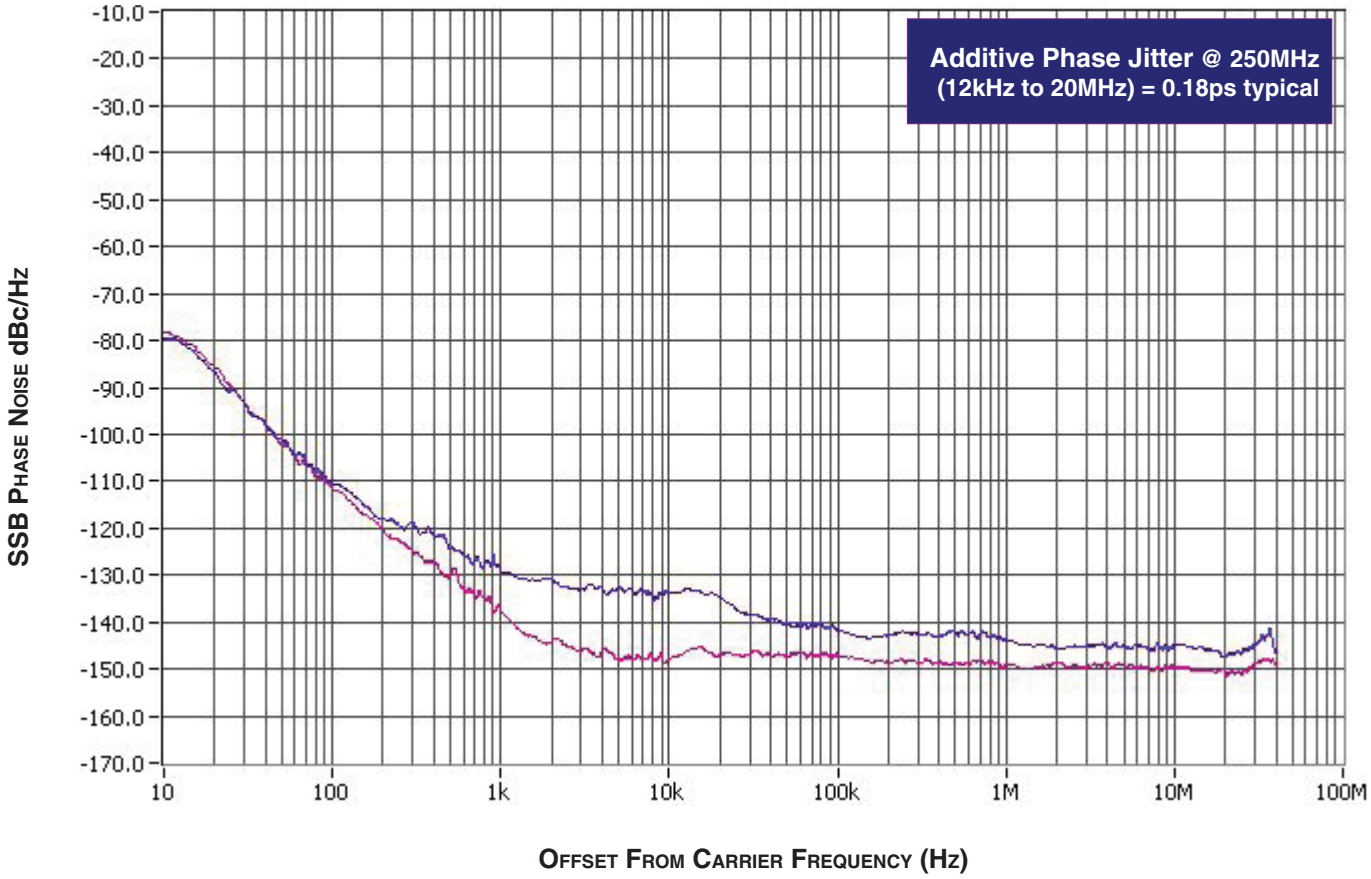
TABLE 5B. AC CHARACTERISTICS, V_{DD} = 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					250	MHz
t_{PD}	Propagation Delay; NOTE 1	CLK to Qx		2.7		3.4	ns
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section		250MHz, Integration Range: 12kHz – 20MHz		0.3		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3					450	ps
*t*sk(o)	Output Skew; NOTE 3, 4					25	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	250		700	ps
odc	Output Duty Cycle;		Fout ≤ 133MHz	45		55	%
		NOTE 5	Fout > 133MHz	40		60	%

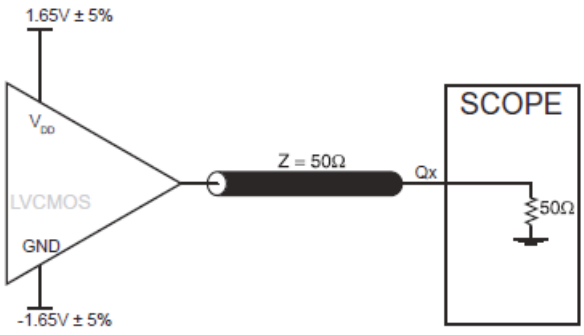
For NOTES, please see above Table 5A.

Additive Phase Jitter

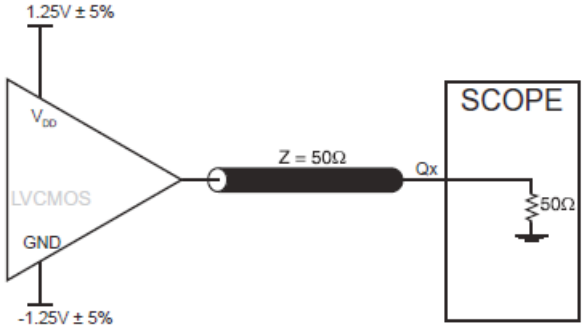
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



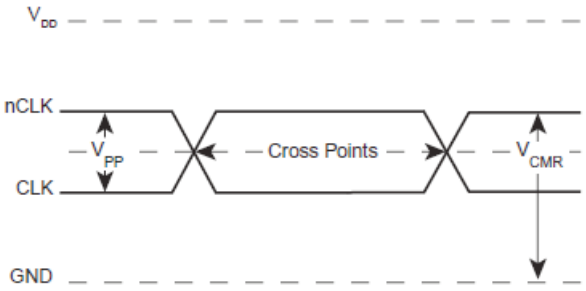
PARAMETER MEASUREMENT INFORMATION



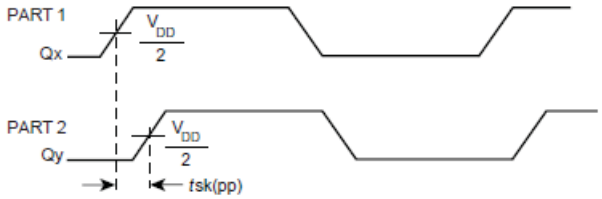
3.3V OUTPUT LOAD AC TEST CIRCUIT



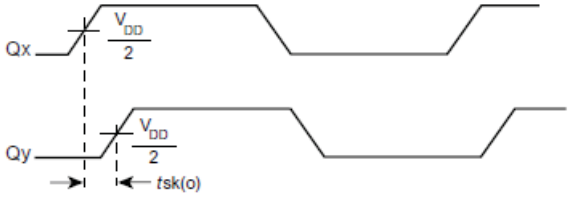
2.5V OUTPUT LOAD AC TEST CIRCUIT



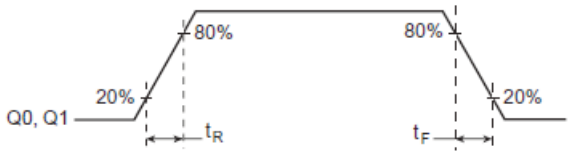
DIFFERENTIAL INPUT LEVEL



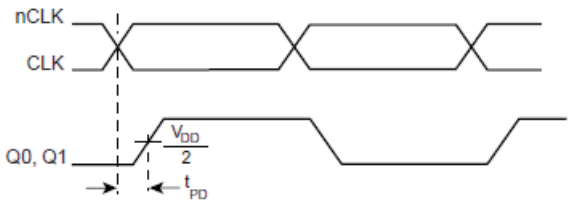
PART-TO-PART SKEW



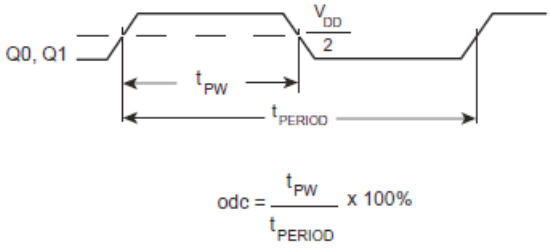
OUTPUT SKEW



OUTPUT RISE/FALL TIME



PROPAGATION DELAY



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

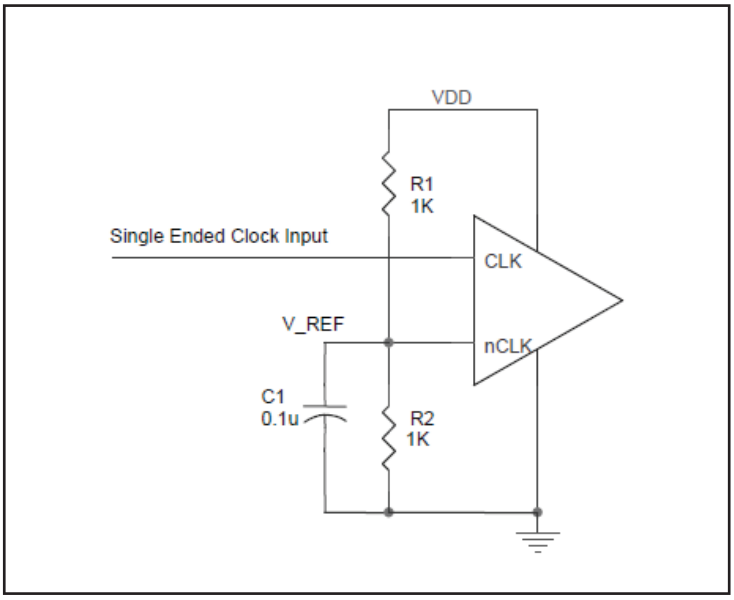


Figure 1. Single Ended Signal Driving Differential Input

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. Figures 2A to 2E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 2A,* the input termination applies for IDT HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

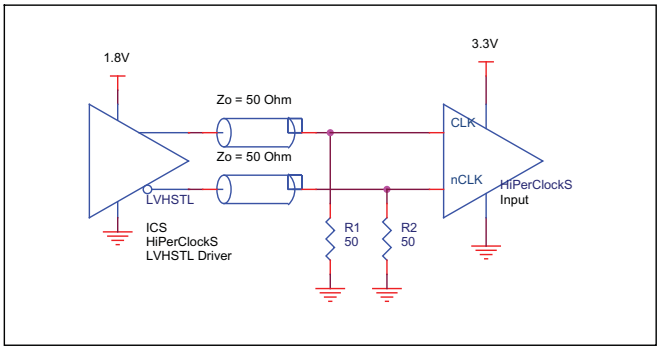


Figure 2A. HiPerClockS CLK/nCLK Input Driven by IDT HiPerClockS LVHSTL Driver

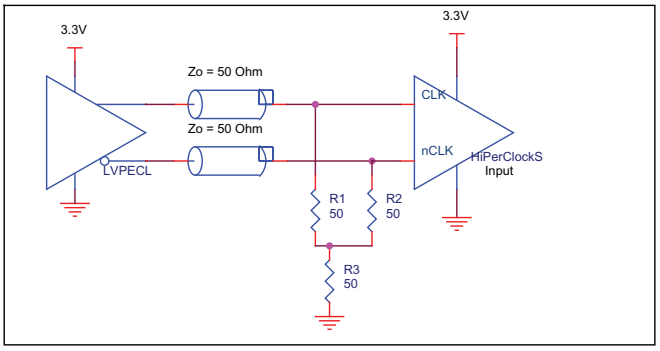


Figure 2B. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver

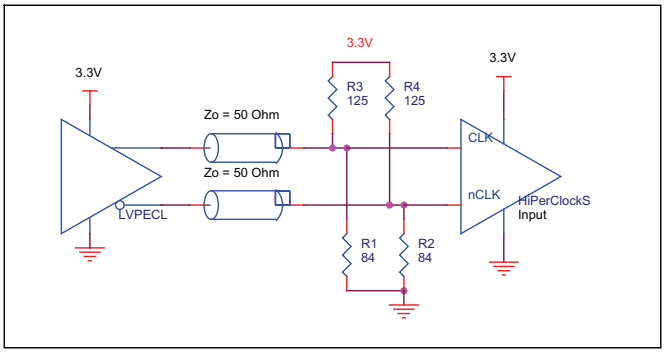


Figure 2C. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver

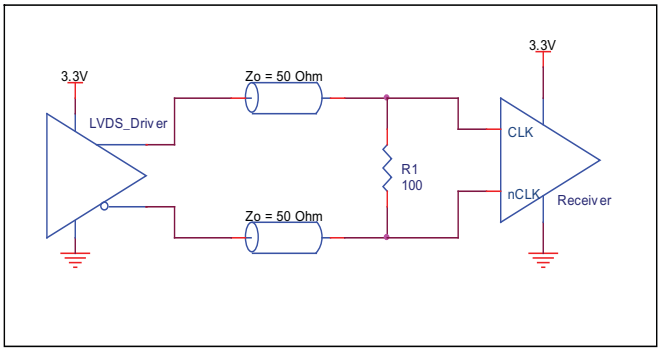


Figure 2D. HiPerClockS CLK/nCLK Input Driven by 3.3V LVDS Driver

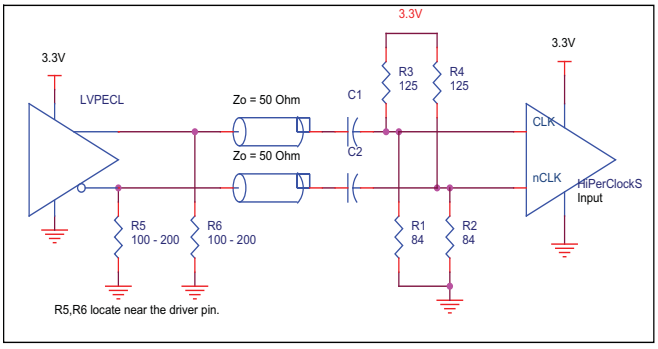


Figure 2E. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver with AC Couple

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD SOIC

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	123°C/W	110°C/W	99°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	103°C/W	94°C/W	89°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for 87021I is: 414

Package Outline - M Suffix for 8 Lead SOIC

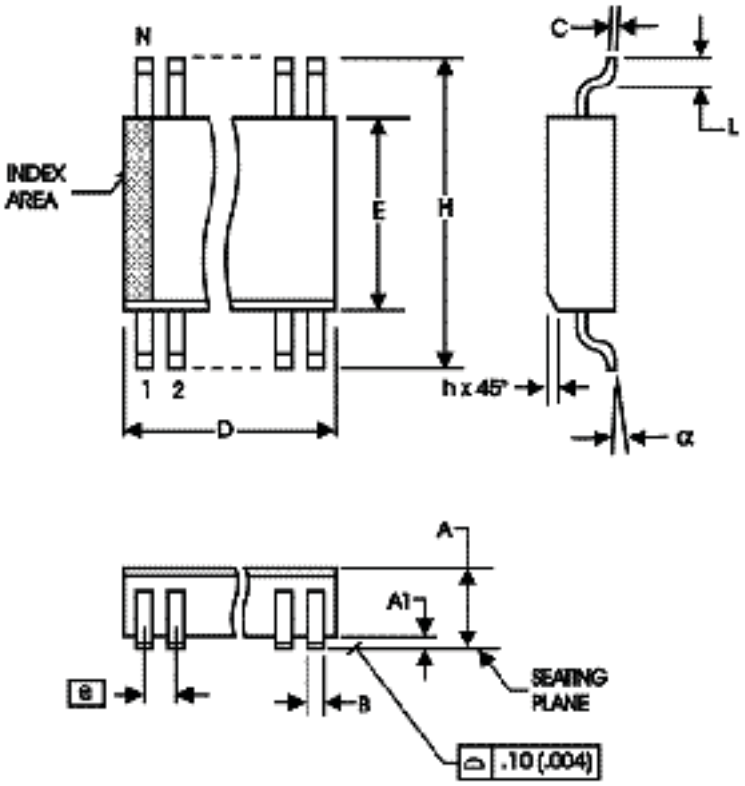


Table 7. Package Dimensions

SYMBOL	Millimeters	
	MINIMUN	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
87021AMILF	87021AIL	8 lead “Lead Free” SOIC	Tube	-40°C to +85°C
87021AMILFT	87021AIL	8 lead “Lead Free” SOIC	Tape and Reel	-40°C to +85°C

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	T2	2	Pin Characteristics Table - added R_{OUT} row.	8/26/08
B	T8	1 1 12	Removed ICS from the part numbers where needed. General Description - Removed the ICS chip and HiPerClockS. Features Section - Removed reference to lead free packages. Ordering Information - removed quantity from tape and reel. Deleted LF note below the table. Updated header and footer.	1-26-16
B	8	12	Changed Shipping Packaging from "Tray" to "Tube".	9-2-2021

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(Rev.1.0 Mar 2020)

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