General Description

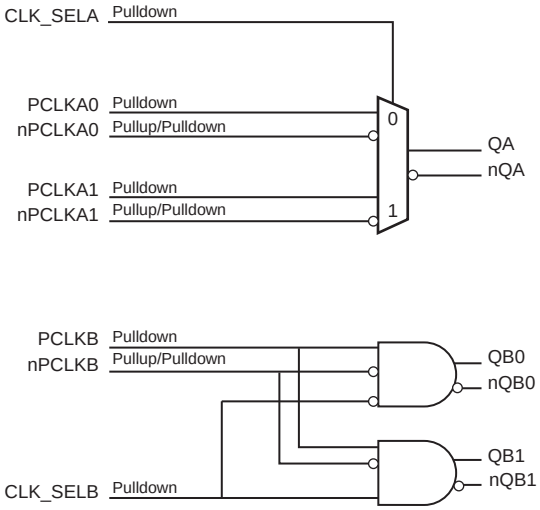
The ICS853S54I is a dual 2:1 and 1:2 Multiplexer. The 2:1 Multiplexer allows one of 2 inputs to be selected onto one output pin and the 1:2 MUX switches one input to one of two outputs. This device is useful for multiplexing multi-rate Ethernet PHYs which have 100 M bit and 1000 bit transmit/receive pairs onto an optical SFP module which has a single transmit/receive pair. See Application Section for further information.

The ICS853S54I is optimized for applications requiring very high performance and has a maximum operating frequency of 2.5GHz. The device is packaged in a small, 3mm x 3mm VFQFN package, making it ideal for use on space-constrained boards.

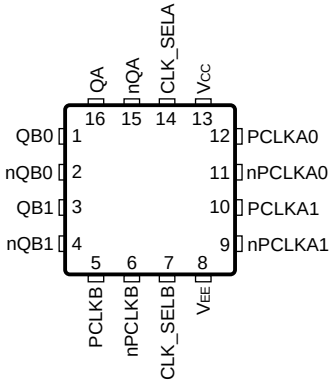
Features

- Three differential LVPECL output pairs
- Three differential LVPECL clock inputs
- PCLKx/nPCLKx pairs can accept the following differential input levels: LVPECL, LVDS, CML
- Maximum output frequency: 2.5GHz
- Part-to-part skew: 200ps (maximum)
- Propagation delay: QA, nQA: 450ps (maximum)
  QBx, nQBx: 420ps (maximum)
- LVPECL mode operating voltage supply range:
  V_{CC} = 2.375V to 3.465V, V_{EE} = 0V
- ECL mode operating voltage supply range:
  V_{CC} = 0V, V_{EE} = -3.465V to -2.375V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) packaging

Block Diagram



Pin Assignment



ICS853S54I

16-Lead VFQFN
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	QB0, nQB0	Output		Differential output pair. LVPECL/ECL interface levels.
3, 4	QB1, nQB1	Output		Differential output pair. LVPECL/ECL interface levels.
5	PCLKB	Input	Pulldown	Non-inverting LVPECL/ECL differential clock input.
6	nPCLKB	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V_{CC}/2 default when left floating.
7	CLK_SELB	Input	Pulldown	Clock select pin for QBx outputs. When HIGH, selects QB1/nQB1 outputs. When LOW, selects QB0/nQB0 outputs. LVCMOS/LVTTL interface levels.
8	V_{EE}	Power		Negative supply pin.
9	nPCLKA1	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V_{CC}/2 default when left floating.
10	PCLKA1	Input	Pulldown	Non-inverting LVPECL/ECL differential clock input.
11	nPCLKA0	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V_{CC}/2 default when left floating.
12	PCLKA0	Input	Pulldown	Non-inverting LVPECL/ECL differential clock input.
13	V_{CC}	Power		Positive supply pin.
14	CLK_SELA	Input	Pulldown	Clock select pin for QA output. When HIGH, selects QA output. When LOW, selects nQA output. LVCMOS/LVTTL interface levels.
15, 16	nQA, QA	Output		Differential output pair. LVPECL/ECL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
$R_{PULLDOWN}$	Input Pullup Resistor			37.5		kΩ
$R_{VCC/2}$	RPullup/Pulldown Resistor			37.5		kΩ

Function Tables

Table 3A. Control Input Function Table, (Bank A)

Bank A	
Control Input	**Outputs**
CLK_SELA	**QA, nQA**
0 (default)	Selects PCLKA0, nPCLKA0
1	Selects PCLKA1, nPCLKA1

Table 3B. Control Input Function Table, (Bank B)

Bank B		
Control Input	**Outputs**	
CLK_SELB	**QB0, nQB0**	**QB1, nQB1**
0 (default)	Follows PCLKB input	Logic Low
1	Logic Low	Follows PCLKB input

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V (LVPECL mode, V_{EE} = 0V)
Negative Supply Voltage, V_{EE}	-4.6V (ECL mode, V_{CC} = 0V)
Inputs, V_I (LVPECL mode)	-0.5V to V_{CC} + 0.5V
Inputs, V_I (ECL mode)	0.5V to V_{EE} – 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Operating Termperature Range, T_A	-40°C to 85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA}	74.7°C/W (0 mps)

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 2.375V to 3.465V, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{EE}	Power Supply Current				45	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{CC} = 2.375V to 3.465V, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			$0.7V_{CC}$		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		$0.3V_{CC}$	V
I_{IH}	Input High Current	CLK_SELA, CLK_SELB	$V_{CC} = V_{IN}$			150	µA
I_{IL}	Input Low Current	CLK_SELA, CLK_SELB	$V_{CC} = V_{IN}$	-150			µA

Table 4C. LVCMOS/LVTTL DC Characteristics, V_{CC} = 0V, V_{EE} = -3.465V to -2.375V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			$0.3V_{EE}$		0.3	V
V_{IL}	Input Low Voltage			V_{EE} – 0.3		$0.7V_{EE}$	V
I_{IH}	Input High Current	CLK_SELA, CLK_SELB	$V_{CC} = V_{IN}$			150	µA
I_{IL}	Input Low Current	CLK_SELA, CLK_SELB	$V_{CC} = V_{IN}$	-150			µA

Table 4D. LVPECL DC Characteristics, V_{CC} = 2.375V to 3.465V, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLKA[0:1], PCLKB	$V_{CC} = V_{IN}$			200	µA
		nPCLKA[0:1], nPCLKB	$V_{CC} = V_{IN}$			200	µA
I_{IL}	Input Low Current	PCLKA[0:1], PCLKB	V_{CC} = 3.465V, V_{IN} = 0V	-200			µA
		nPCLKA[0:1], nPCLKB	V_{CC} = 3.465V, V_{IN} = 0V	-200			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.15		1.2	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			1.2		V_{CC}	V
V_{OH}	Output High Current; NOTE 3			V_{CC} – 1.125	V_{CC} – 1.005	V_{CC} – 0.875	V
V_{OL}	Output Low Current; NOTE 3			V_{CC} – 1.895	V_{CC} – 1.78	V_{CC} – 1.62	V
V_{SWING}	Peak-to-Peak Output Voltage Swing			0.6		1.0	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.
NOTE 3: Outputs terminated with 50Ω to V_{CC} – 2V.

AC Electrical Characteristics

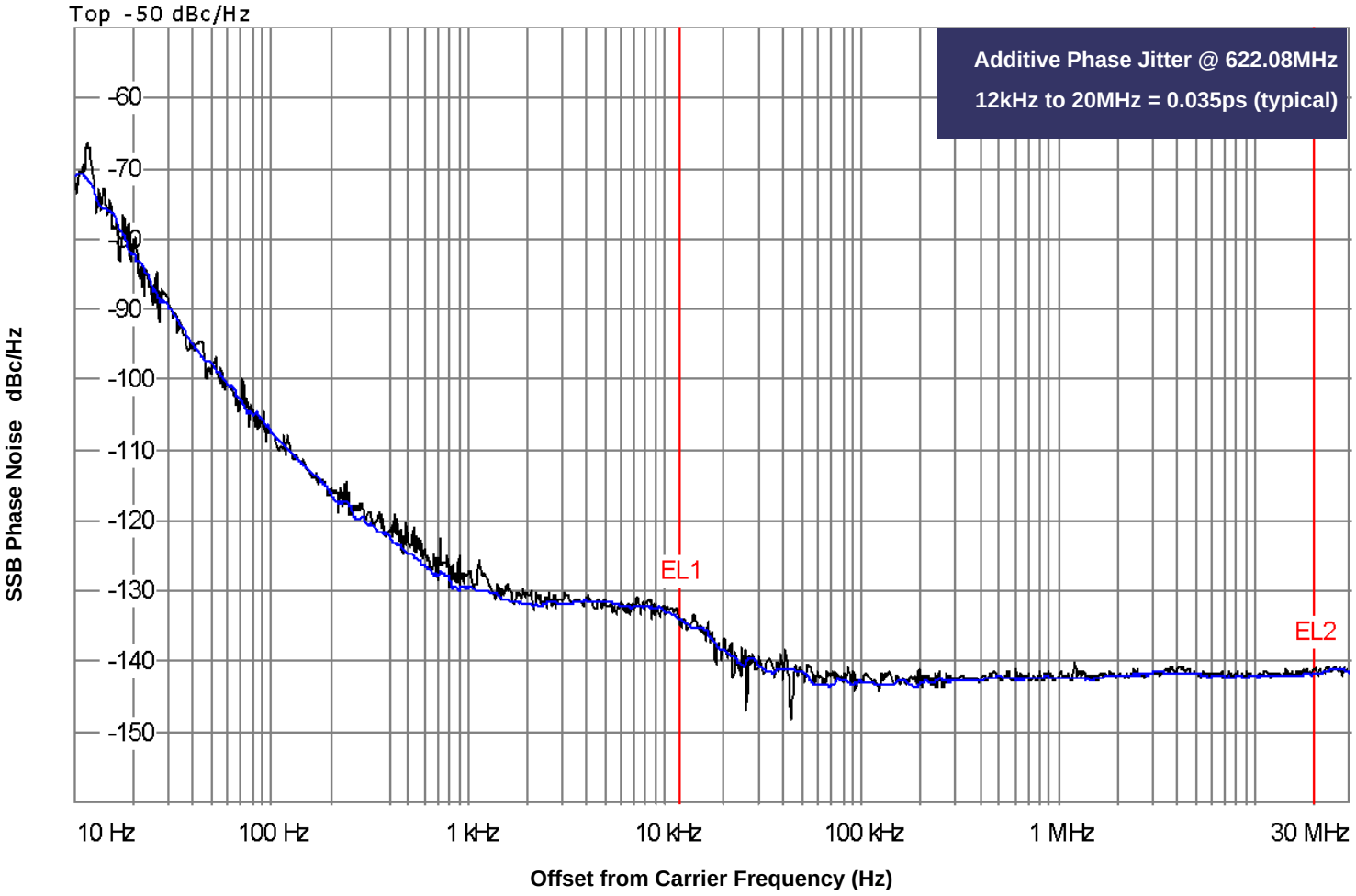
Table 5. AC Characteristics, V_{CC} = 2.375V to 3.465V, V_{EE} = 0V or V_{CC} = 0V, V_{EE} = -3.465V to -2.375V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency					2.5	GHz
t_{PD}	Propagation Delay; NOTE 1	QA, nQA		225	335	445	ps
		QBx, nQBx		195	305	420	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3					200	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; NOTE 4		622.08MHz Integration Range: 12kHz - 20MHz		0.035		ps
$MUX_{\_ISOLATION}$	MUX Isolation; NOTE 5		f_{OUT} = 622.08MHz, V_{PP} = 800mV		65		dB
t_R / t_F	Output Rise/Fall Time		20% to 80%	75	155	250	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters are measured ≤ 1GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Measured using clock input at 622.08MHz.
NOTE 5: Q/nQ output measured differentially. See *Parameter Measurement Information* for MUX Isolation diagram.

Additive Phase Jitter

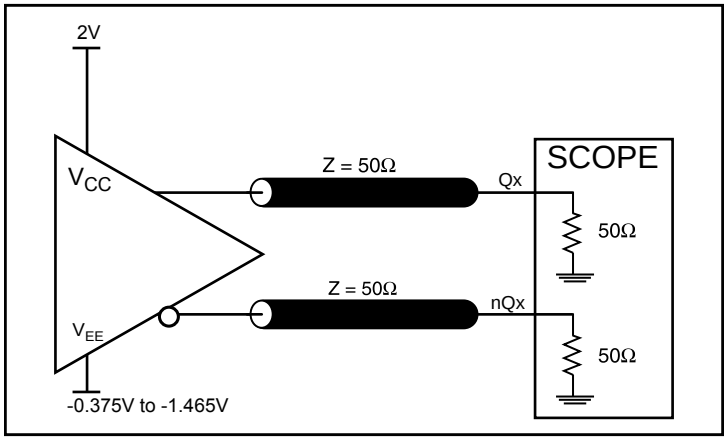
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



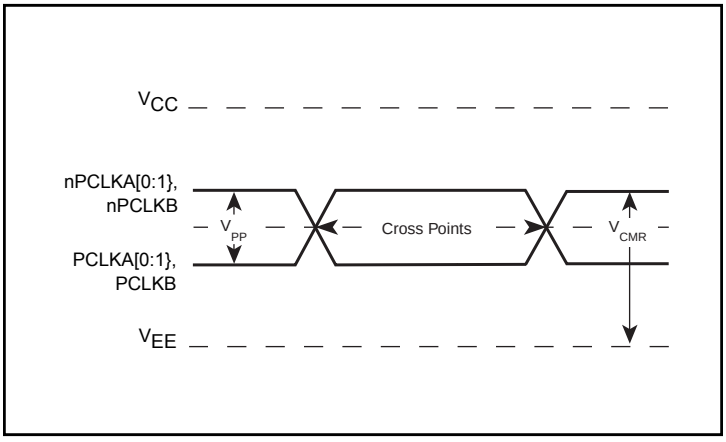
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

The source generator “IFR2042 10kHz – 56.4GHz Low Noise Signal Generator as external input to an Agilent 8133A 3GHz Pulse Generator”.

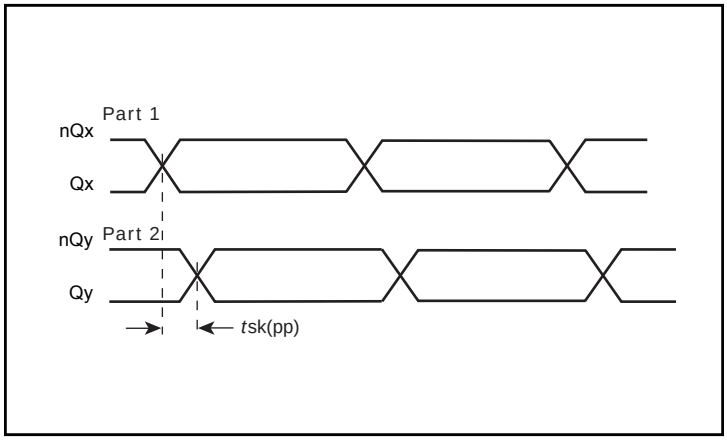
Parameter Measurement Information



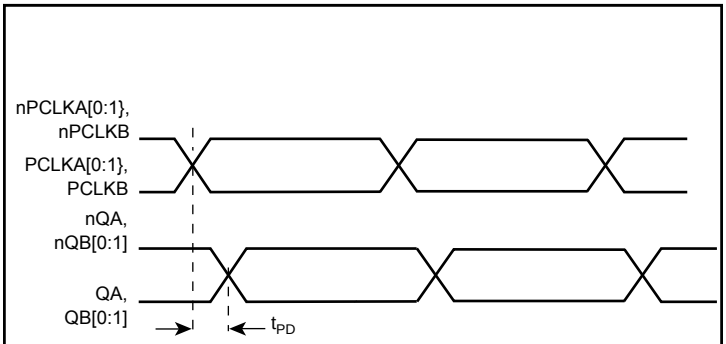
LVPECL Output Load AC Test Circuit



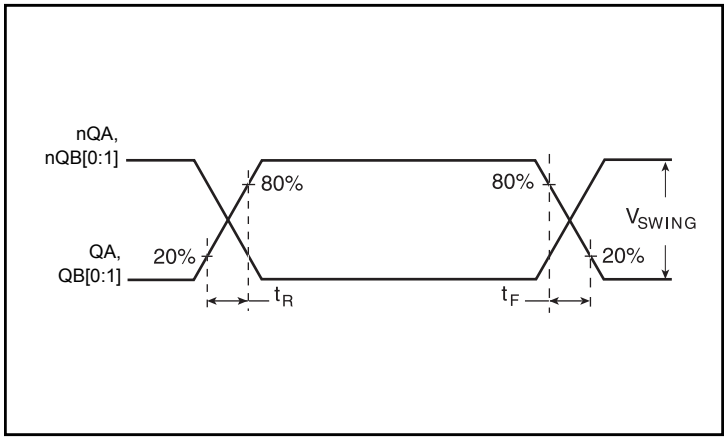
Differential Input Level



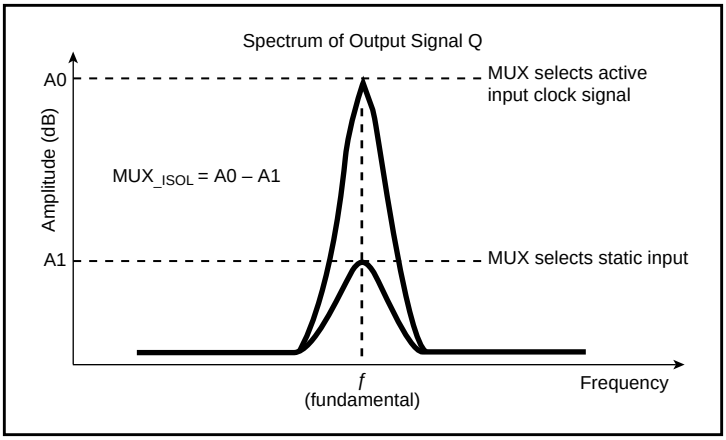
Part-to-Part Skew



Propagation Delay



Output Rise/Fall Time



MUX Isolation

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{CC}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

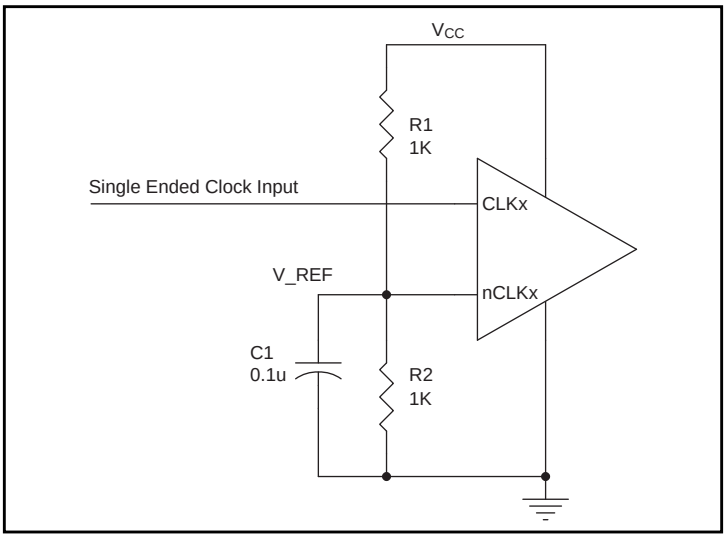


Figure 1. Single-Ended Signal Driving Differential Input

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

PCLK/nPCLK Inputs

For applications not requiring the use of the differential input, both PCLK and nPCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVPECL Differential Clock Input Interface (3.3V)

The PCLK /nPCLK accepts LVDS, LVPECL, and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2C* show interface examples for the PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

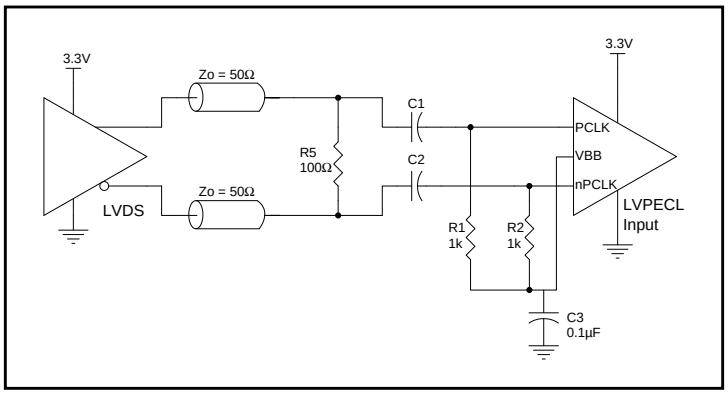


Figure 2A. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

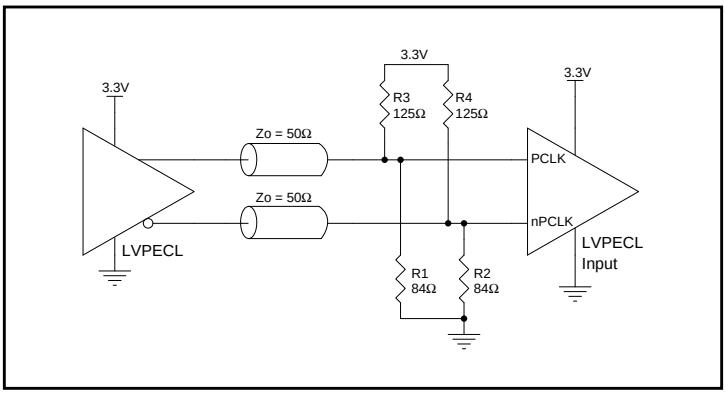


Figure 2B. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

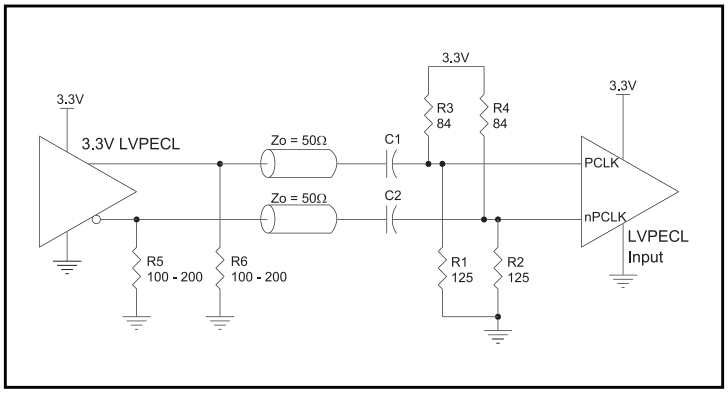


Figure 2C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

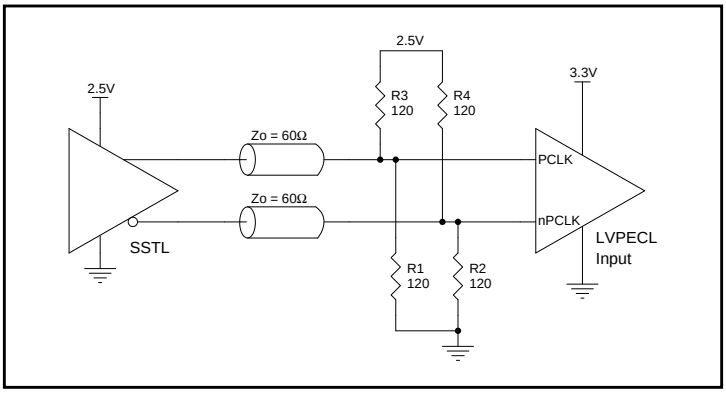


Figure 2D. PCLK/nPCLK Input Driven by an SSTL Driver

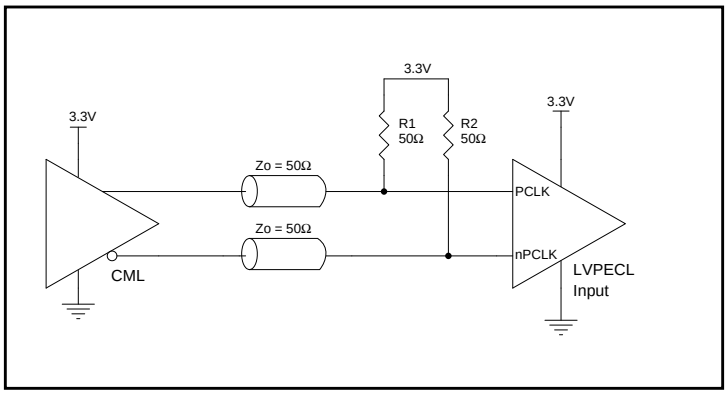


Figure 2E. PCLK/nPCLK Input Driven by a CML Driver

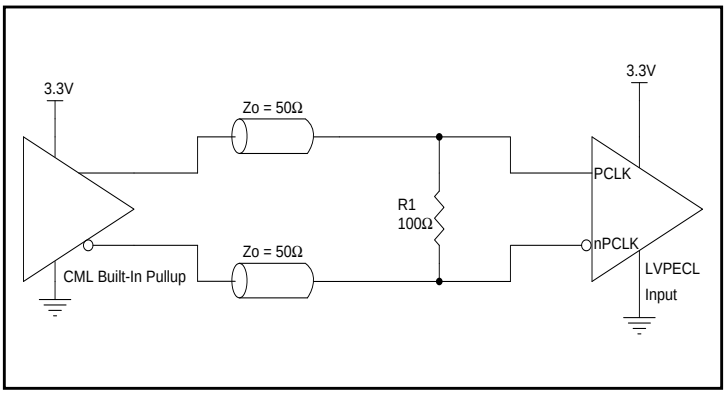


Figure 2F. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

LVPECL Clock Input Interface (2.5V)

The PCLK /nPCLK accepts LVPECL, LVDS and other differential signals. The differential signal must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2C* show interface examples for the PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

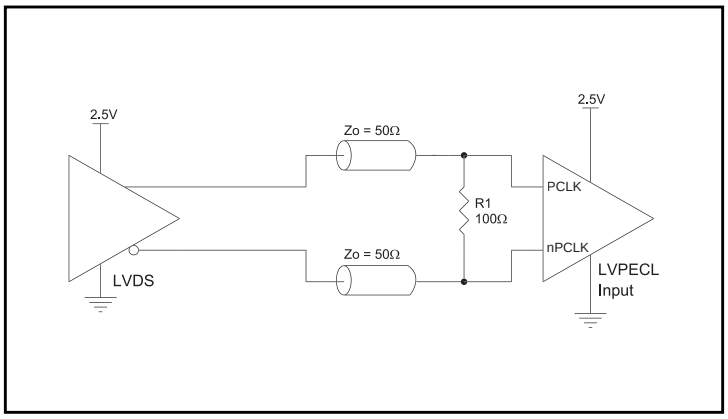


Figure 2A. PCLK/nPCLK Input Driven by a 2.5V LVDS Driver

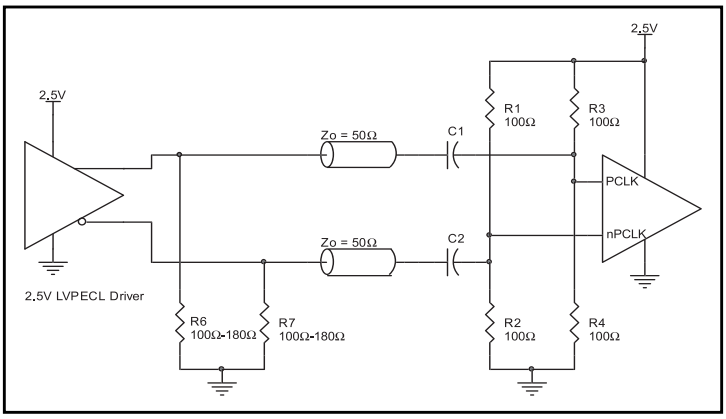


Figure 2B. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

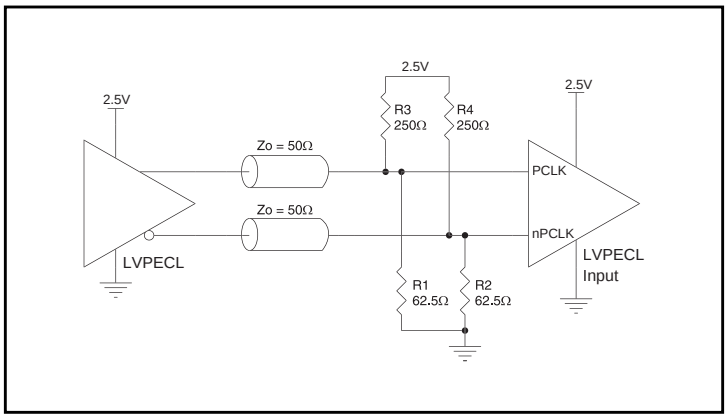


Figure 2C. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

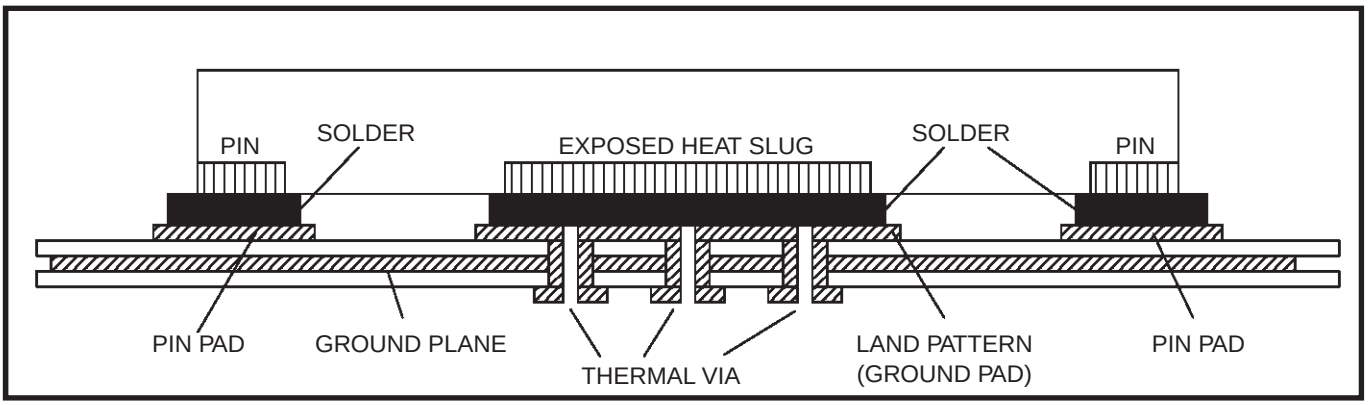


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

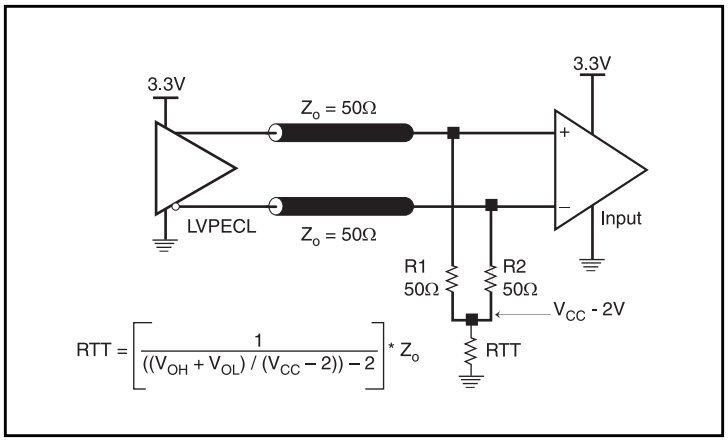


Figure 5A. 3.3V LVPECL Output Termination

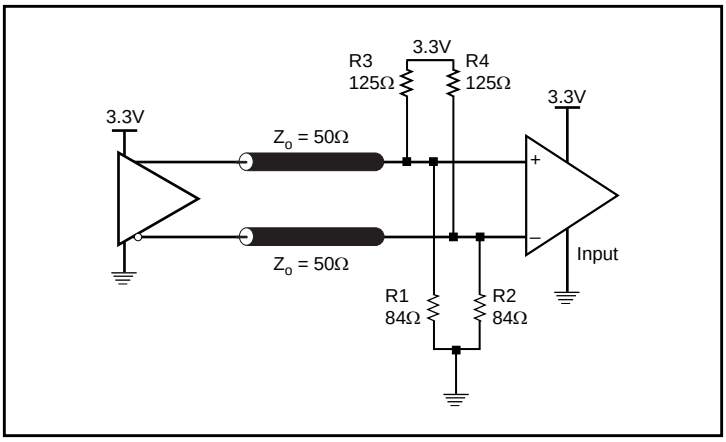


Figure 5B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 6A and *Figure 6B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 6B can be eliminated and the termination is shown in *Figure 6C.*

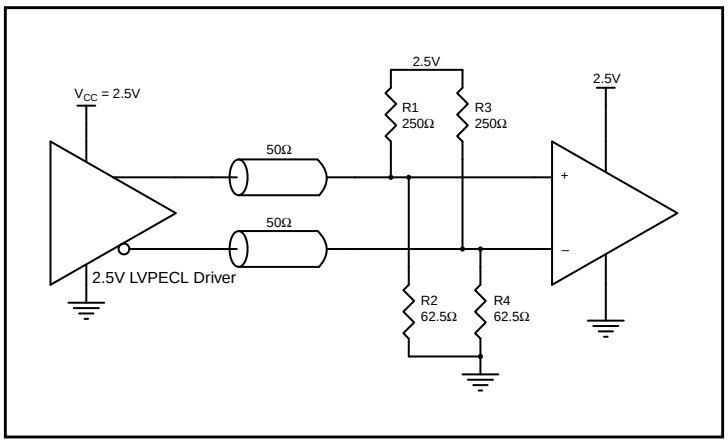


Figure 6A. 2.5V LVPECL Driver Termination Example

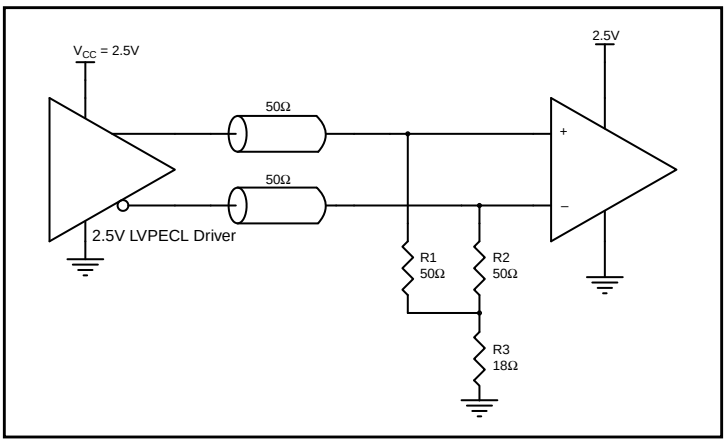


Figure 6B. 2.5V LVPECL Driver Termination Example

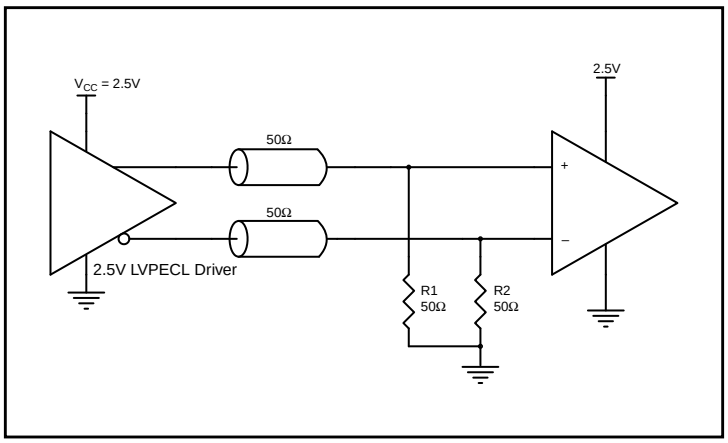
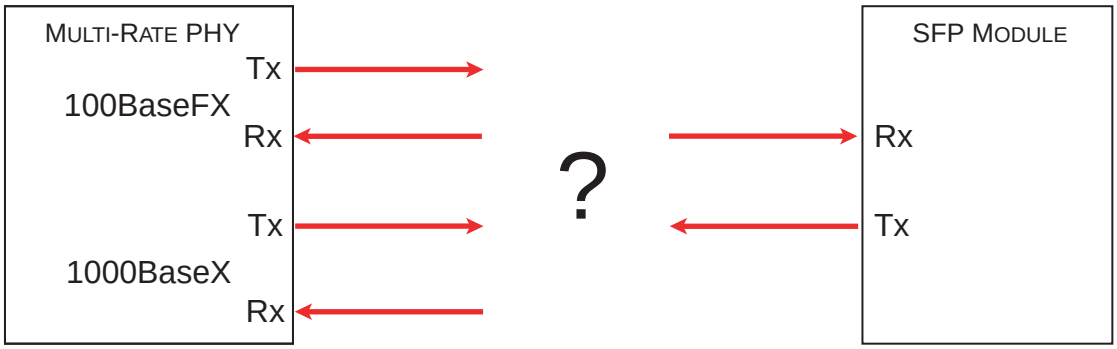


Figure 6C. 2.5V LVPECL Driver Termination Example

A Typical Application for the ICS853S54I

Used to connect a multi-rate PHY with the Tx/Rx pins of an SFP Module.

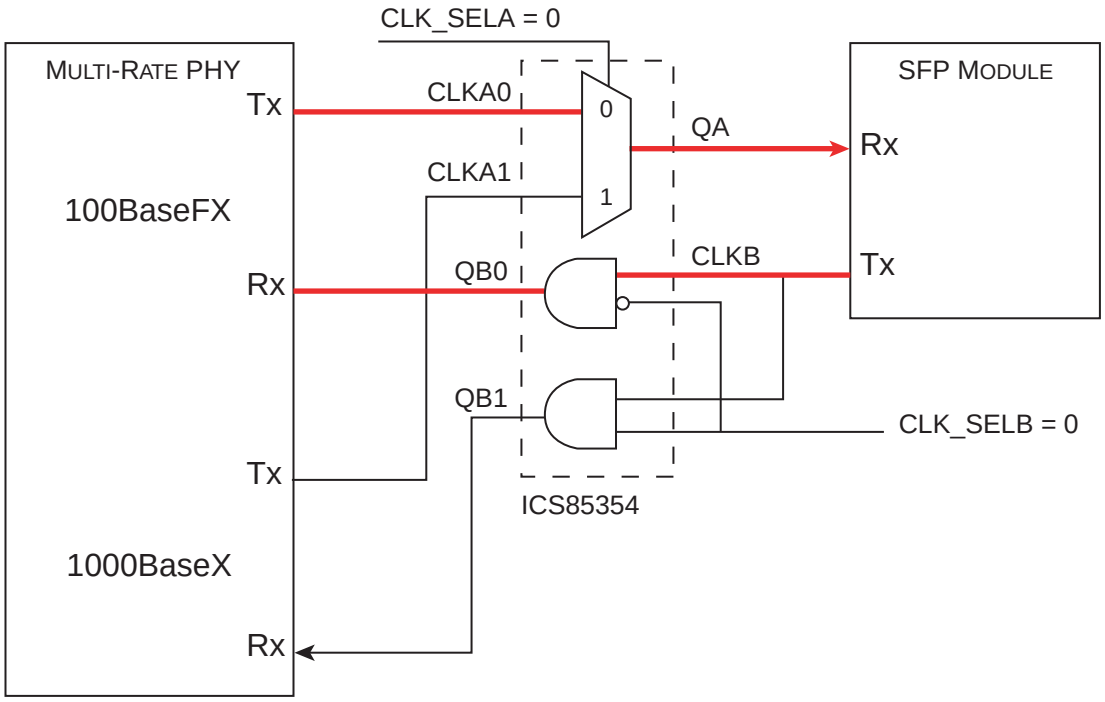
Problem Addressed: How to map the 2 Tx/Rx pairs of the multi-rate PHY to the single Tx/Rx pair on the SFP Module.



Mode 1, 100BaseX Connected to SFP

All lines are differential pairs, but drawn as single-ended to simplify the drawing.

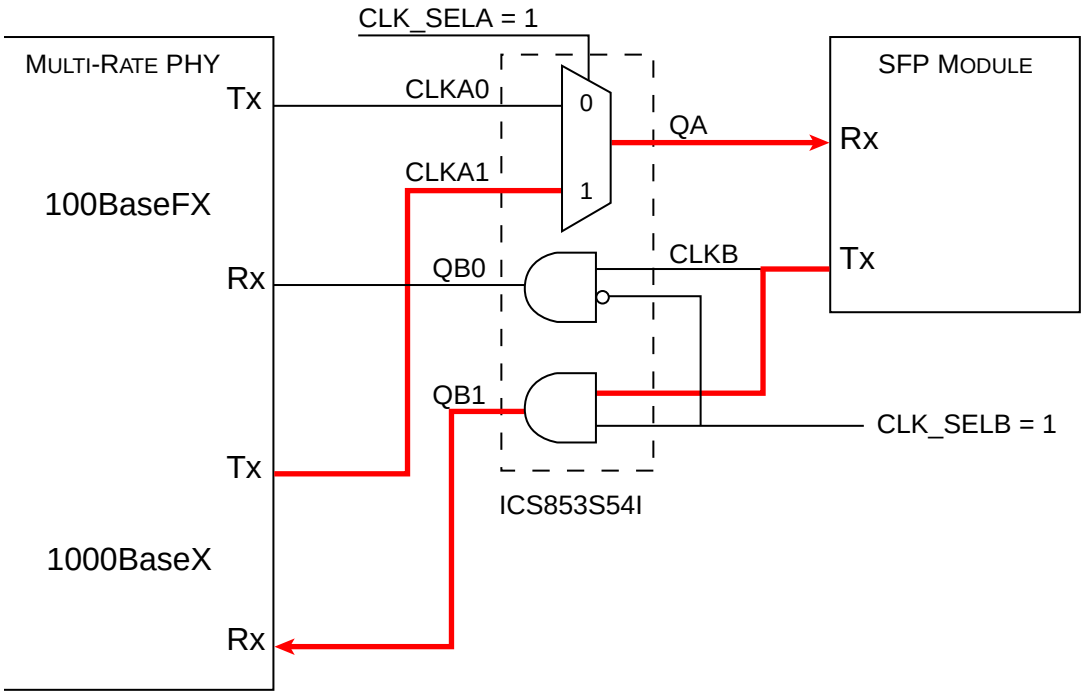
Bold red lines ——— are active connections highlighting the signal path.



Mode 2, 100BaseX Connected to SFP

All lines are differential pairs, but drawn as single-ended to simplify the drawing.

Bold red lines ——— are active connections highlighting the signal path.



Power Considerations

This section provides information on power dissipation and junction temperature for the ICS853S54I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS853S54I is the sum of the core power plus the power dissipation in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 45mA = **155.925mW**
- Power $(outputs)_{MAX}$ = **32mW/Loaded Output pair**
  If all outputs are loaded, the total power is 3 * 32mW = **96mW**

Total Power$_{\_MAX}$ (3.3V, with all outputs switching) = 155.925mW + 96mW = **251.925mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 74.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.252W * 74.7°C/W = 103.8°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 6. Thermal Resistance θ_{JA} for 16 Lead VFQFN, Forced Convection

θ_{JA} **by Velocity**			
Meters per Second	**0**		
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

The LVPECL output driver circuit and termination are shown in *Figure 7.*

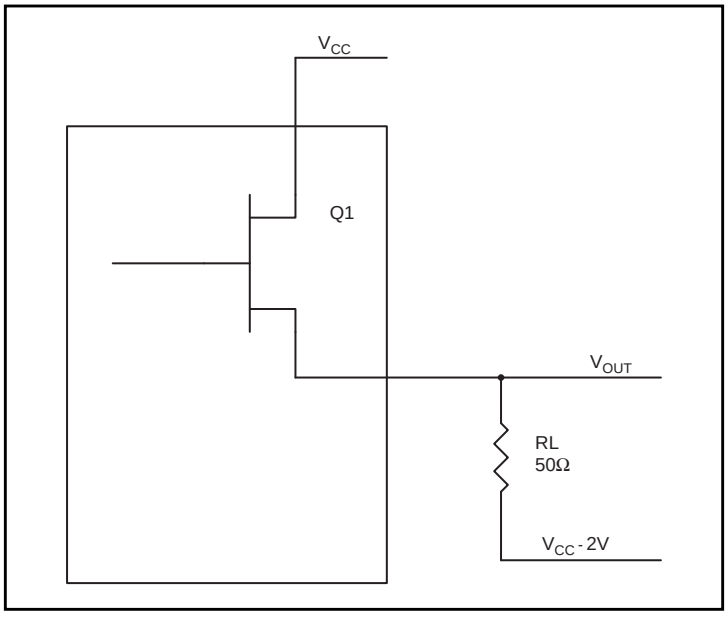


Figure 7. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.875V}$
  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{0.875V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.62V}$
  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.62V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.875V)/50Ω] * 0.875V =$ **19.69mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.62V)/50Ω] * 1.62V =$ **12.31mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **32mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 16 Lead VFQFN

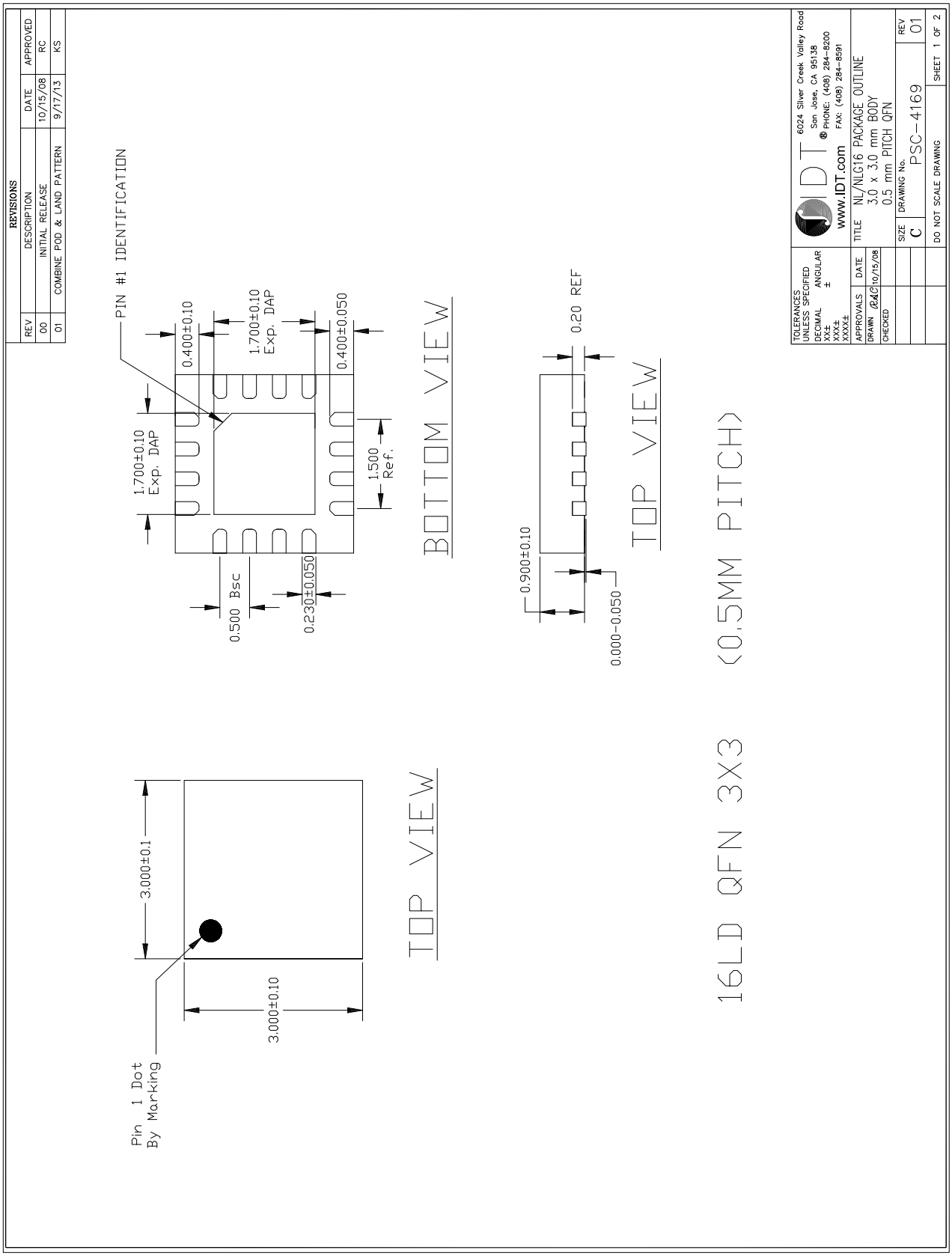
θ_{JA} by Velocity			
Meters per Second	**0**		
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

Transistor Count

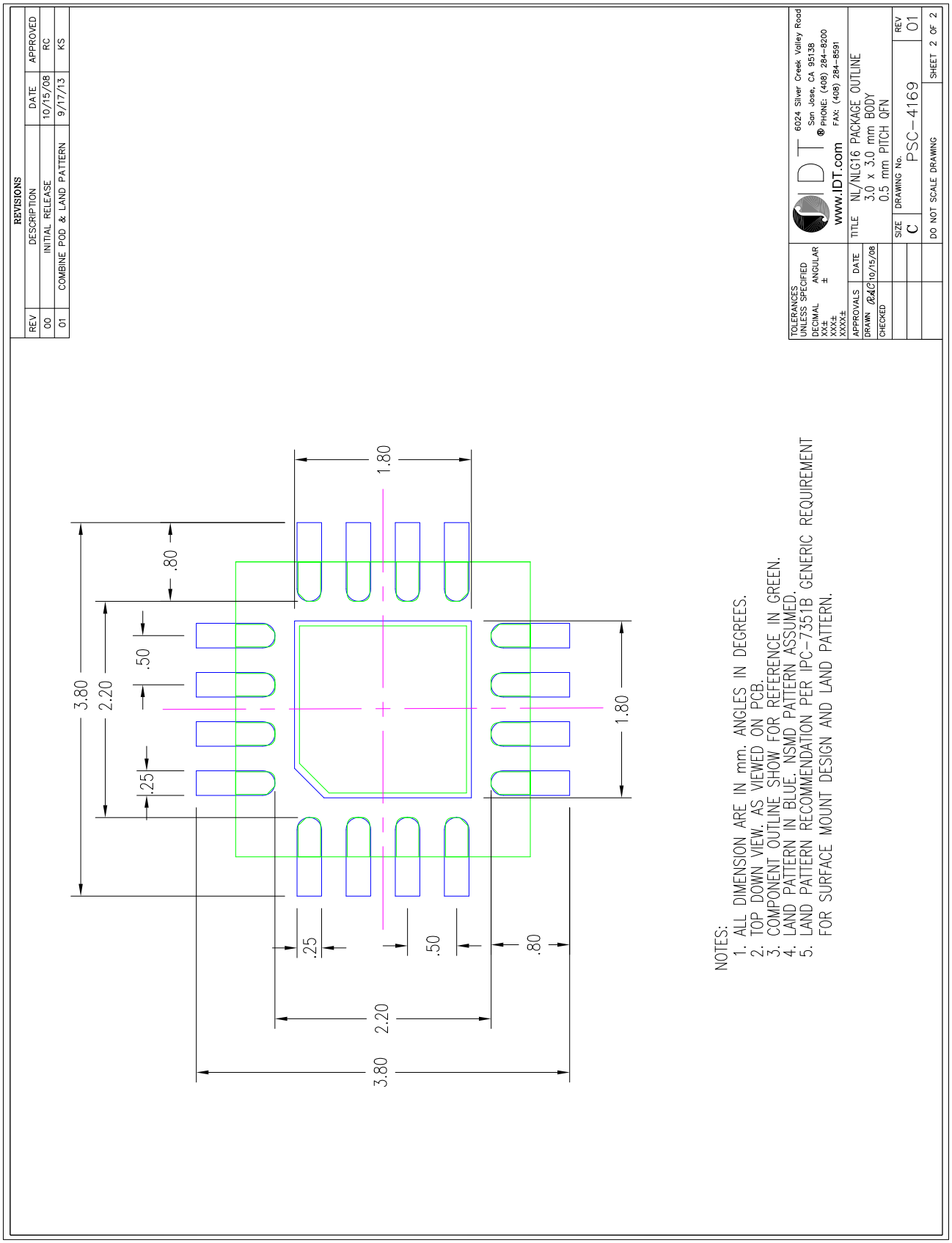
The transistor count for ICS853S54I is: 296

This is a suggested replacement for ICS85354

Package Outline Drawings (Sheet 1)



Package Outline Drawings (Sheet 2)



Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
853S54AKILF	S54A	“Lead-Free” 16 Lead VFQFN	Tube	-40°C to 85°C
853S54AKILFT	S54A	“Lead-Free” 16 Lead VFQFN	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T9	1 8 19	Deleted HiperClockS Logo. Added CML to 3rd bullet. Added figures 2D, 2E and 2F. Deleted quantity from tape and reel.	10/30/2012
B	-	18	Updated the package outline drawings.	5/27/2017

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.