

## GENERAL DESCRIPTION

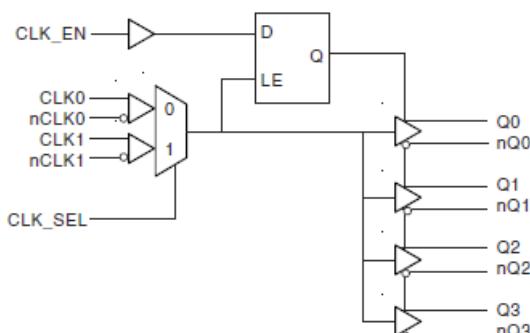
The 8523I-03 is a low skew, high performance 1-to-4 Differential-to-LVHSTL fanout buffer. The 8523I-03 has two selectable clock inputs. The input pairs can accept most standard differential input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the 8523I-03 ideal for those applications demanding well defined performance and repeatability.

## FEATURES

- 4 differential LVHSTL compatible outputs
- Selectable differential CLK0, nCLK0 and CLK1, nCLK1 clock inputs
- Clock input pairs can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency: 650MHz
- Translates any single-ended input signal to LVHSTL levels with resistor bias on nCLK input
- Output skew: 50ps (maximum)
- Part-to-part skew: 400ps (maximum)
- Propagation delay: 1.2ns (typical)
- $V_{OH} = 1V$  (maximum)
- 3.3V core, 1.8V output operating supply
- Lead-Free package available
- -40°C to 85°C ambient operating temperature

## BLOCK DIAGRAM



## PIN ASSIGNMENT

|                 |    |    |                  |
|-----------------|----|----|------------------|
| GND             | 1  | 20 | Q0               |
| CLK_EN          | 2  | 19 | nQ0              |
| CLK_SEL         | 3  | 18 | V <sub>DDO</sub> |
| CLK0            | 4  | 17 | Q1               |
| nCLK0           | 5  | 16 | nQ1              |
| CLK1            | 6  | 15 | Q2               |
| nCLK1           | 7  | 14 | nQ2              |
| nc              | 8  | 13 | V <sub>DDO</sub> |
| nc              | 9  | 12 | Q3               |
| V <sub>DD</sub> | 10 | 11 | nQ3              |

**8523I-03**  
20-Lead TSSOP  
6.5mm x 4.4mm x 0.92mm body package  
**G Package**  
Top View

**TABLE 1. PIN DESCRIPTIONS**

| Number | Name             | Type   |          | Description  |
|--------|------------------|--------|----------|--|
| 1      | GND              | Power  |          | Power supply ground.   |
| 2      | CLK_EN           | Input  | Pullup   | Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Q outputs are forced low, nQ outputs are forced high. LVCMS / LVTTL interface levels. |
| 3      | CLK_SEL          | Input  | Pulldown | Clock select input. When HIGH, selects differential CLK1, nCLK1 inputs. When LOW, selects CLK0, nCLK0 inputs. LVCMS / LVTTL interface levels.                            |
| 4      | CLK0             | Input  | Pulldown | Non-inverting differential clock input.  |
| 5      | nCLK0            | Input  | Pullup   | Inverting differential clock input.  |
| 6      | CLK1             | Input  | Pulldown | Non-inverting differential clock input.  |
| 7      | nCLK1            | Input  | Pullup   | Inverting differential clock input.  |
| 8, 9   | nc               | Unused |          | No connect.  |
| 10     | V <sub>DD</sub>  | Power  |          | Core supply pin.   |
| 11, 12 | nQ3, Q3          | Output |          | Differential output pair. LVHSTL interface levels.   |
| 13, 18 | V <sub>DDO</sub> | Power  |          | Output supply pins.  |
| 14, 15 | nQ2, Q2          | Output |          | Differential output pair. LVHSTL interface levels.   |
| 16, 17 | nQ1, Q1          | Output |          | Differential output pair. LVHSTL interface levels.   |
| 19, 20 | nQ0, Q0          | Output |          | Differential output pair. LVHSTL interface levels.   |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

| Symbol                | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C <sub>IN</sub>       | Input Capacitance       |                 |         |         | 4       | pF    |
| R <sub>PULLUP</sub>   | Input Pullup Resistor   |                 |         | 51      |         | KΩ    |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor |                 |         | 51      |         | KΩ    |

TABLE 3A. CONTROL INPUT FUNCTION TABLE

| Inputs |         |                 | Outputs       |                |
|--------|---------|-----------------|---------------|----------------|
| CLK_EN | CLK_SEL | Selected Source | Q0:Q3         | nQ0:nQ3        |
| 0      | 0       | CLK0, nCLK0     | Disabled; LOW | Disabled; HIGH |
| 0      | 1       | CLK1, nCLK1     | Disabled; LOW | Disabled; HIGH |
| 1      | 0       | CLK0, nCLK0     | Enabled       | Enabled        |
| 1      | 1       | CLK1, nCLK1     | Enabled       | Enabled        |

After CLK\_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1.

In the active mode, the state of the outputs are a function of the CLK0, nCLK0 and CLK1, nCLK1 inputs as described in Table 3B.

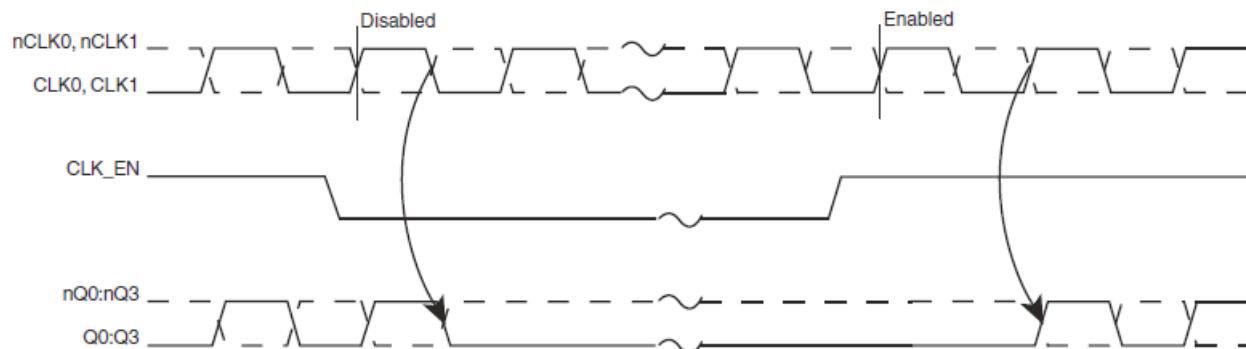


FIGURE 1. CLK\_EN TIMING DIAGRAM

TABLE 3B. CLOCK INPUT FUNCTION TABLE

| Inputs         |                | Outputs |         | Input to Output Mode         | Polarity      |
|----------------|----------------|---------|---------|------------------------------|---------------|
| CLK0 or CLK1   | nCLK0 or nCLK1 | Q0:Q3   | nQ0:nQ3 |                              |               |
| 0              | 0              | LOW     | HIGH    | Differential to Differential | Non Inverting |
| 1              | 1              | HIGH    | LOW     | Differential to Differential | Non Inverting |
| 0              | Biased; NOTE 1 | LOW     | HIGH    | Single Ended to Differential | Non Inverting |
| 1              | Biased; NOTE 1 | HIGH    | LOW     | Single Ended to Differential | Non Inverting |
| Biased; NOTE 1 | 0              | HIGH    | LOW     | Single Ended to Differential | Inverting     |
| Biased; NOTE 1 | 1              | LOW     | HIGH    | Single Ended to Differential | Inverting     |

NOTE 1: Please refer to the Application Information section, "Wiring the Differential Input to Accept Single Ended Levels".

**ABSOLUTE MAXIMUM RATINGS**

|  |                          |
|--|--------------------------|
| Supply Voltage, $V_{CC}$                 | 4.6V                     |
| Inputs, $V_I$                            | -0.5V to $V_{CC} + 0.5V$ |
| Outputs, $I_O$                           |                          |
| Continuous Current                       | 50mA                     |
| Surge Current                            | 100mA                    |
| Package Thermal Impedance, $\theta_{JA}$ | 73.2°C/W (0 lfpm)        |
| Storage Temperature, $T_{STG}$           | -65°C to 150°C           |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$** 

| Symbol    | Parameter                   | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$  | Core Supply Voltage         |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{DDO}$ | Output Power Supply Voltage |                 | 1.6     | 1.8     | 2.0     | V     |
| $I_{DD}$  | Power Supply Current        |                 |         |         | 55      | mA    |

**TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$** 

| Symbol   | Parameter          | Test Conditions        | Minimum                           | Typical | Maximum        | Units   |
|----------|--------------------|------------------------|-----------------------------------|---------|----------------|---------|
| $V_{IH}$ | Input High Voltage | $CLK\_EN$ , $CLK\_SEL$ | 2                                 |         | $V_{DD} + 0.3$ | V       |
| $V_{IL}$ | Input Low Voltage  | $CLK\_EN$ , $CLK\_SEL$ | -0.3                              |         | 0.8            | V       |
| $I_{IH}$ | Input High Current | $CLK\_EN$              | $V_{DD} = V_{IN} = 3.465V$        |         | 5              | $\mu A$ |
|          |                    | $CLK\_SEL$             | $V_{DD} = V_{IN} = 3.465V$        |         | 150            | $\mu A$ |
| $I_{IL}$ | Input Low Current  | $CLK\_EN$              | $V_{DD} = 3.465V$ , $V_{IN} = 0V$ | -150    |                | $\mu A$ |
|          |                    | $CLK\_SEL$             | $V_{DD} = 3.465V$ , $V_{IN} = 0V$ | -5      |                | $\mu A$ |

**TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$** 

| Symbol    | Parameter                               | Test Conditions   | Minimum                           | Typical | Maximum         | Units   |
|-----------|---|-------------------|-----------------------------------|---------|-----------------|---------|
| $I_{IH}$  | Input High Current                      | $nCLK0$ , $nCLK1$ | $V_{DD} = V_{IN} = 3.465V$        |         | 5               | $\mu A$ |
|           |   | $CLK0$ , $CLK1$   | $V_{DD} = V_{IN} = 3.465V$        |         | 150             | $\mu A$ |
| $I_{IL}$  | Input Low Current                       | $nCLK0$ , $nCLK1$ | $V_{DD} = 3.465V$ , $V_{IN} = 0V$ | -150    |                 | $\mu A$ |
|           |   | $CLK0$ , $CLK1$   | $V_{DD} = 3.465V$ , $V_{IN} = 0V$ | -5      |                 | $\mu A$ |
| $V_{PP}$  | Peak-to-Peak Input Voltage              |                   | 0.15                              |         | 1.3             | V       |
| $V_{CMR}$ | Common Mode Input Voltage;<br>NOTE 1, 2 |                   | 0.5                               |         | $V_{DD} - 0.85$ | V       |

NOTE 1: For single ended applications the maximum input voltage for  $CLK0$ ,  $nCLK0$  and  $CLK1$ ,  $nCLK1$  is  $V_{DD} + 0.3V$ .

NOTE 2: Common mode voltage is defined as  $V_{IH}$ .

**TABLE 4D. LVHSTL DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$** 

| Symbol      | Parameter                         | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|-----------------------------------|-----------------|---------|---------|---------|-------|
| $V_{OH}$    | Output High Voltage; NOTE 1       |                 | 0.7     |         | 1.0     | V     |
| $V_{OL}$    | Output Low Voltage; NOTE 1        |                 | 0       |         | 0.4     | V     |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing |                 | 0.4     |         | 1.0     | V     |

NOTE 1: Outputs terminated with  $50\Omega$  to ground.

**TABLE 5. AC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$** 

| Symbol      | Parameter                    | Test Conditions        | Minimum | Typical | Maximum | Units |
|-------------|------------------------------|------------------------|---------|---------|---------|-------|
| $f_{MAX}$   | Maximum Output Frequency     |                        |         |         | 650     | MHz   |
| $t_{PD}$    | Propagation Delay; NOTE 1    | $f \leq 650\text{MHz}$ | 0.9     | 1.2     | 1.5     | ns    |
| $tsk(o)$    | Output Skew; NOTE 2, 4       |                        |         |         | 50      | ps    |
| $tsk(pp)$   | Part-to-Part Skew; NOTE 3, 4 |                        |         |         | 400     | ps    |
| $t_R / t_F$ | Output Rise/Fall Time        | 20% to 80%             | 150     |         | 500     | ps    |
| odc         | Output Duty Cycle            | $f > 200\text{MHz}$    | 45      | 50      | 55      | %     |
|             |                              | $f \leq 200\text{MHz}$ | 48      |         | 52      | %     |

All parameters measured at 500MHz unless noted otherwise.

The cycle to cycle jitter on the input will equal the jitter on the output. The part does not add jitter.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

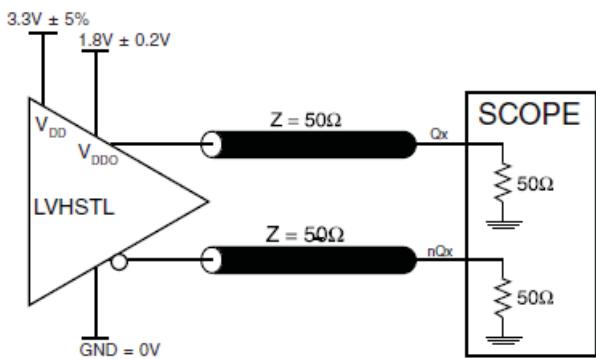
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at output differential cross points.

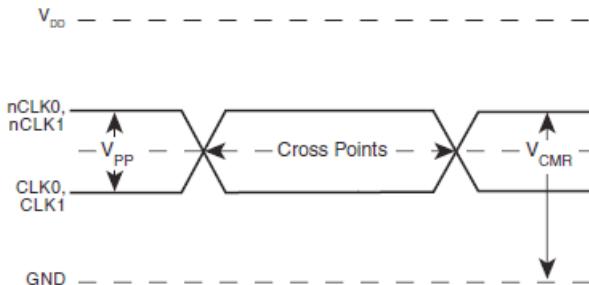
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

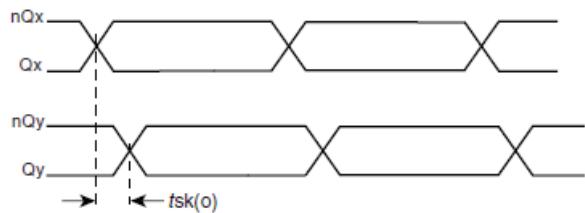
## PARAMETER MEASUREMENT INFORMATION



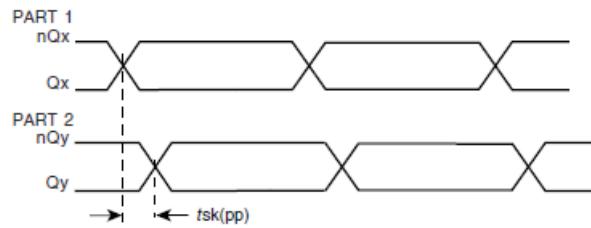
3.3V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



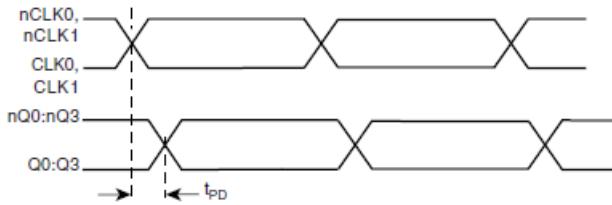
DIFFERENTIAL INPUT LEVEL



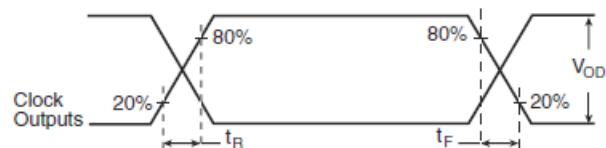
OUTPUT SKEW



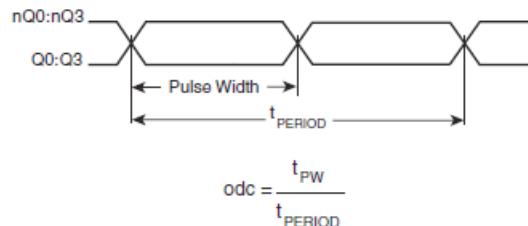
PART-TO-PART SKEW



PROPAGATION DELAY



OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

## APPLICATION INFORMATION

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio

of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{DD} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .

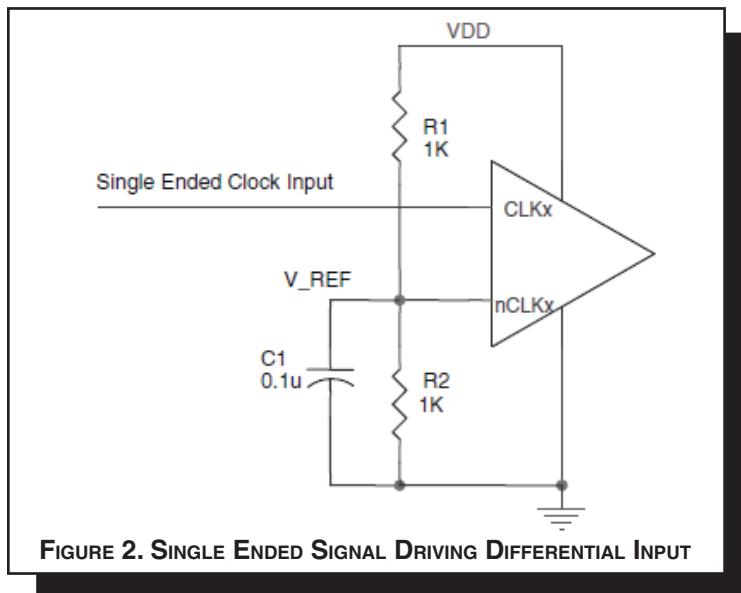
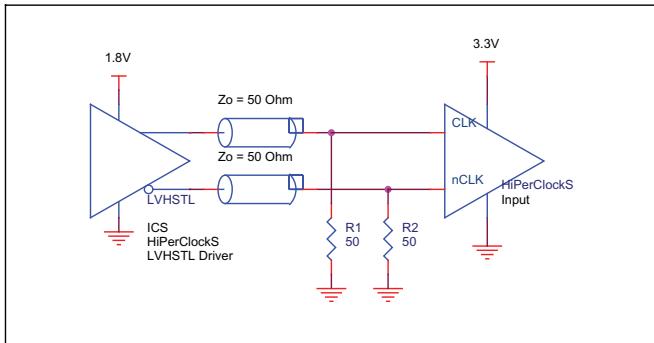


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

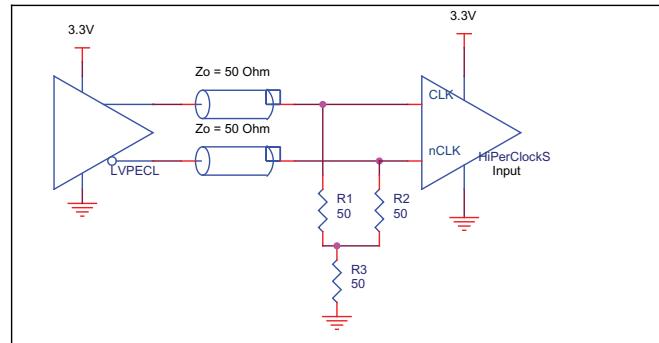
## DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 3A to 3E show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are

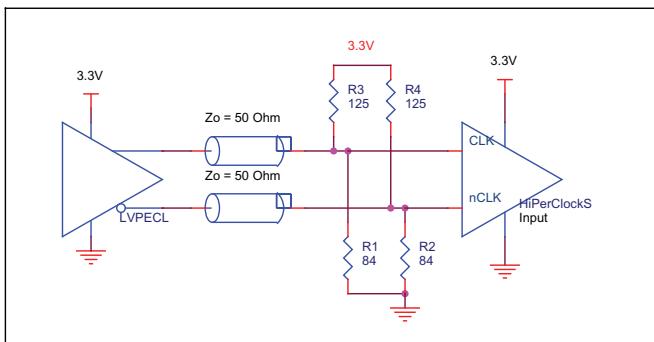
examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 4A*, the input termination applies for LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



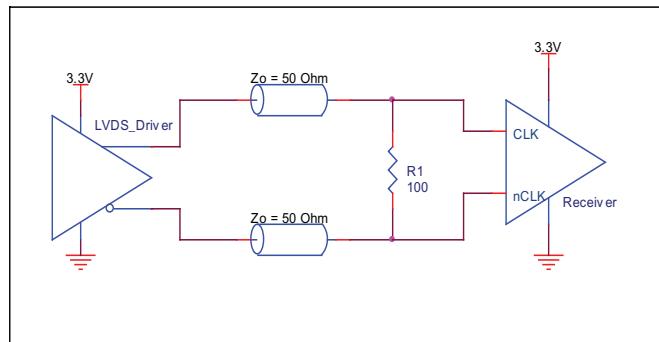
**FIGURE 3A. CLK/nCLK INPUT DRIVEN BY LVHSTL DRIVER**



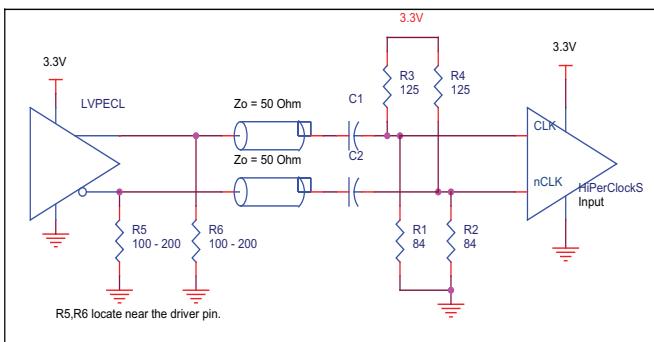
**FIGURE 3B. CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



**FIGURE 3C. CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



**FIGURE 3D. CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER**



**FIGURE 3E. CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE**

## SCHEMATIC EXAMPLE

This application note provides general design guide using 8523I-03 LVHSTL buffer. Figure 3 shows a schematic example of the 8523I-03 LVHSTL Clock buffer. In this example, the input

is driven by an LVHSTL driver. CLK\_EN is set at logic low to select CLK0/nCLK0 input.

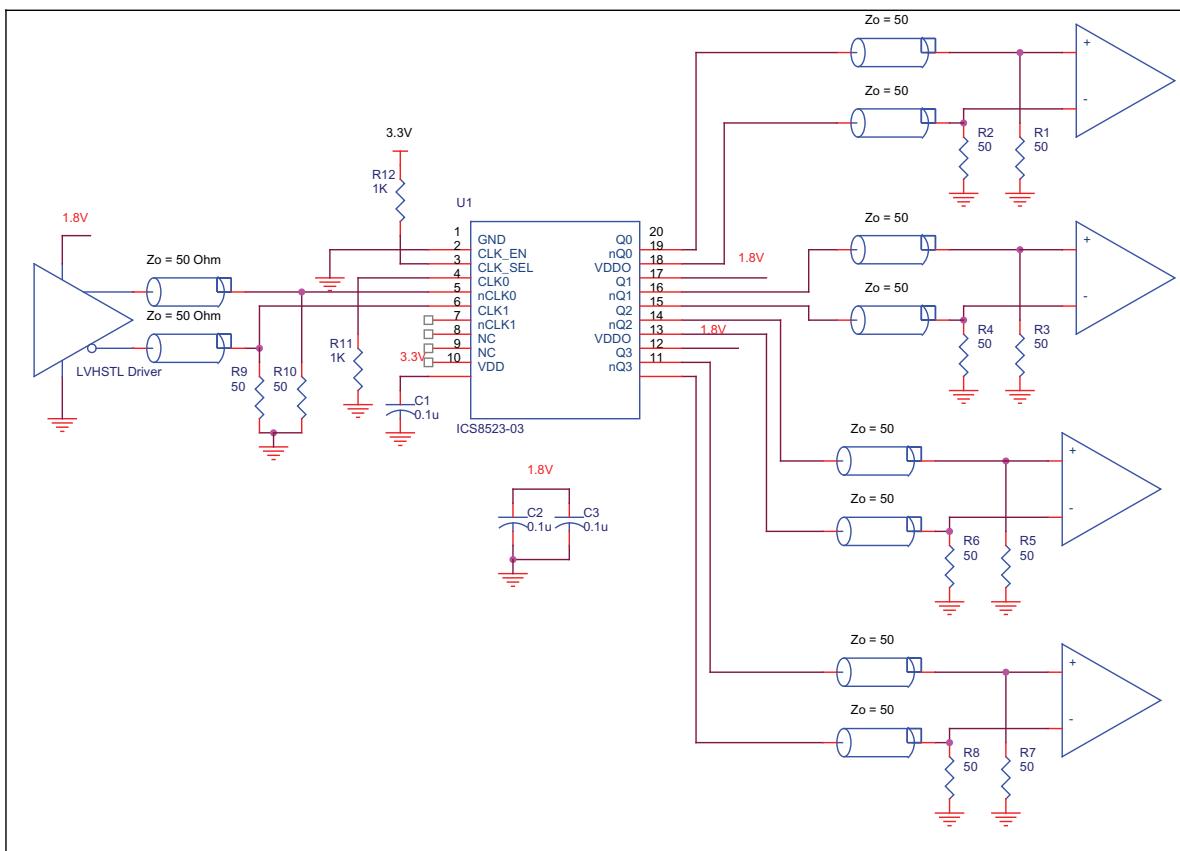


FIGURE 4. EXAMPLE 8523I-03 LVHSTL CLOCK OUTPUT BUFFER SCHEMATIC

## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 8523I-03. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 8523I-03 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * I_{DD\_MAX} = 3.465V * 55mA = 190mW$
- Power (outputs)<sub>MAX</sub> = **32.8mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $4 * 32.8mW = 131mW$

**Total Power<sub>MAX</sub>** (3.465V, with all outputs switching) =  $190mW + 131mW = 321mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for the devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * P_{d\_total} + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$P_{d\_total}$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below. Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$85^\circ\text{C} + 0.321\text{W} * 66.6^\circ\text{C/W} = 106.4^\circ\text{C}$ . This is well below the limit of 125°C.

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

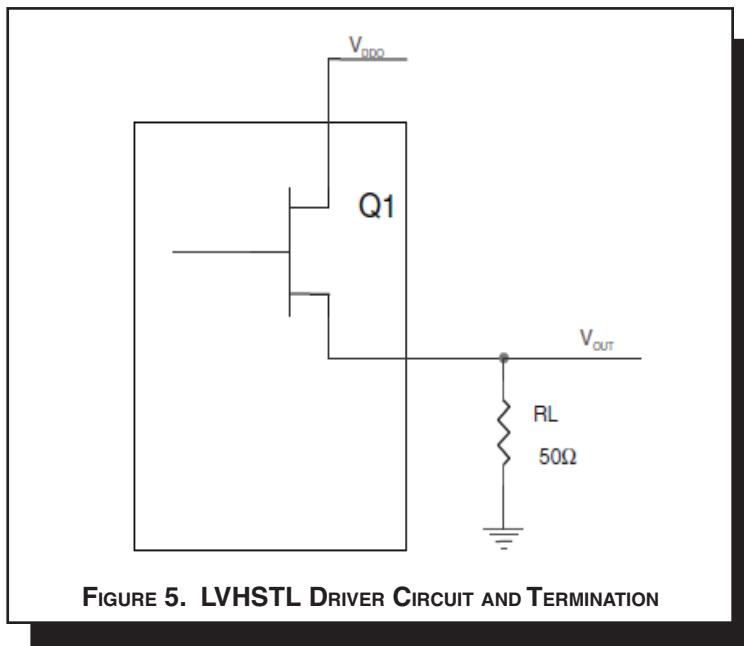
**TABLE 6. THERMAL RESISTANCE  $\theta_{JA}$  FOR 20-PIN TSSOP, FORCED CONVECTION**

| <b><math>\theta_{JA}</math> by Velocity (Linear Feet per Minute)</b>  |           |            |            |
|---|-----------|------------|------------|
|   | <b>0</b>  | <b>200</b> | <b>500</b> |
| Single-Layer PCB, JEDEC Standard Test Boards  | 114.5°C/W | 98.0°C/W   | 88.0°C/W   |
| Multi-Layer PCB, JEDEC Standard Test Boards   | 73.2°C/W  | 66.6°C/W   | 63.5°C/W   |
| <b>NOTE:</b> Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs. |           |            |            |

### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVHSTL output driver circuit and termination are shown in *Figure 5*.



To calculate worst case power dissipation into the load, use the following equations which assume a  $50\Omega$  load.

$Pd_H$  is power dissipation when the output drives high.

$Pd_L$  is the power dissipation when the output drives low.

$$Pd_H = (V_{OH\_MAX}/R_L) * (V_{DDO\_MAX} - V_{OH\_MAX})$$

$$Pd_L = (V_{OL\_MAX}/R_L) * (V_{DDO\_MAX} - V_{OL\_MAX})$$

$$Pd_H = (1V/50\Omega) * (2V - 1V) = 20mW$$

$$Pd_L = (0.4V/50\Omega) * (2V - 0.4V) = 12.8mW$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = 32.8mW$$

## RELIABILITY INFORMATION

**TABLE 7.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 20 LEAD TSSOP**

**$\theta_{JA}$  by Velocity (Linear Feet per Minute)**

|  | <b>0</b>  | <b>200</b> | <b>500</b> |
|--|-----------|------------|------------|
| Single-Layer PCB, JEDEC Standard Test Boards | 114.5°C/W | 98.0°C/W   | 88.0°C/W   |
| Multi-Layer PCB, JEDEC Standard Test Boards  | 73.2°C/W  | 66.6°C/W   | 63.5°C/W   |

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for 8523I-03 is: 472

## PACKAGE OUTLINE - G SUFFIX FOR 20 LEAD TSSOP

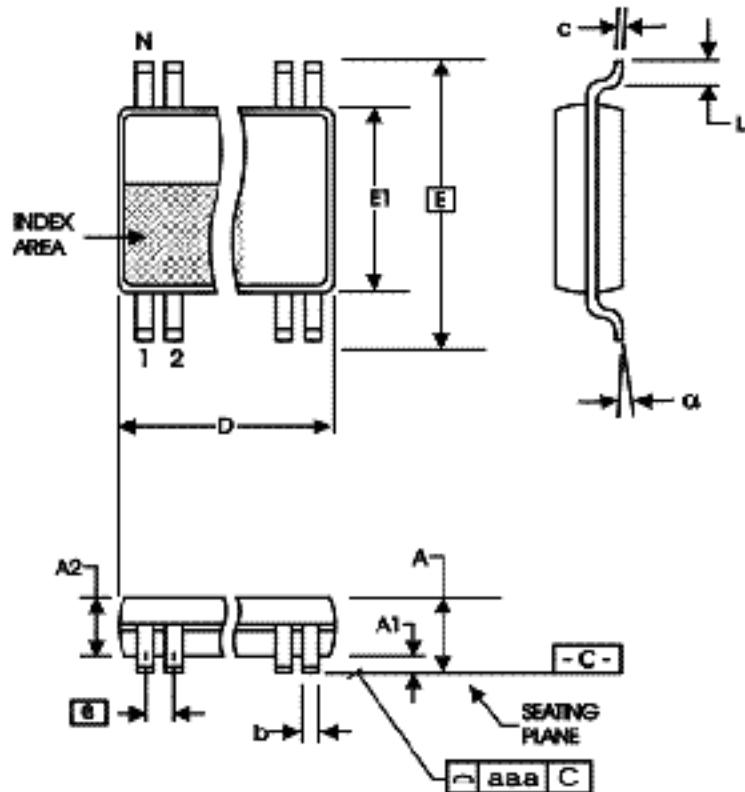


TABLE 8. PACKAGE DIMENSIONS

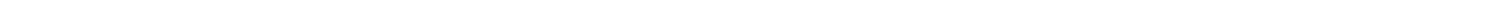
| SYMBOL   | Millimeters |           |
|----------|-------------|-----------|
|          | Minimum     | Maximum   |
| N        | 20          |           |
| A        | --          | 1.20      |
| A1       | 0.05        | 0.15      |
| A2       | 0.80        | 1.05      |
| b        | 0.19        | 0.30      |
| c        | 0.09        | 0.20      |
| D        | 6.40        | 6.60      |
| E        | 6.40 BASIC  |           |
| E1       | 4.30        | 4.50      |
| e        | 0.65 BASIC  |           |
| L        | 0.45        | 0.75      |
| $\alpha$ | $0^\circ$   | $8^\circ$ |
| aaa      | --          | 0.10      |

Reference Document: JEDEC Publication 95, MS-153

**TABLE 9. ORDERING INFORMATION**

| Part/Order Number | Marking      | Package                   | Shipping Packaging | Temperature   |
|-------------------|--------------|---------------------------|--------------------|---------------|
| 8523AGI-03LN      | ICS8523AI03L | 20 lead "Lead-Free" TSSOP | tube               | -40°C to 85°C |
| 8523AGI-03LNT     | ICS8523AI03L | 20 lead "Lead-Free" TSSOP | Tape and Reel      | -40°C to 85°C |

| REVISION HISTORY SHEET |       |              |  |         |
|------------------------|-------|--------------|--|---------|
| Rev                    | Table | Page         | Description of Change  | Date    |
| A                      | T9    | 1<br>8<br>14 | Features section - added Lead-Free bullet.<br>Updated Differential Clock Input Interface section and deleted LVPECL Clock Input Interface section.<br>Added Lead-Free marking to Ordering Information table. | 9/13/04 |
| A                      | T9    | 14           | Ordering Information Table - corrected Lead-Free Part Number from "LF" to "LN".  | 10/5/04 |
| A                      | T9    | 14<br>16     | Updated datasheet's header/footer with IDT from ICS.<br>Removed ICS prefix from Part/Order Number column.<br>Added Contact Page.   | 8/12/10 |
| A                      | T9    | 14           | Ordering Information - removed leaded devices.<br>Updated data sheet format.   | 11/9/15 |

**Corporate Headquarters**

6024 Silver Creek Valley Road  
San Jose, California 95138

**Sales**

800-345-7015 or +408-284-8200  
Fax: 408-284-2775  
[www.IDT.com](http://www.IDT.com)

**Technical Support**

**email:** [clocks@idt.com](mailto:clocks@idt.com)

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### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

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