

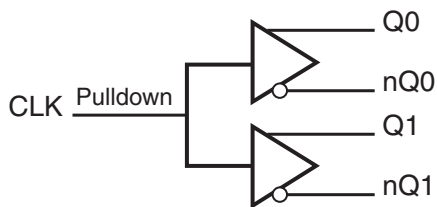
General Description

The ICS85222I-02 is a 1-to-2 LVCMOS / LVTTL-to- Differential HSTL translator. The ICS85222I-02 has one single-ended clock input. The single-ended clock input accepts LVCMOS or LVTTL input levels and translates them to HSTL levels. The small outline 8-pin SOIC package makes this device ideal for applications where space, high performance and low power are important.

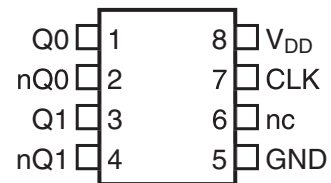
Features

- Two differential HSTL outputs
- One LVCMOS/LVTTL clock input
- CLK input can accept the following input levels: LVCMOS or LVTTL
- Maximum output frequency: 350MHz
- Part-to-part skew: 500ps (maximum)
- Propagation delay: 1.55ns (maximum)
- V_{OH} : 1.4V (maximum)
- Output crossover voltage: 0.5V - 0.9V
- Full 3.3V operating supply voltage
- -40°C to 85°C ambient operating temperature
- Lead-free RoHS compliant packaging

Block Diagram



Pin Assignment



ICS85222I-02

8-Lead SOIC

3.90mm x 4.92mm x 1.37mm body package

M Package

Top View

Pin Descriptions and Characteristics

Table 1. Pin Descriptions

Number	Name	Type		Description
1	Q0	Output		Differential output pair. HSTL interface levels.
2	nQ0	Output		Differential output pair. HSTL interface levels.
3	Q1	Output		Differential output pair. HSTL interface levels.
4	nQ1	Output		Differential output pair. HSTL interface levels.
5	GND	Power		Power supply ground.
6	nc	Unused		No connect
7	CLK	Input	Pulldown	LVC MOS / LV TTL clock input.
8	V _{DD}	Power		Positive supply pin.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

NOTE: Unused output pairs must be terminated.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
R _{PULLDOWN}	Input Pulldown Resistor			51		kΩ

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to $V_{DD} + 0.5V$
Outputs, I_O Continuous Current Surge Current	50mA 100mA
Junction Temperature, T_J	125°C
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current	Outputs not loaded			50	mA

Table 3B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	CLK $V_{DD} = V_{IN} = 3.465V$			150	μA
I_{IL}	Input Low Current	CLK $V_{DD} = 3.465V, V_{IN} = 0V$	-5			μA

Table 3C. HSTL DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		1.0		1.4	V
V_{OL}	Output Low Voltage; NOTE 1		0		0.4	V
V_{OX}	Output Crossover Voltage		0.5		0.9	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6	1.0	1.4	V

NOTE 1: All outputs must be terminated with 50Ω to ground.

AC Electrical Characteristics

Table 4. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				350	MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq 350MHz$	1.0		1.55	ns
$t_{sk(o)}$	Output Skew; NOTE 2, 3				35	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 4				500	ps
t_R/t_F	Output Rise/Fall Time	20% to 80%	225		700	ps
odc	Output Duty Cycle	$f \leq 250MHz$	40		60	%
		$f > 250MHz$	35		65	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All outputs must be terminated with 50Ω to ground.

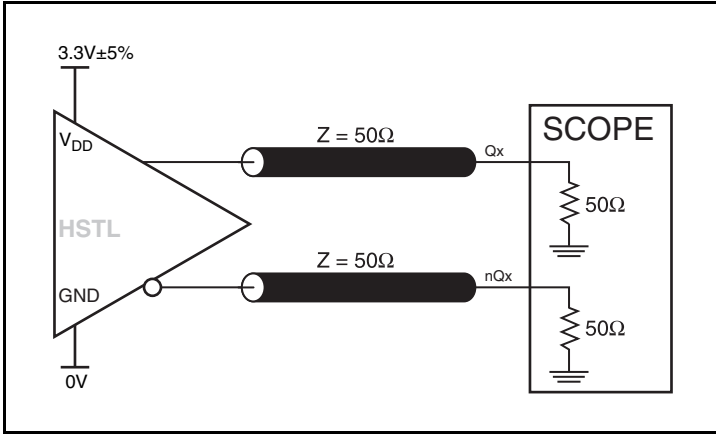
NOTE 1: Measured from $V_{DD}/2$ of the input to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

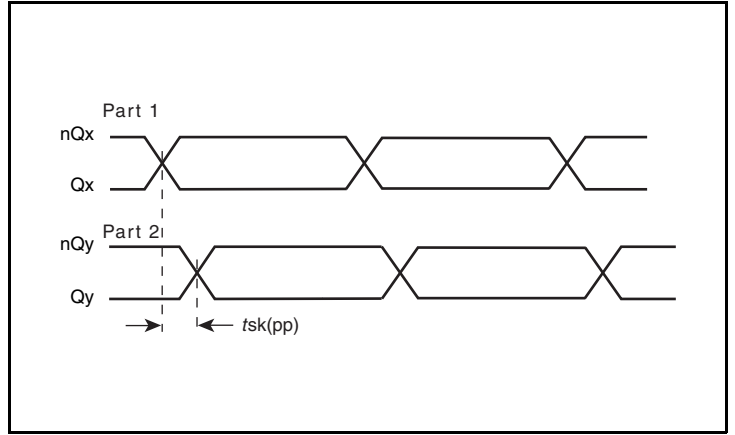
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoints.

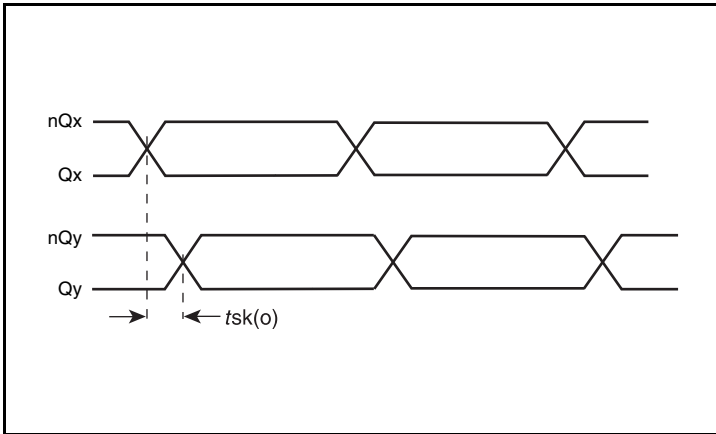
Parameter Measurement Information



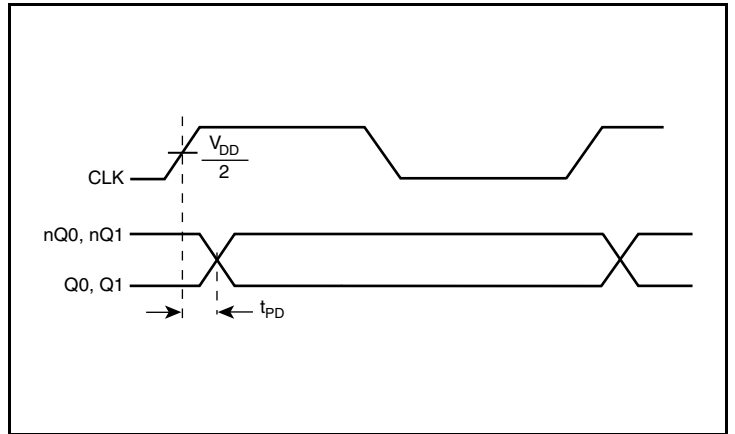
3.3V Core/3.3V Output Load AC Test Circuit



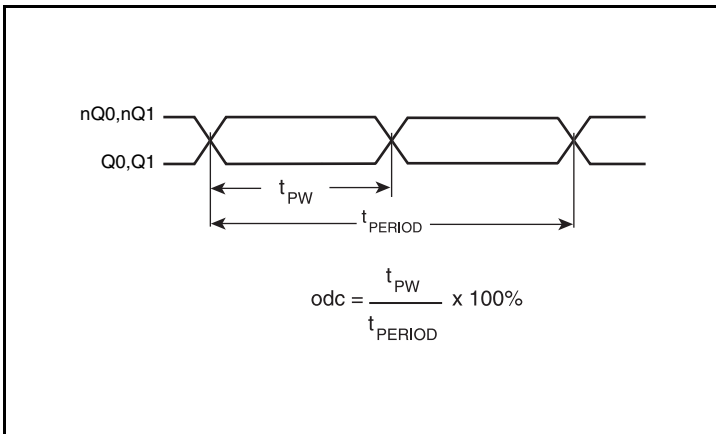
Part-to-Part Skew



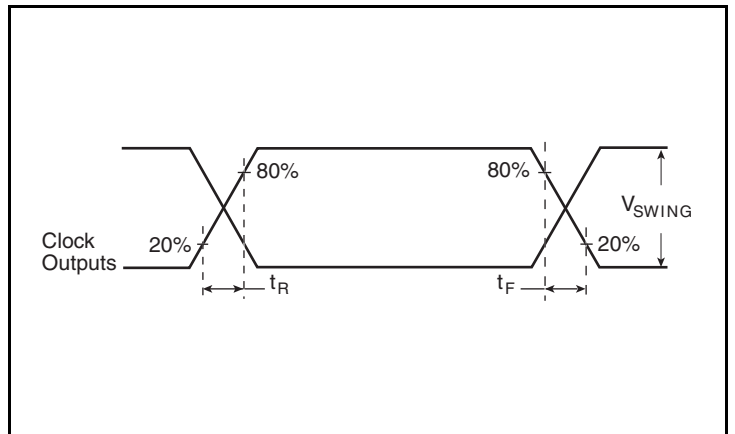
Output Skew



Propagation Delay



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Application Information

Recommendations for Unused Input and Output Pins

Outputs:

HSTL Outputs

All outputs must be terminated with 50Ω to ground.

Schematic Example

Figure 1 shows a schematic example of ICS85222I-02. In the example, the input is driven by a 7Ω LVCMOS driver with a series termination. The decoupling capacitor should be physically located

near the power pin. For ICS85222I-02, the unused output need to be terminated.

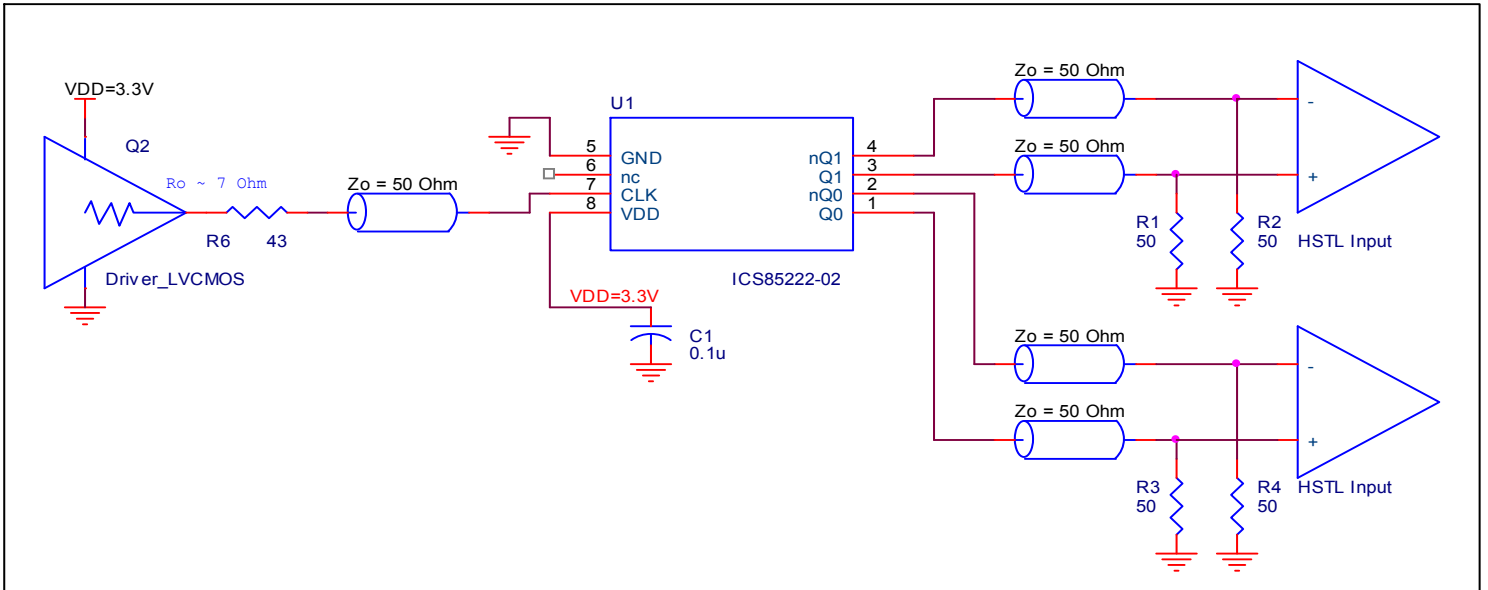


Figure 1. ICS85222I-02 HSTL Buffer Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS85222I-02. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS85222I-02 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{DD_MAX} * I_{DD_MAX} = 3.465V * 50mA = 173.25mW$
- Power (outputs)_{MAX} = **82.3mW/Loaded Output pair**
If all outputs are loaded, the total power is $2 * 82.3mW = 164.6mW$

Total Power_{MAX} (3.465V, with all outputs switching) = $173.3mW + 164.6mW = 337.85mW$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 103°C/W per Table 5 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.338W * 103^\circ C/W = 119.8^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 5. Thermal Resistance θ_{JA} for 8-Lead SOIC, Forced Convection

Meters per Second	θ_{JA} by Velocity		
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	103°C/W	94°C/W	89°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

HSTL output driver circuit and termination are shown in *Figure 2*.

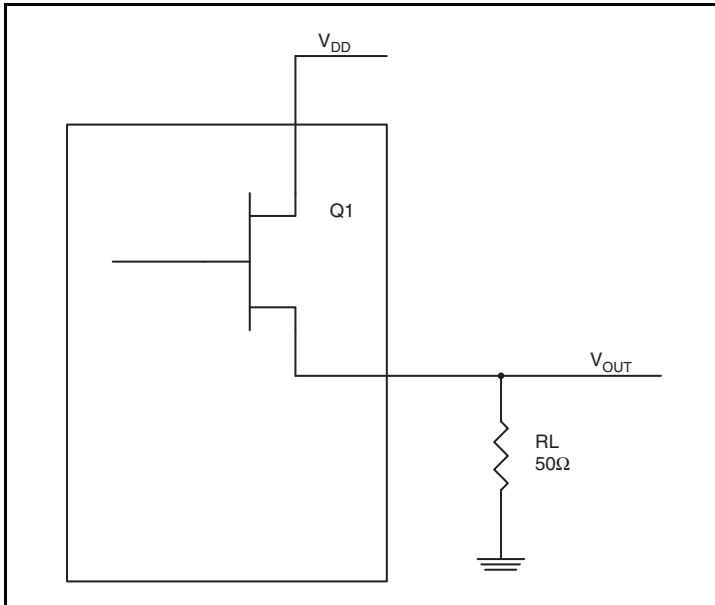


Figure 2. HSTL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = (V_{OH_MAX} / R_L) * (V_{DDO_MAX} - V_{OH_MAX})$$

$$Pd_L = (V_{OL_MAX} / R_L) * (V_{DDO_MAX} - V_{OL_MAX})$$

$$Pd_H = (1.4V / 50\Omega) * (3.465V - 1.4V) = \mathbf{57.8mW}$$

$$Pd_L = (0.4V / 50\Omega) * (3.465V - 0.4V) = \mathbf{24.52mW}$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = \mathbf{82.3mW}$$

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 8-Lead SOIC

θ_{JA} by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	103°C/W	94°C/W	89°C/W

Transistor Count

The transistor count for ICS85222i-02 is: 411

Package Outline and Package Dimension

Package Outline - M Suffix for 8-Lead SOIC

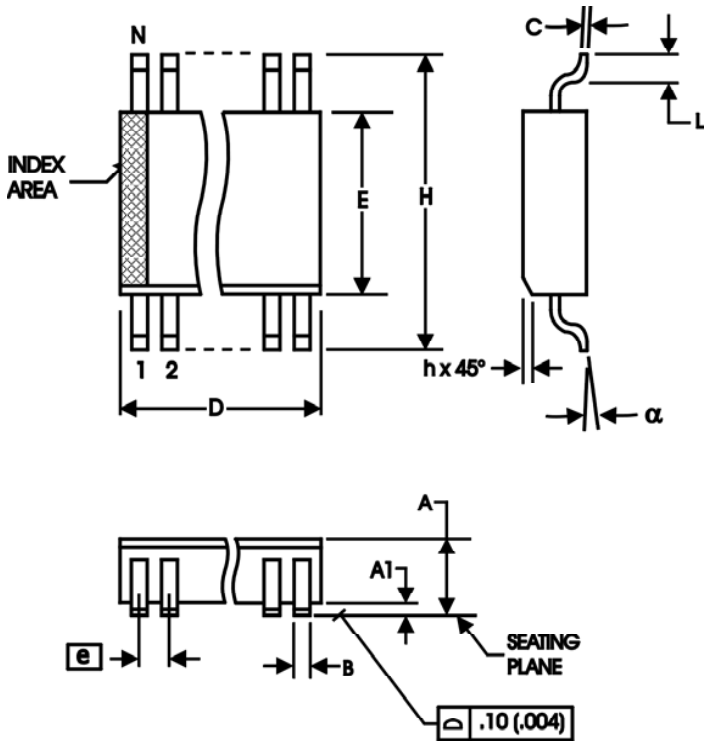


Table 7. Package Dimensions

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	1.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 Basic	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS85222AMI-02LF	222AI02L	"Lead-free" 8-Lead SOIC	Tube	-40°C to 85°C
ICS85222AMI-02LFT	222AI02L	"Lead-free" 8-Lead SOIC	Tape and Reel	-40°C to 85°C

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.