RENESAS

FemtoClock® Crystal/LVCMOS-to-LVDS/LVCMOS Frequency Synthesizer

ICS8440258-46

DATA SHEET

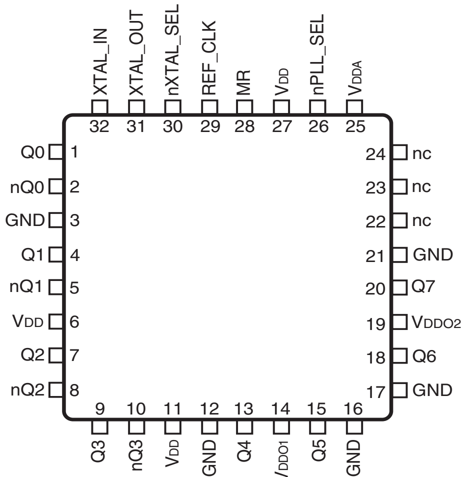
General Description

The ICS8440258-46 is an eight output synthesizer optimized to generate Ethernet clocks. The device will generate 125MHz and 25MHz clocks from a 25MHz crystal with a very good jitter performance. The ICS8440258-46 uses IDT's 3RD generation low phase noise VCO technology. The ICS8440258-46 is packaged in a small, 5mm x 5mm VFQFN package.

Features

- Four differential LVDS outputs at 125MHz
  Two LVCMOS/LVTTL single-ended outputs at 125MHz
  Two LVCMOS/LVTTL single-ended outputs at 25MHz
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.5ps (typical)
- Full 2.5V supply mode
- 0°C to 70°C ambient operating temperature
- Lead-free (RoHS 6) packaging

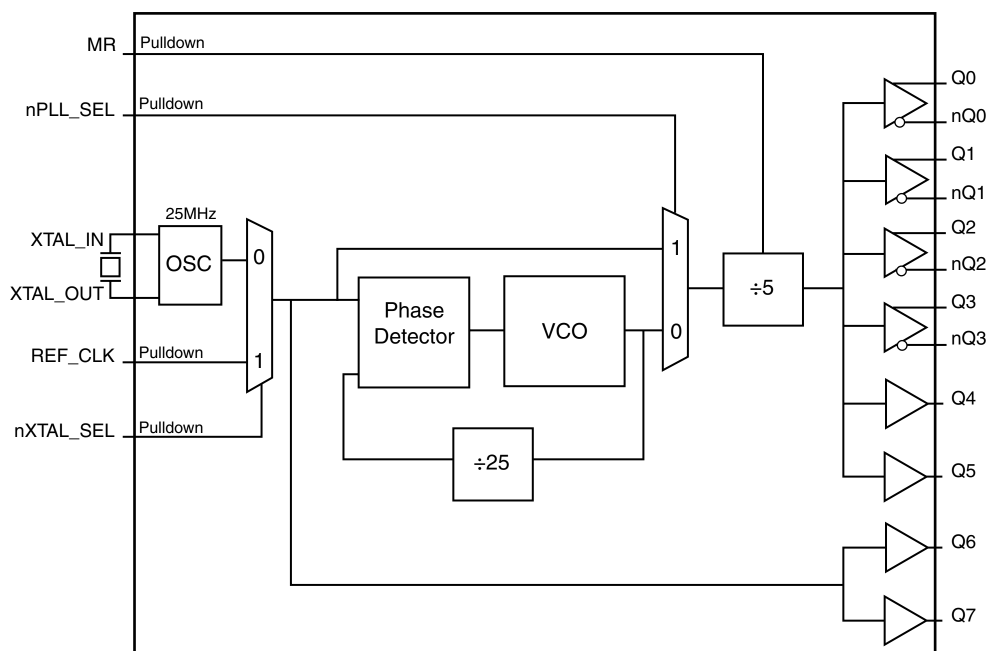
Pin Assignment



ICS8440258-46

32-Lead VFQFN
5mm x 5mm x 0.925mm package body
3.15mm x 3.15mm ePad size
K Package
Top View

Block Diagram



© 2019 Renesas Electronics Corporation

Pin Descriptions and Characteristics

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential clock outputs. LVDS interface levels.
3, 12, 16, 17, 21	GND	Power		Power supply ground.
4, 5	Q1, nQ1	Output		Differential clock outputs. LVDS interface levels.
6, 11, 27	V_{DD}	Power		Core supply pins.
7, 8	Q2, nQ2	Output		Differential clock outputs. LVDS interface levels.
9, 10	Q3, nQ3	Output		Differential clock outputs. LVDS interface levels.
13, 15, 18, 20	Q4, Q5, Q6, Q7	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
14	V_{DDO1}	Power		Output supply pin for Q4 and Q5 LVCMOS outputs.
19	V_{DDO2}	Power		Output supply pin for Q6 and Q7 LVCMOS outputs.
22, 23, 24	nc	Unused		No connect.
25	V_{DDA}	Power		Analog supply pin.
26	nPLL_SEL	Input	Pulldown	PLL Bypass. When LOW, Q[0:3], nQ[0:3], Q4, Q5 is driven from the VCO output. When HIGH, the PLL is bypassed and Q[0:3], nQ[0:3], Q4, Q5 output frequency = reference clock frequency/N output divider. LVCMOS/LVTTL interface levels.
28	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the outputs to go low. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
29	REF_CLK	Input	Pulldown	Single-ended reference clock input. LVCMOS/LVTTL interface levels.
30	nXTAL_SEL	Input	Pulldown	Selects between the crystal or REF_CLK inputs as the PLL reference source. When HIGH, selects REF_CLK. When LOW, selects XTAL inputs. LVCMOS/LVTTL interface levels.
31, 32	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_OUT is the output, XTAL_IN is the input.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	REF_CLK, nXTAL_SEL, MR, nPLL_SEL			4		pF
C_{PD}	Power Dissipation Capacitance (per output)	Q[4:5]	V_{DDO1}, V_{DDO2} = 2.625V		12		pF
		Q[6:7]	V_{DDO1}, V_{DDO2} = 2.625V		7		pF
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{OUT}	Output Impedance	Q[4:5]	V_{DDO1}, V_{DDO2} = 2.5V		11		Ω
		Q[6:7]	V_{DDO1}, V_{DDO2} = 2.5V		22		Ω

© 2019 Renesas Electronics Corporation

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O (LVCMOS)	-0.5V to V_{DDOx}+ 0.5V
Outputs, I_O (LVDS) Continuous Current Surge Current	 10mA 15mA
Operating Temperature Range, T_A	0°C to +70°C
Package Thermal Impedance, θ_{JA}	33.1°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, $V_{DD} = V_{DDO1} = V_{DDO2}$ = 2.5V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.15	2.5	V_{DD}	V
V_{DDO1}, V_{DDO2}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current	Outputs Unterminated		170	187	mA
I_{DDA}	Analog Supply Current	Outputs Unterminated		13	15	mA
I_{DDO1}+ I_{DDO2}	Output Supply Current	Outputs Unterminated			6	mA

Table 3B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDO1} = V_{DDO2}$ = 2.5V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.7	V
I_{IH}	Input High Current	nXTAL_SEL, MR, REF_CLK, nPLL_SEL	$V_{DD} = V_{IN}$ = 2.625V			150	µA
I_{IL}	Input Low Current	nXTAL_SEL, MR, REF_CLK, nPLL_SEL	V_{DD} = 2.625V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage	Q[4:7]	V_{DDO1}, V_{DDO2} = 2.5V±5%; I_{OH} = -12mA	1.8			V
V_{OL}	Output Low Voltage	Q[4:7]	V_{DDO1}, V_{DDO2} = 2.5V±5%; I_{OL} = 12mA			0.5	V

© 2019 Renesas Electronics Corporation

Table 3C. LVDS DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		300	400	485	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		0.85	1.2	1.55	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 4. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency			25		MHz
Equivalent Series Resistance				50	Ω
Shunt Capacitance				7	pF
Load Capacitance			12	18	pF

© 2019 Renesas Electronics Corporation

AC Electrical Characteristics

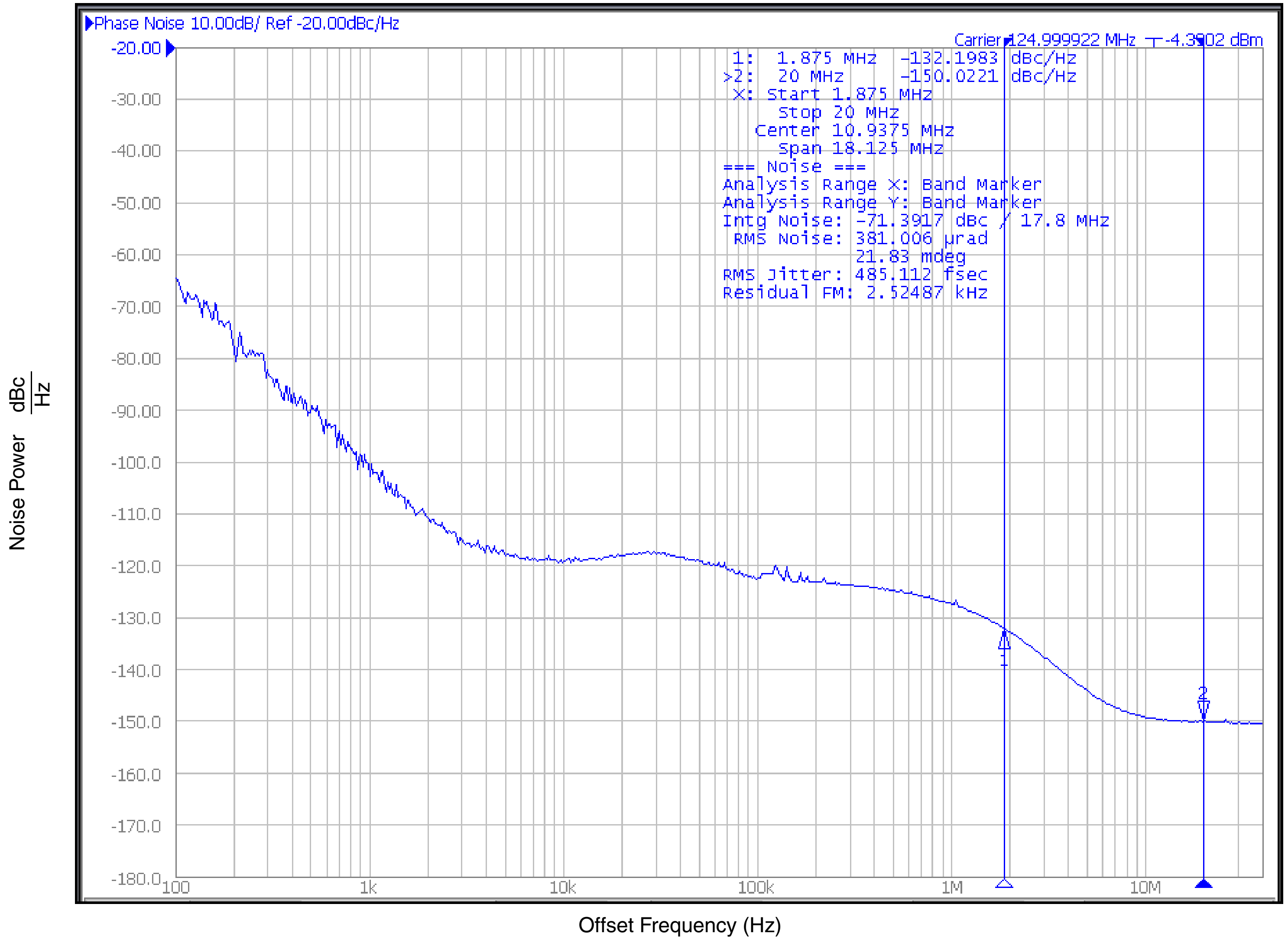
Table 5. AC Characteristics, $V_{DD} = V_{DDO1} = V_{DDO2} = 2.5V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	Q[0:3], nQ[0:3]			125		MHz
		Q4, Q5			125		MHz
		Q6, Q7			25		MHz
*t*sk(o)	Output Skew; NOTE 2	Q[0:3], nQ[0:3]; NOTE 1A	nPLL_SEL = 0			40	ps
		Q[4:5]; NOTE 1B	nPLL_SEL = 0			80	ps
		Q[6:7]; NOTE 1B				80	ps
*t*jit(Ø)	RMS Phase Noise Jitter (Random); NOTE 3	Q[0:3], nQ[0:3]	125MHz, Integration Range: 1.875MHz - 20MHz		0.5		ps
			125MHz, Integration Range: 12kHz - 20MHz		1.149		ps
		Q4, Q5	125MHz, Integration Range: 1.875MHz - 20MHz		0.5		ps
			125MHz, Integration Range: 12kHz - 20MHz		1.188		ps
t_R / t_F	Output Rise/Fall Time	Q[0:3], nQ[0:3]	20% to 80%	330		600	ps
		Q[4:5]	20% to 80%	250		450	ps
		Q[6:7]	20% to 80%	0.78		2.7	ns
odc	Output Duty Cycle	Q[0:3], nQ[0:3]		45		55	%
		Q[4:5]		45		55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Device characterized with a 25MHz, 12pF quartz crystal.
NOTE 1A: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross point.
NOTE 1B: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDOX}/2$.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Refer to Phase Noise Plots.

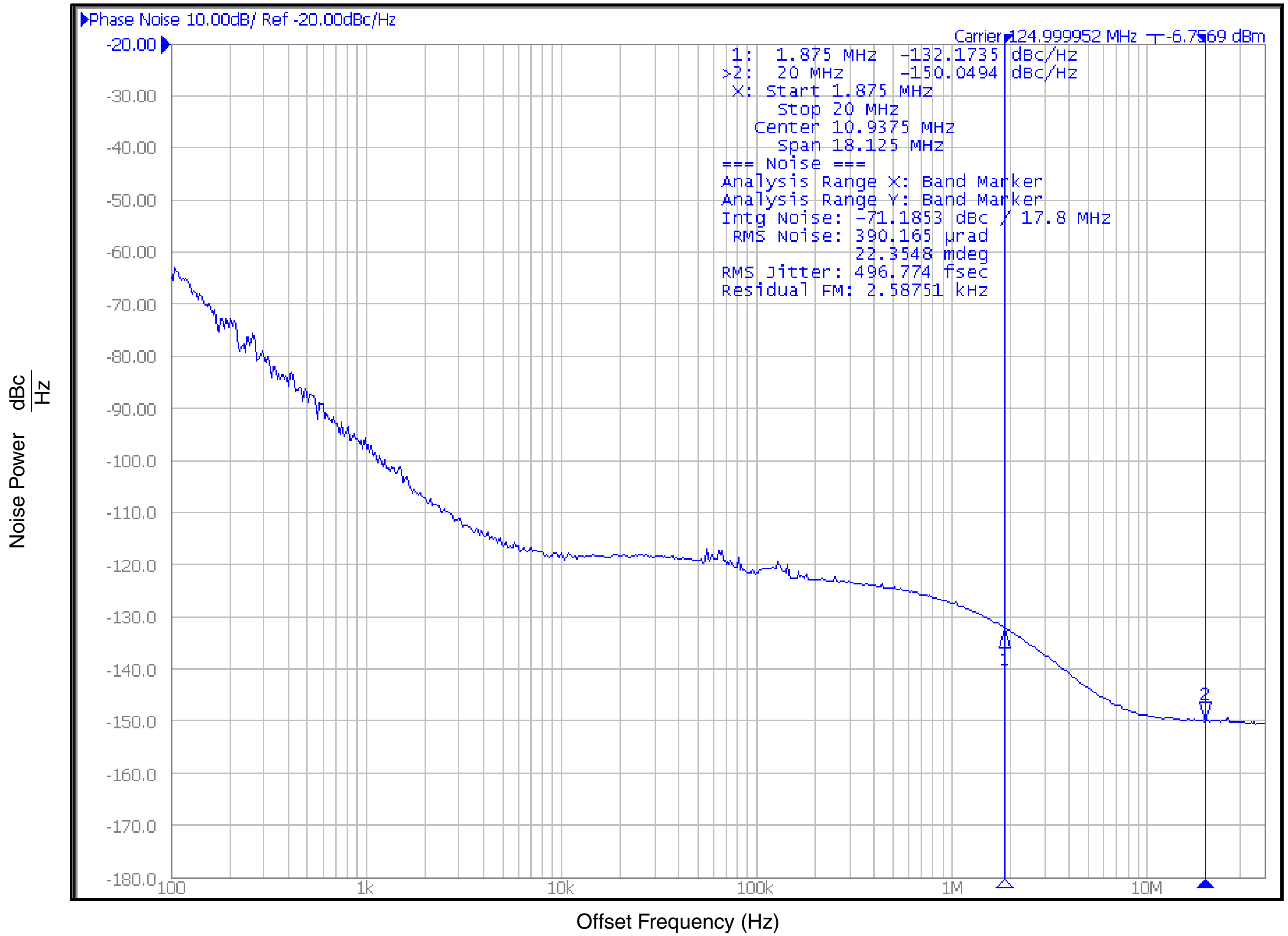
© 2019 Renesas Electronics Corporation

Typical Phase Noise at 125MHz @ 2.5V (LVCMOS output), 1.875MHz – 20MHz



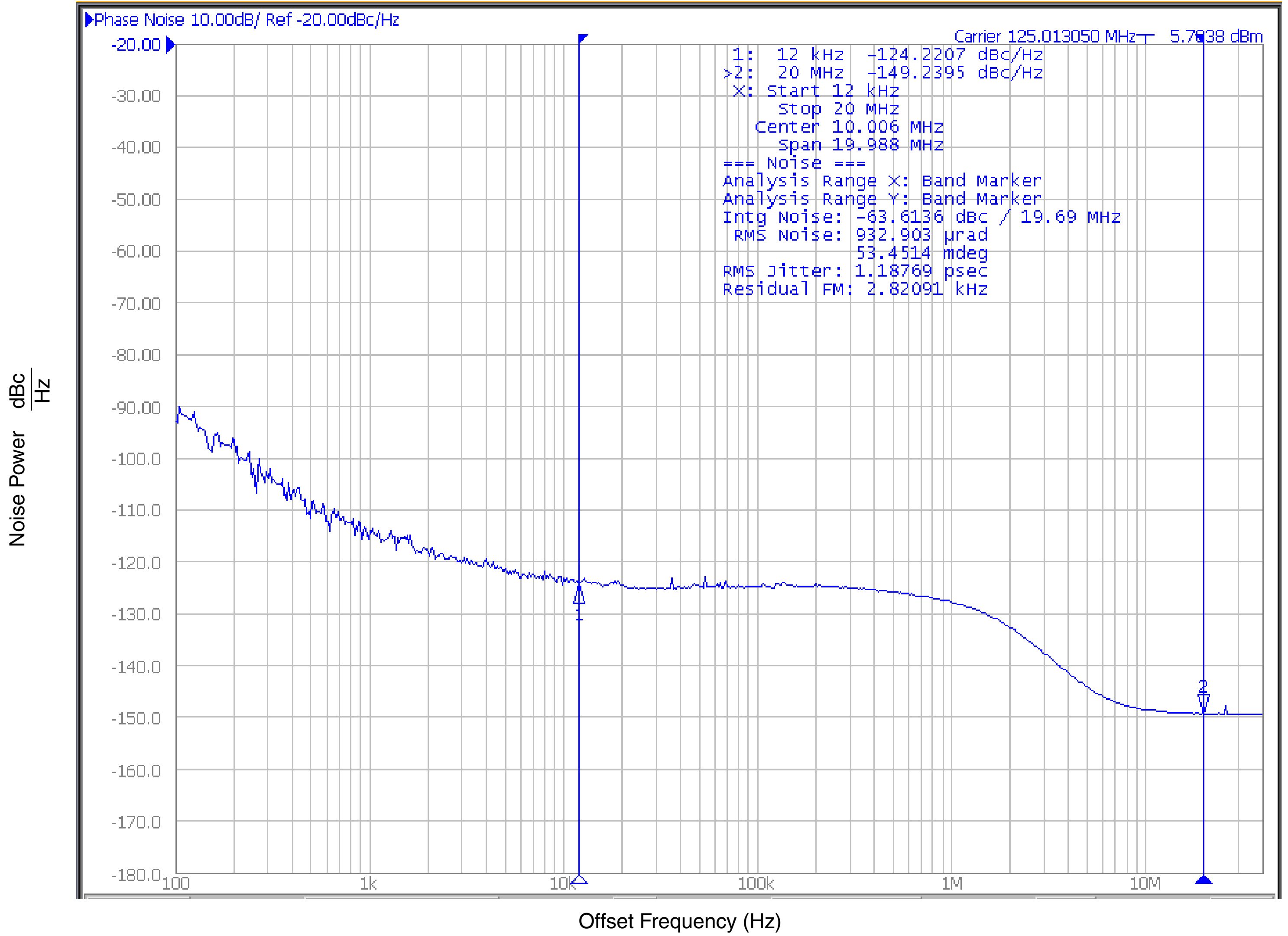
© 2019 Renesas Electronics Corporation

Typical Phase Noise at 125MHz @ 2.5V (LVDS output), 1.875MHz – 20MHz



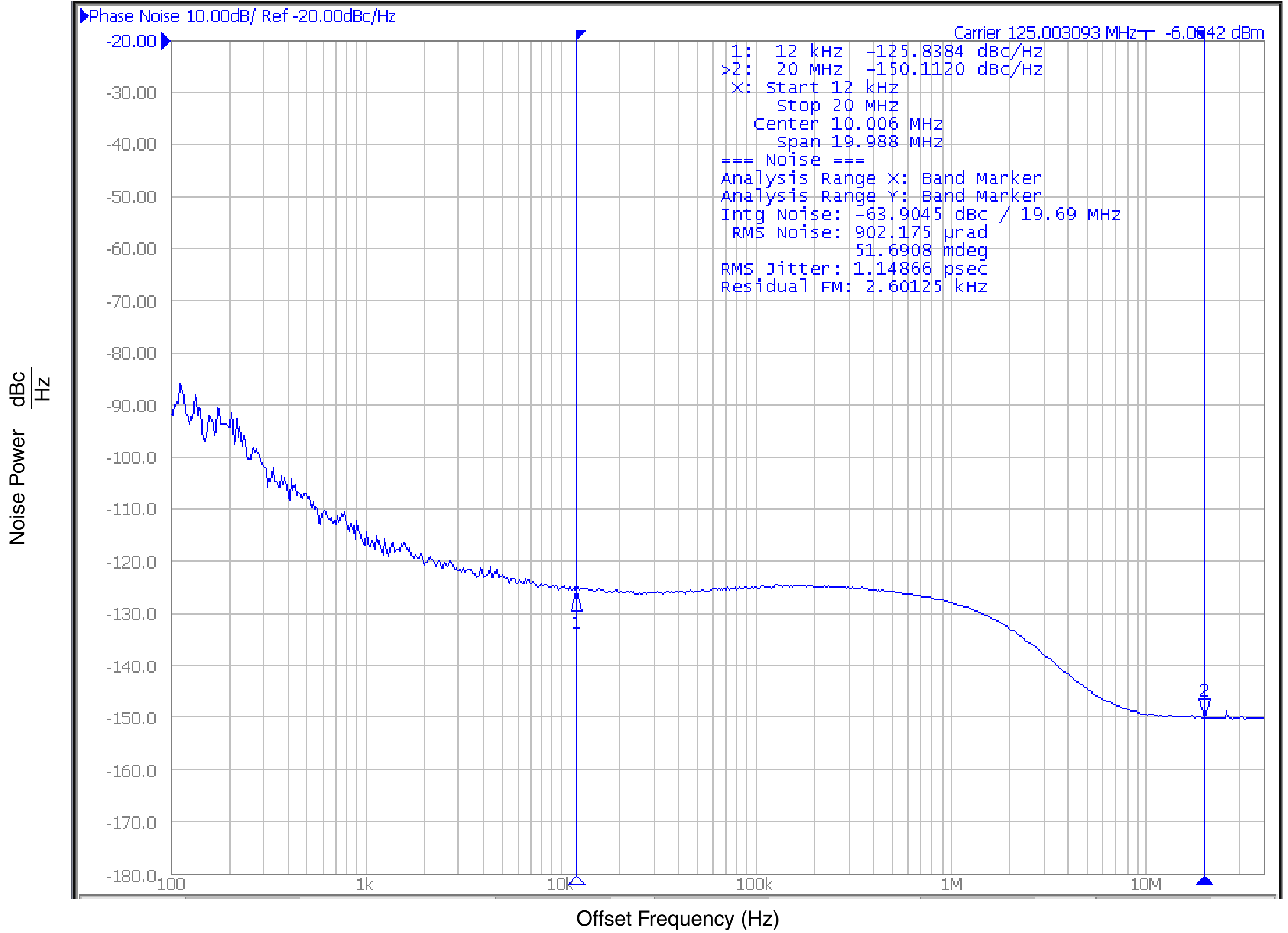
© 2019 Renesas Electronics Corporation

Typical Phase Noise at 125MHz @ 2.5V (LVCMOS output), 12kHz – 20MHz



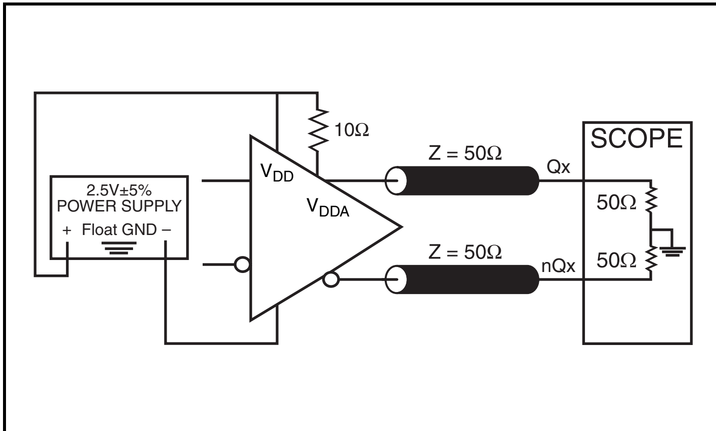
© 2019 Renesas Electronics Corporation

Typical Phase Noise at 125MHz @ 2.5V (LVDS output), 12kHz – 20MHz

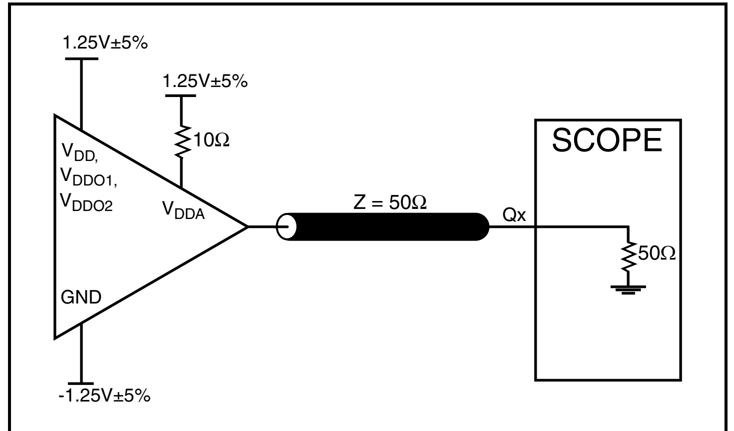


© 2019 Renesas Electronics Corporation

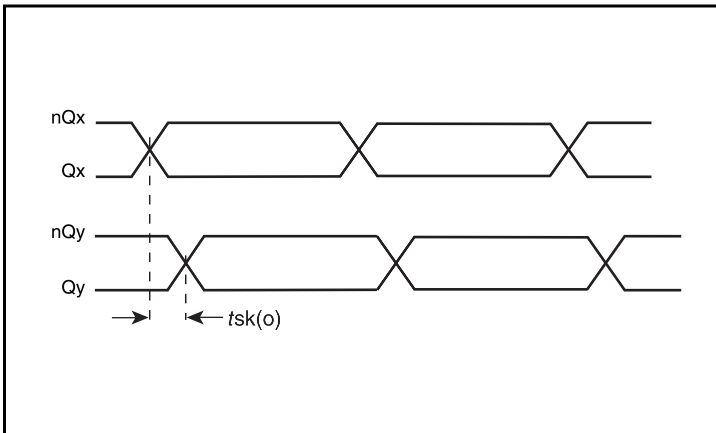
Parameter Measurement Information



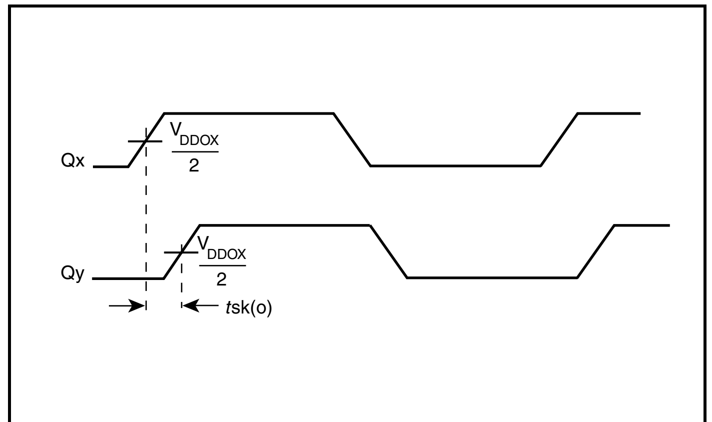
2.5V LVDS Output Load Test Circuit



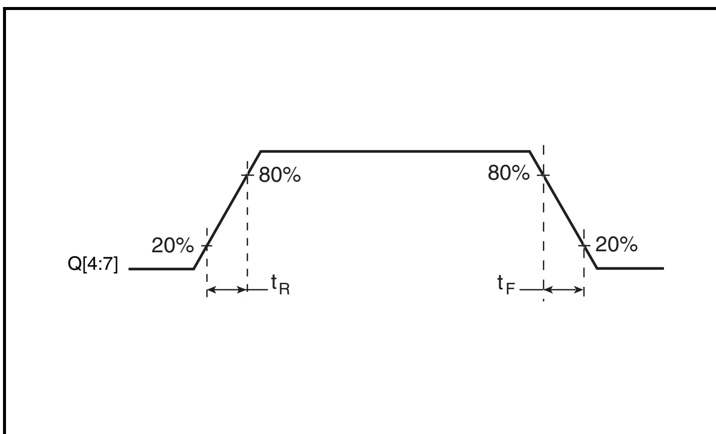
2.5V LVCMOS Output Load Test Circuit



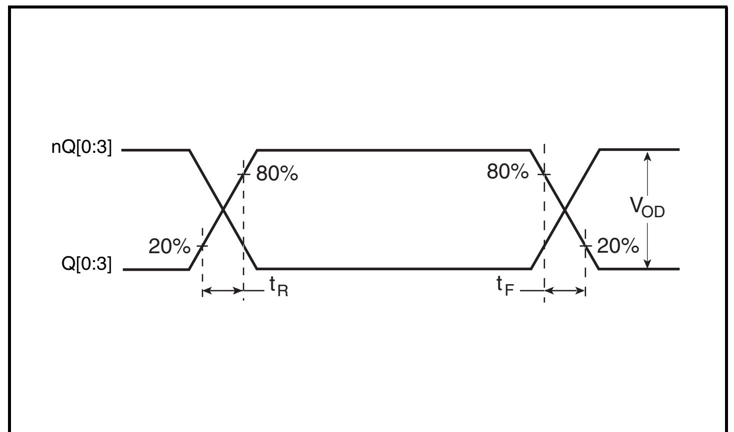
LVDS Output Skew



LVCMOS Output Skew



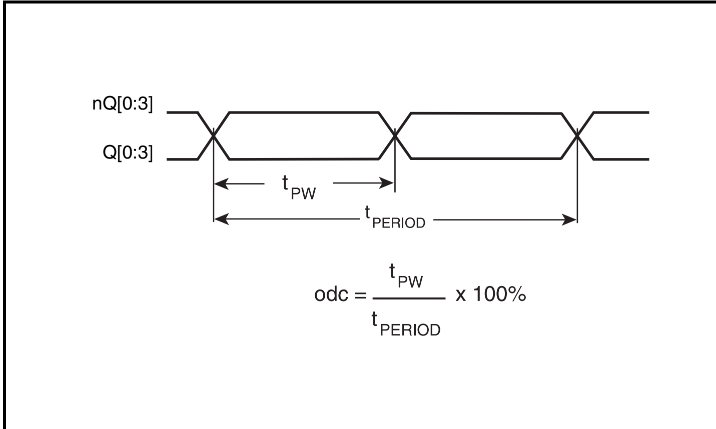
LVCMOS Output Rise/Fall Time



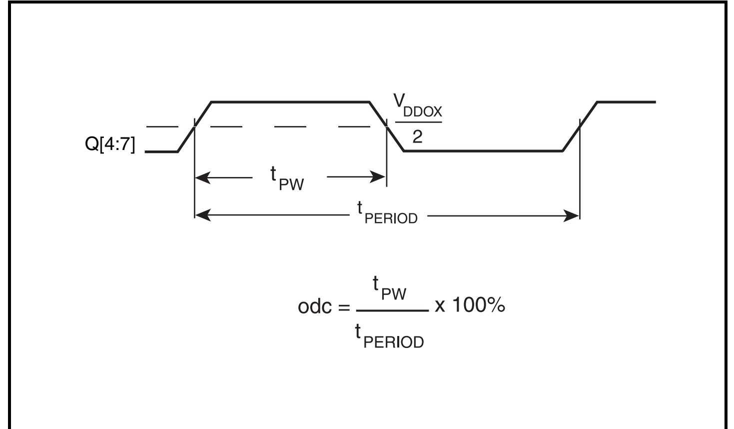
LVDS Output Rise/Fall Time

© 2019 Renesas Electronics Corporation

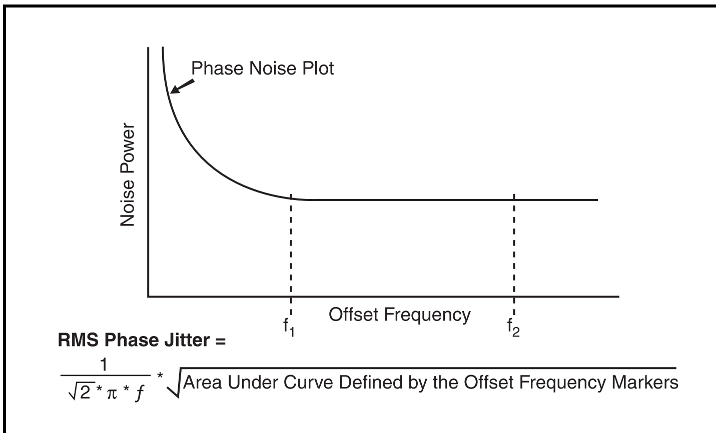
Parameter Measurement Information, continued



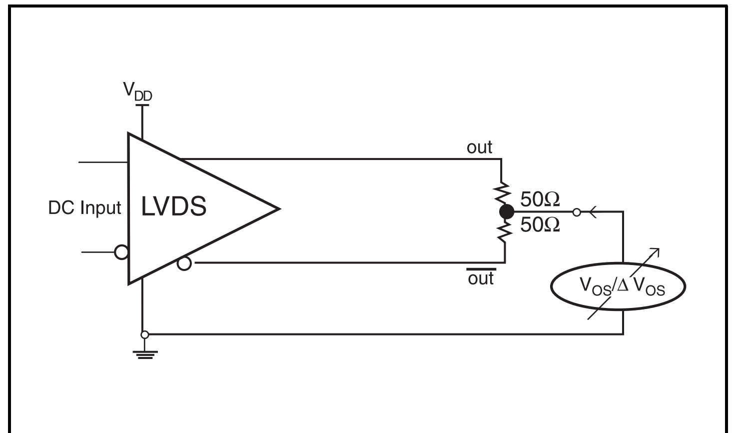
LVDS Output Duty Cycle/Pulse Width/Period



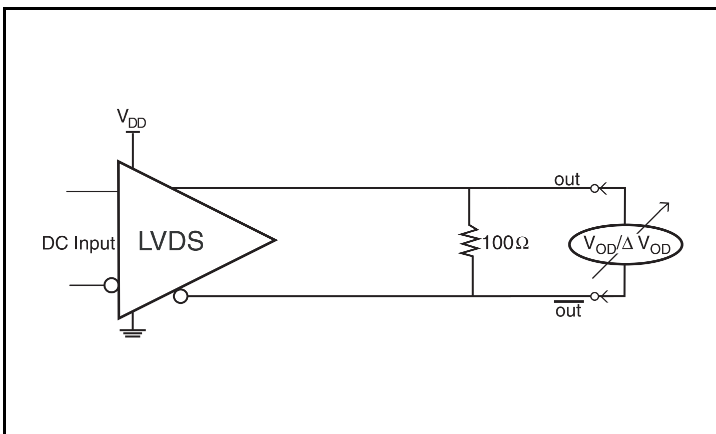
LVCMOS Output Duty Cycle/Pulse Width/Period



RMS Phase Jitter



Offset Voltage Setup



Differential Output Duty Cycle/Pulse Width/Period

© 2019 Renesas Electronics Corporation

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_CLK Input

For applications not requiring the use of a reference clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK input to ground.

LVCMOS Control Pins

All control pins have internal pulldown resistors; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

LVCMOS Outputs

All unused LVCMOS outputs can be left floating. There should be no trace attached.

© 2019 Renesas Electronics Corporation

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 1A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 1B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

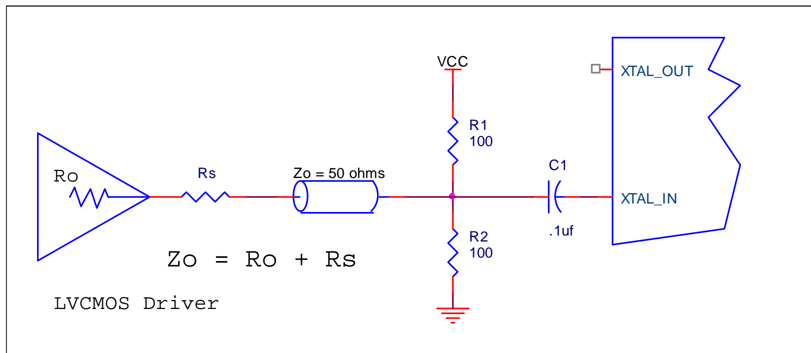


Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface

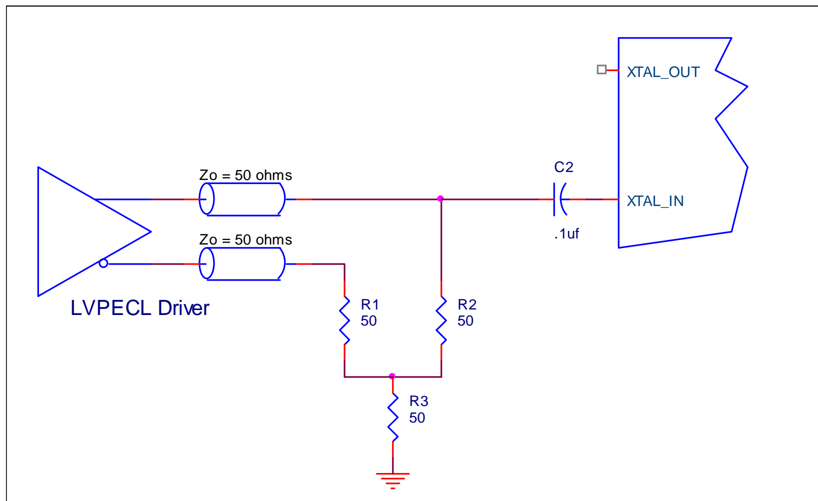
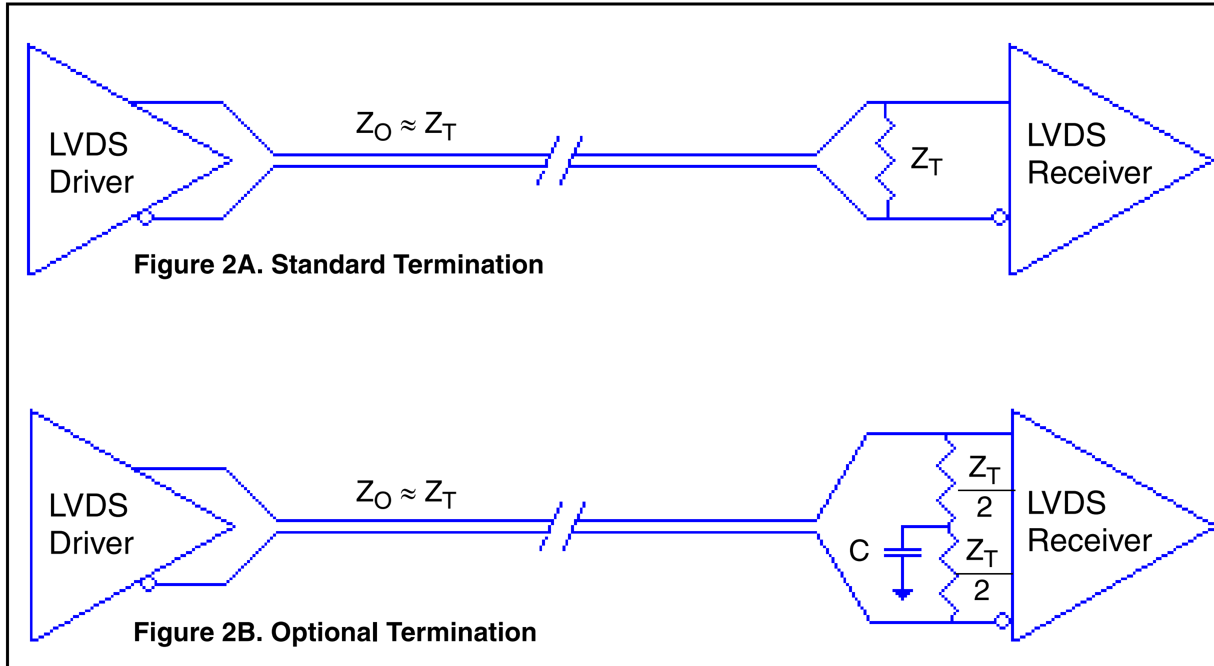


Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface

© 2019 Renesas Electronics Corporation

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 2A* can be used with either type of output structure. *Figure 2B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.



LVDS Termination

© 2019 Renesas Electronics Corporation

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor's Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

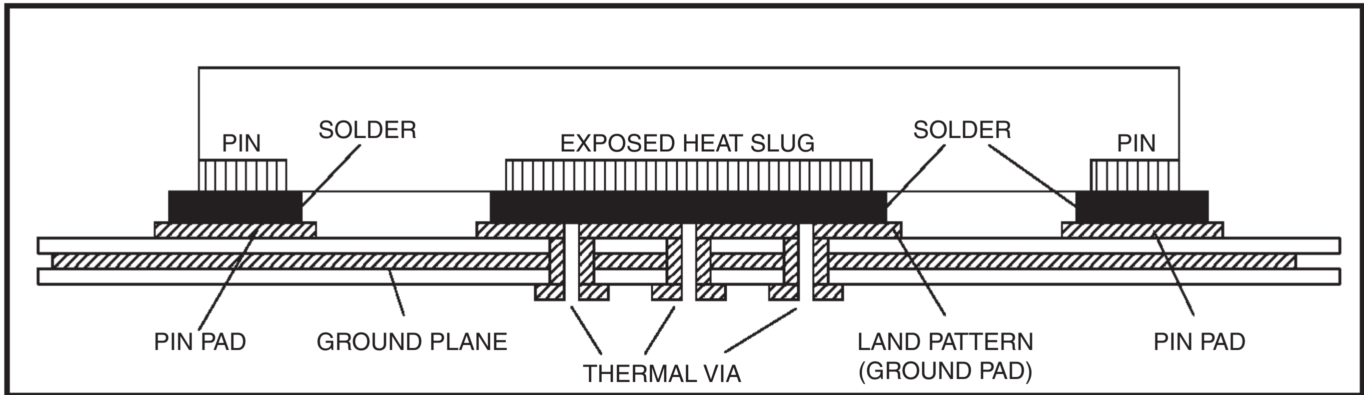


Figure 3. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

© 2019 Renesas Electronics Corporation

Schematic Layout

Figure 4 shows an example ICS8440258-46 application schematic. The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set. Input and output terminations shown are intended as examples only and may not represent the exact user configuration.

In this example an 18pF parallel resonant 25MHz crystal is used with load caps C7 = C6 = 22pF. The load caps are recommended for frequency accuracy, but these may be adjusted for different board layouts. Crystals with different load capacities may be used, but the load capacitors will have to be changed accordingly. If different crystal types are used, please consult IDT for recommendations.

The schematic example shows two different LVDS output terminations; the standard termination 100Ω shunt termination for an LVDS compliant receiver and an AC coupled termination for a non-LVDS differential receiver. The AC coupled termination requires that the designer select the values of R3 and R4 in order to center the LVDS swing within the common mode range of the receiver. In addition the designer must make sure that the target receiver will operate reliably with the LVDS swing, which is reduced relative to other logic families such as HCSL or LVPECL.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS8440258-46 provides separate $V_{DD,}$ V_{DDA} and V_{DDO} pins to isolate any high speed switching noise at the outputs from coupling into the internal PLL.

In order to achieve the best possible filtering, it is highly recommended that the 0.1uF capacitors be placed on the ICS8440258-46 side of the PCB as close to the power pins as possible. This is represented by the placement of these capacitors in the schematic. If space is limited, the ferrite beads, 10uF capacitors and the 0.1uF capacitors connected directly to 2.5V can be placed on the opposite side of the PCB. If space permits, place all filter components on the device side of the board.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

© 2019 Renesas Electronics Corporation

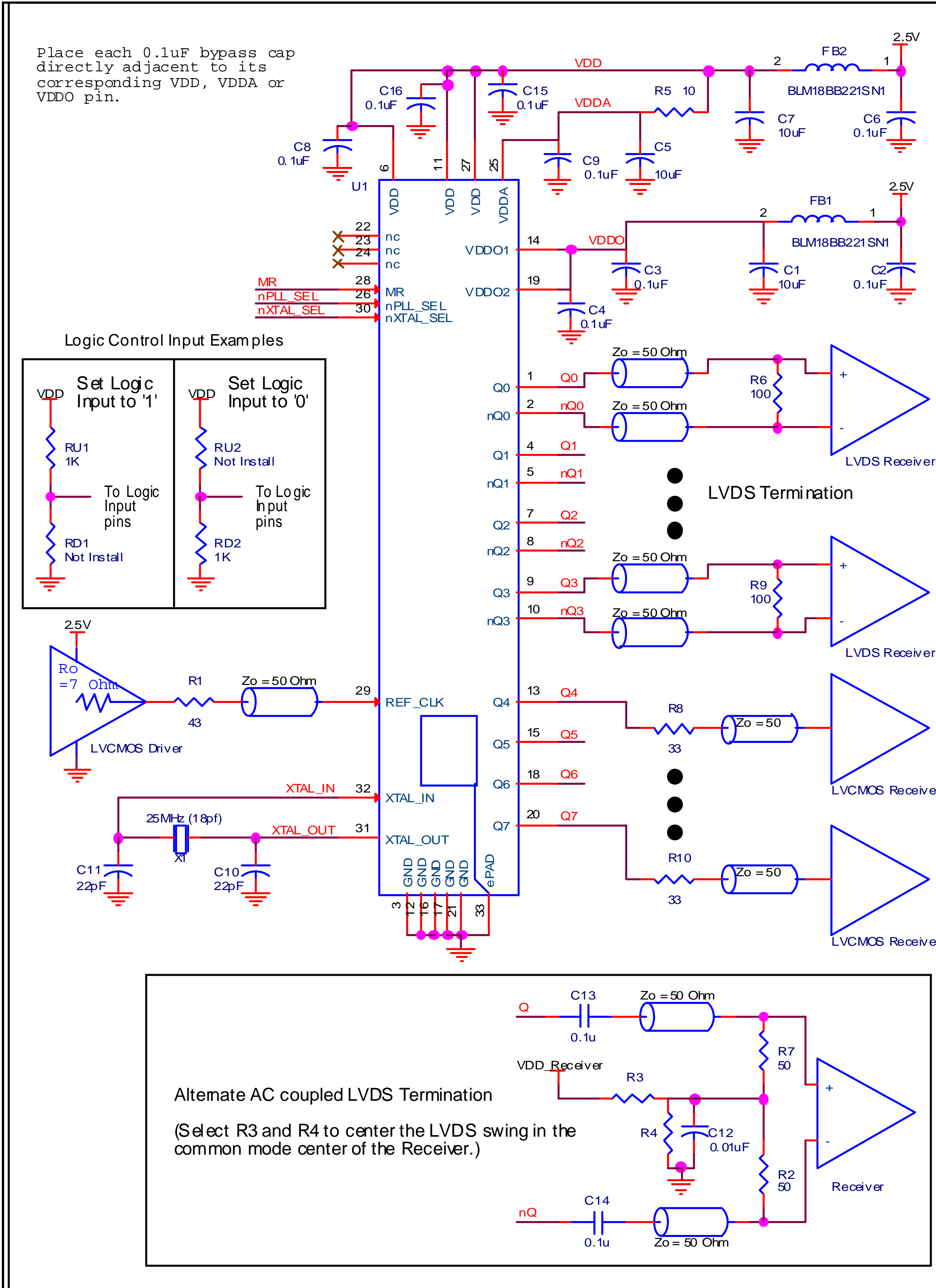


Figure 4. ICS8440258-46 Schematic Example

© 2019 Renesas Electronics Corporation

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8440258-46.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8440258-46 is the sum of the core power plus the analog plus the power dissipated into the load.
The following is the power dissipation for V_{DD} = 2.5V + 5% = 2.625V, which gives worst case results.

Core and LVDS Output Power Dissipation

The maximum currents at 70° are as follows:

I_{DD_MAX} = 187mA

I_{DDA_MAX} = 15mA

I_{DDOX_MAX} = 6mA

- Power (core, LVDS) = V_{DDX_MAX} * (I_{DD_MAX} + I_{DDA_MAX} + I_{DDOX_MAX}) = 2.625V * (187mA + 15mA + 6mA) = **546mW**

LVCMOS Output Power Dissipation

- Output Impedance R_{OUT} Power Dissipation into the Load 50Ω to $V_{DDOX_MAX}/2$
  Output Current I_{OUT} = V_{DDOX_MAX} / [2 * (50Ω + R_{OUT})] = 2.625V / [2 * (50Ω + 11Ω)] = **21.52mA**
  Output Current I_{OUT} = V_{DDOX_MAX} / [2 * (50Ω + R_{OUT})] = 2.625V / [2 * (50Ω + 22Ω)] = **18.23mA**
- Power Dissipation on the R_{OUT} per LVCMOS output
  Power (R_{OUT}) = R_{OUT} * $(I_{OUT})^2$ = 11Ω * $(21.52mA)^2$ = **5.09mW per output**
  Power (R_{OUT}) = R_{OUT} * $(I_{OUT})^2$ = 22Ω * $(18.23mA)^2$ = **7.31mW per output**
- Total Power Dissipation on the R_{OUT}
  Total Power (R_{OUT}) = 5.09mW * 2 = **10.18mW**
  Total Power (R_{OUT}) = 7.31mW * 2 = **14.62mW**
- Dynamic Power Dissipation at 125MHz
  Power (125MHz) = C_{PD} * Frequency * $(V_{DDOX_MAX})^2$ = 12pF * 125MHz * $(2.625V)^2$ = **10.34mW per output**
  Total Power (125MHz) = 10.34mW * 2 = **20.68mW**
- Dynamic Power Dissipation at 25MHz
  Power (25MHz) = C_{PD} * Frequency * $(V_{DDOX_MAX})^2$ = 7pF * 25MHz * $(2.625V)^2$ = **1.21mW per output**
  Total Power (25MHz) = 1.21mW * 2 = **2.42mW**

Total Power Dissipation

- **Total Power**
  = Power (core, LVDS) + Total Power (R_{OUT}) + Total Power (125MHz) + Total Power (25MHz)
  = 546mW + 10.18mW + 14.62mW + 20.68mW + 2.42mW
  = 594mW

© 2019 Renesas Electronics Corporation

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 33.1°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.594W * 33.1°C/W = 89.7°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} **Vs. Air Flow**			
Meters per Second	**0**	**1**	**3**
Multi-Layer PCB, JEDEC Standard Test Boards	33.1°C/W	28.1°C/W	25.4°C/W

© 2019 Renesas Electronics Corporation

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**3**
Multi-Layer PCB, JEDEC Standard Test Boards	33.1°C/W	28.1°C/W	25.4°C/W

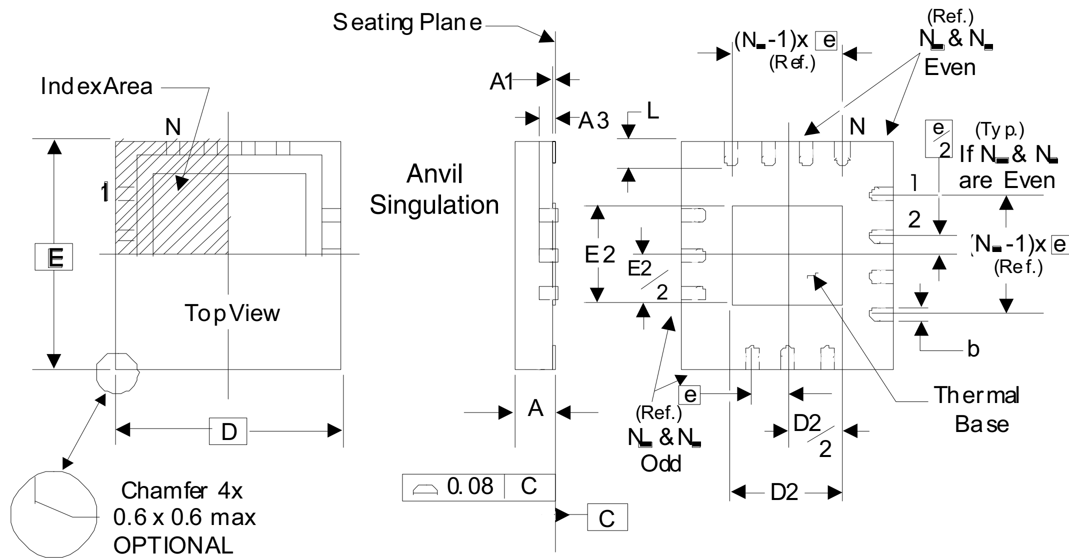
Transistor Count

The transistor count for ICS8440258-46 is: 2610

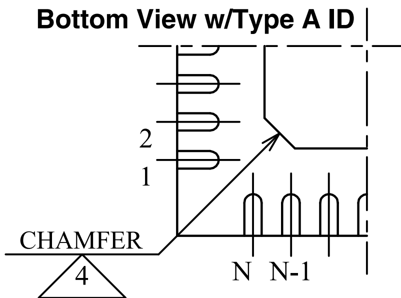
© 2019 Renesas Electronics Corporation

Package Outline and Package Dimensions

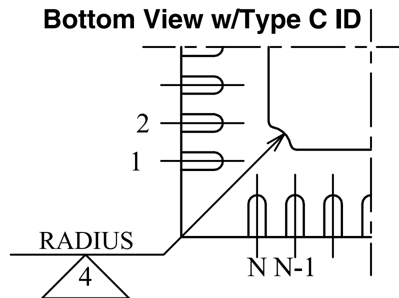
Package Outline - K Suffix for 32 Lead VFQFN



Bottom View w/Type A ID



Bottom View w/Type C ID



There are 2 methods of indicating pin 1 corner at the back of the VFQFN package:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

Table 8. Package Dimensions

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A	0.80		1.00
A1	0		0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D & N_E			8
D & E		5.00 Basic	
D2 & E2	3.0		3.3
e		0.50 Basic	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 8.

© 2019 Renesas Electronics Corporation

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8440258CK-46LF	ICS0258C46L	“Lead-Free” 32 Lead VFQFN	Tray	0°C to 70°C
8440258CK-46LFT	ICS0258C46L	“Lead-Free” 32 Lead VFQFN	Tape & Reel	0°C to 70°C

© 2019 Renesas Electronics Corporation

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use o any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2023 Renesas Electronics Corporation. All rights reserved.