Low Voltage, Low Skew, 1.244GHz PLL Clock Synthesizer

843S06

DATA SHEET

General Description

The 843S06 is a low voltage, low skew 3.3V LVPECL Clock Synthesizer. The device targets clock distribution in SDH/SONET telecommunication systems but is well suited for a wide range of applications requiring high performance high-speed clock synthesis.

The device implements a fully integrated multiplying PLL including:

- An on-chip analog voltage controlled oscillator (VCO)
- Phase-frequency detector
- Programmable frequency dividers (prescalers)

The loop filter is external in order to optimize the PLL for different applications.

As an option, the 843S06 may be operated with an external voltage controlled crystal oscillator for applications demanding a high-Q oscillator.

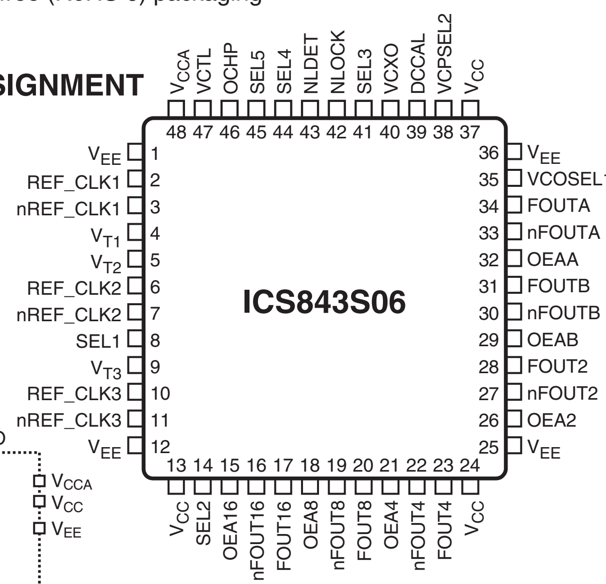
Features

- Six differential 3.3V LVPECL outputs

  1,244.16/622.08MHz; 1,244.16/622.08MHz
  622.08/311.04MHz; 311.04/155.52MHz
  155.52/77.76MHz; 77.76/38.88MHz

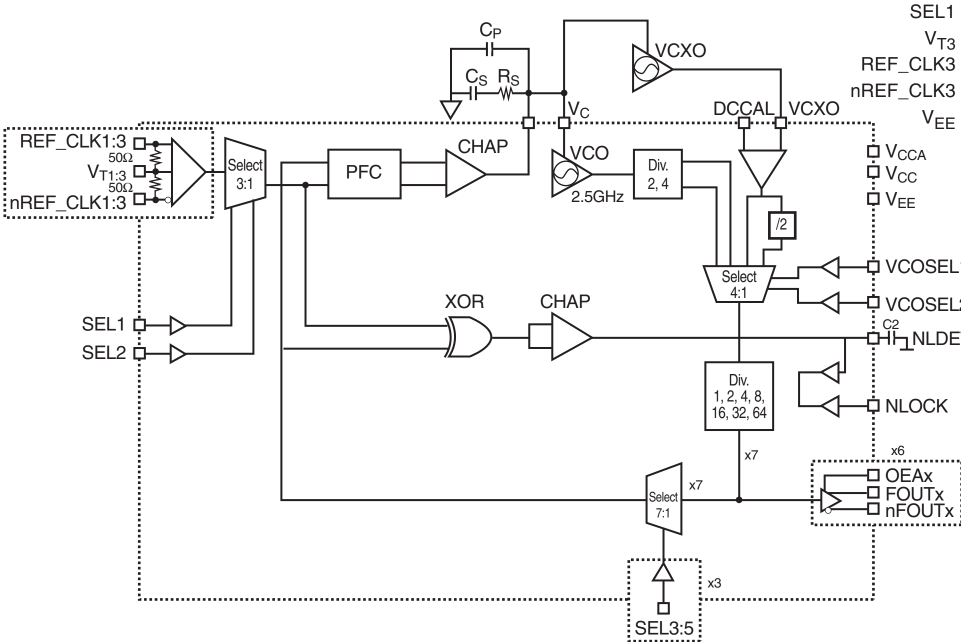
- Three selectable differential reference clock inputs
  Clock frequency range: 19MHz to 622MHz
- REF_CLKx, nREF_CLKx pairs can accept the following differential input level: LVPECL
- Intrinsic jitter: 0.017mUI$_{RMS}$ @ 622MHz
- Output skew: 200ps (maximum)
- Optional external VCXO possible
- Simple external loop filter
- Lock detect output signal
- Full 3.3V operating supply
- Low power operation 0.6W (typical)
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

Pin Assignment



48-Lead TQFP, E-Pad
7mm x 7mm x 1.0mm
package body
Y Package
Top View

Block Diagram



Features

The 843S06 comprises:

- a low-noise analog VCO
- a Phase-Frequency Detector
- frequency dividers (prescalers)
- a charge pump

into an integrated PLL frequency synthesizer. Careful design and layout matching ensures short delay and minimum skew between input reference clocks and outputs.

Jitter Performance

The frequency of the input reference clock may range between 19.44MHz and 622.08MHz. Since changing the reference frequency alters the loop-gain within the PLL it may be necessary to adjust the loop-filter components when switching to a different reference frequency in order to achieve ITU-T recommended performance.

PLL Propagation Delay

When the PLL is in lock, the Phase Frequency Detector aligns the positive (low to high transition) flanks of the reference clock and divided VCO clock on it's inputs. These inputs are marked R and V on *Figure 1.* This means the positive transition of any FOUTx output clock is aligned with the positive transition of the reference clock under the condition of equal reference clock frequency and FOUTx output frequency, please refer to *Figure 3.* Figure 3 defines the PLL propagation delay parameter (D_{OUT}). Note that D_{OUT} will change with leakage currents drawn from the loop-filter, hence D_{OUT} is loop-filter dependant.

Figure 3 is an example for D_{OUT} phase relationships. The REF_CLK[1:3] input signals shown are in reference to FOUT2 output signals, both running at Fx MHz with the PLL locked using the recommended loop-filter and no excessive leakage current drawn from the charge pump output. A skew of 200ps maximum is expected, (see Figure 4). Skew over supply and temperature definitions are at any combination of extremes. The expected skew values are only valid with the PLL locked when using the recommended loop-filter. The Total Output Uncertainty is $D_{OUT} + t_{skew}$, (see Figures 3 and 4).

Output Clocks

The 843S06 is equipped with six LVPECL compatible output buffers. Each of the output buffers is equipped with an LVTTL enable pin that may be used to disable clock signals not in use for noise reduction. Clock outputs are synchronized by the falling edge. The phases of the clock output signals are aligned with less than 200ps skew peak-to-peak between any two clock signals. Available clock signals from the PLL are divide by 1 (signal FOUTA and by FOUTB), divide by 2 (FOUT2), divide by 4 (FOUT4), divide by 8 (FOUT8) and divide by 16 (FOUT16).

Lock Detect

The device outputs a signal NLDET that may be used to signal whether or not the PLL is locked thus allowing fault diagnostics. The NLDET outputs the result of an XOR operation of the signals input to the phase-frequency detector. To be useful, this signal must be filtered by a capacitor. The recommended value of this capacitor is 10nF. The filtered lock-detect signal is output as an LVTTL compatible signal on the output NLOCK via a comparator.

PLL Loop-Filter

It has been chosen to locate the passive loop-filter components externally to the device. This allows for easy optimization of the loop-filter to different applications. The recommended loop-filter is a simple first-order RC-Circuit as shown on *Figure 1*, resulting in a second order, type 2 loop.

The values of R_S, C_S and C_P depend on the application. With respect to ITU-T recommended jitter performance, appropriate values for R_S, C_S and C_P have been determined to be $R_S = 3.92k\Omega$, $C_S = 0.22\mu F$, and $C_P = 1pF$ for input frequency of 155.52MHz; and $R_S = 9.09k\Omega$, $C_S = 0.01\mu F$, and $C_P = 0$ for input frequency of 19.44MHz.

Note that the loop-filter should be terminated to the negative VCO supply. An external VCXO might require a different termination point for lowest point.

Charge Pump Polarity

When the PLL increases the VCO frequency, the charge pump pin OCHP sinks current. That is, the voltage on the loop-filter capacitor drops to increase the oscillator frequency. So be aware, that an external VCO must have a negative VCO constant in order to achieve a stable lock.

On-Chip VCO Power Down

When operated with an external VCXO the on-chip VCO should be powered down for noise reduction. This is done by leaving V_{CCA} open. See V_{CCA} pin description.

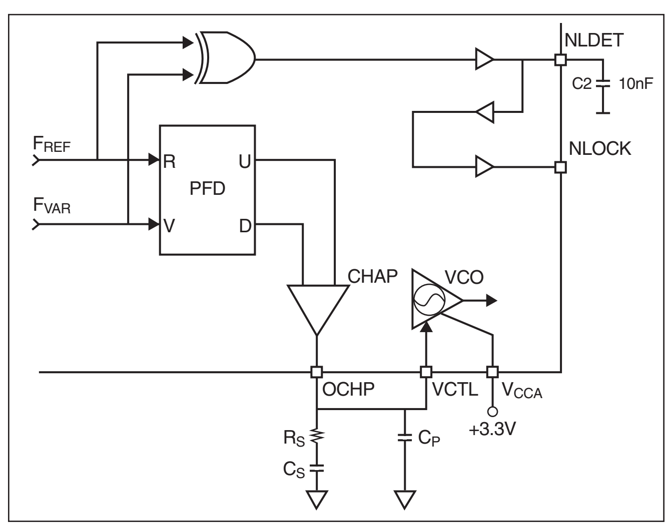


Figure 1. Application Diagram

TABLE 1. INPUT REFERENCE FREQUENCIES AS FUNCTION OF SEL[3:5] SETTINGS

VCO Source and Corresponding VCOSEL[1:2] Settings		FOUTA	Input Reference Frequency (CKREFx [MHz]) and Corresponding SEL[3:5] Settings							
		MHz	0, 0, 0	0, 0, 1	0, 1, 0	0, 1, 1	1, 0, 0	1, 0, 1	1, 1, 0	1, 1, 1
Internal VCO Ext. VCO: 1244MHz Ext. VCO: 622MHz	0, 1 0, 0 1, 1	622	622	311	155	78	39	19	N/A 9.7	Disable Feedback
Internal VCO Ext. VCO: 2488MHz Ext. VCO: 1244MHz	1, 0 0, 0 1, 1	1244	N/A 1244	622	311	155	78	39	19	

PRESCALER SETTINGS

For the PLL to achieve lock a proper relation must exist between the input reference frequency and the setting of the on-chip prescalers. The prescalers are set by signals: VCOSEL1, VCOSEL2, SEL3, SEL4, and SEL5 (refer to Table 1).

First, determine the desired master output frequency. This is the frequency of output clock FOUTA (FOUTA is mirrored by FOUTB). Next, select whether the oscillator is external or internal. The VCO source can be external (622, 1244 or 2488MHz) or internal (2488MHz). Table 1 gives the value of VCOSEL1/2. Finally, the proper relation between the reference clock frequency and the setting of SEL3, SEL4, SEL5 is read from Table 1.

DUTY CYCLE CALIBRATION

When operated with an external oscillator, the differential LVPECL inputs (VCXO and DCCAL) are to be used. In single-ended operation the duty cycle of the outputs FOUTA and FOUTB may be adjusted by tuning the voltage on DCCAL.

Table 2. Pin Descriptions

Number	Name	Type		Description
1, 12, 25, 36	V_{EE}	Power		Negative supply pins.
2	REF_CLK1	LVPECL IN		Non-inverting differential reference clock input. R_T = 50Ω termination to V_{T1}. See Figure 2, Termination of REF_CLKx. See Table 6.
3	nREF_CLK1	LVPECL IN		Inverting differential reference clock input. R_T = 50Ω termination to V_{T1}. See Figure 2, Termination of REF_CLKx. See Table 6.
4	V_{T1}	Bias		Termination input. Common termination point of 2 x 50Ω resistors, internally biased to 2V. $Z_{IN,VT1}$ = 1kΩ.
5	V_{T2}	Bias		Termination input. Common termination point of 2 x 50Ω resistors, internally biased to 2V. $Z_{IN,VT2}$ = 1kΩ.
6	REF_CLK2	LVPECL IN		Non-inverting differential reference clock input. R_T = 50Ω termination to V_{T2}. See Figure 2, Termination of REF_CLKx. See Table 6.
7	nREF_CLK2	LVPECL IN		Inverting differential reference clock input. R_T = 50Ω termination to V_{T2}. See Figure 2, Termination of REF_CLKx. See Table 6.
8, 14	SEL1, SEL2	LVT IN	Pullup Note1	Reference clock select inputs. See Table 3A. LVTTL interface levels.
9	V_{T3}	Bias		Termination input. Common termination point of 2 x 50Ω resistors, internally biased to 2V. $Z_{IN,VT3}$ = 1kΩ.
10	REF_CLK3	LVPECL IN		Non-inverting differential reference clock input. R_T = 50Ω termination to V_{T3}. See Figure 2, Termination of REF_CLKx. See Table 6.
11	nREF_CLK3	LVPECL IN		Inverting differential reference clock input. R_T = 50Ω termination to V_{T3}. See Figure 2, Termination of REF_CLKx. See Table 6.
13, 24, 37	V_{CC}	Power		Core supply pins.
15, 18, 21 26, 29, 32	OEA16, OEA8, OEA4, OEA2, OEAB, OEAA	LVT IN	Pullup Note1	Output enable pins. When HIGH (default), the FOUTx output is enabled. When LOW, the FOUTx output is disabled. 16kΩ resistor. LVTTL interface levels.
16, 17	nFOUT16, FOUT16	LVPECL OUT		Differential clock output pair (÷16). LVPECL interface levels.
19, 20	nFOUT8, FOUT8	LVPECL OUT		Differential clock output pair (÷8). LVPECL interface levels.
22, 23	nFOUT4, FOUT4	LVPECL OUT		Differential clock output pair (÷4). LVPECL interface levels.
27, 28	nFOUT2, FOUT2	LVPECL OUT		Differential clock output pair (÷2). LVPECL interface levels.
30, 31	nFOUTB, FOUTB	LVPECL OUT		Differential clock output pair (÷1). LVPECL interface levels.
33, 34	nFOUTA, FOUTA	LVPECL OUT		Differential clock output pair (÷1). LVPECL interface levels.
35, 38	VCOSEL1, VCOSEL2	LVT IN	Pullup Note1	Select pins for internal or external oscillator and prescale. See Table 4B. 16kΩ resistor. LVTTL interface levels.

NOTE 1: Pullup refers to internal pullup resistors. See Table 2, Pin Characteristics Table, for typical values.

Continued on next page.

TABLE 2. PIN DESCRIPTIONS, CONTINUED

Number	Name	Type		Description
39, 40	DCCAL, VCXO	LVT IN		Differential external clock input, F_{MAX} = 2.7GHz/1.35GHz. The input can be used differentially or the DCCAL input may be used as a VCXO duty cycle control. When selecting external VCXO (divide by 1) the duty cycle of the FOUTA/B, nFOUTA/B outputs can be controlled by DCCAL. Adjust range: 40/60 to 60/40 assuming sinusoidal input at VCXO. DC-CAL is connected to the inverted input. NOTE: Pins DCCAL (pin 39) and VCXO (pin 40) can handle ESD, HBM of maximum value: 500V.
41, 44, 45	SEL3, SEL4, SEL5	LVT IN	Pullup Note1	Prescaler select inputs. See Table 4C. LVTTL interface levels.
42	NLOCK	LVT OUT		Lock detect buffered. When 10nF is connected to NLDET, then NLOCK = 0 signals PLL in-lock; NLOCK = 1 signals PLL out-of-lock. See Note 2.
43	NLDET	Analog OUT		Lock detect unfiltered. Connect pin to a 10nF capacitor to ground.
46	OCHP	Analog OUT		Charge pump output to be connected to the loop filter. The pin will sink current to increase the oscillator frequency and source current to decrease the oscillator frequency. Refer to Figure 1.
47	VCTL	Analog IN		Voltage control pin for internal VCO. To be connected to the loop filter.
48	V_{CCA}	Power		Internal VCO analog supply pin. Leave open when using external VCO.
	Heat sink	Power		Heatsink is electrically isolated from the internal device and is attached facing down.

NOTE 1: *Pullup* refers to internal pullup resistors. See Table 2, Pin Characteristics Table, for typical values.
NOTE 2: Refer to the Application Note on page 15.

TABLE 3. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			16		kΩ

Table 4A. Control Input Function Table

Input Select		
SEL1	SEL2	Input Clock
0	0	REF_CLK1
0	1	REF_CLK2
1	0	REF_CLK3
1	1	No input reference to PLL (default)

Table 4B. VCOSEL Input Function Table

Input Select		
VCOSEL1	VCOSEL2	
0	0	External VCXO, ÷2, (F_{MAX} = 2.7GHz)
0	1	Internal VCO, F_{NOM} = 622MHz
1	0	Internal VCO, F_{NOM} = 1.244MHz
1	1	External VCXO, ÷1, (F_{MAX} = 1.35GHz) (default)

Table 4C. Output Divider Select Function Table

Input Select				
SEL3	SEL4	SEL5	Input Divider	V_{TNOM} Frequency (MHz)
0	0	0	÷1	622
0	0	1	÷2	622 - 311
0	1	0	÷4	311 - 155
0	1	1	÷8	155 - 78
1	0	0	÷16	78 - 39
1	0	1	÷32	39 -19
1	1	0	÷64	19
1	1	1	No feedback to PLL from VCO (default)	

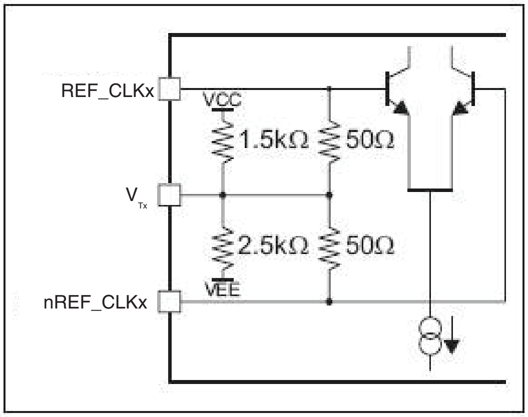


Figure 2. Termination of REF_CLKx Inputs

Absolute Maximum Ratings

Supply Voltage, $V_{CC,}$ V_{CCA}	-0.5V to 4.0V
Input Voltage, V_I	-0.5V to V_{CC} + 0.5V
Input Current, I_I	-1.0mA to 1.0mA
Output Voltage, V_O	-0.5V to V_{CC}
Output Current, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JC}	5°C/W
Operating Temperature, T_J	-40°C to 125°C
Storage Temperature, T_{STG}	-65°C to 125°C
Electrostatic Discharge Voltage, ESD	
HBM (Note1, 2)	1000V max.
CDM (Note 3)	50V max.

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

NOTE 1: Human Body Model tested to JESD22-A114-D

NOTE 2: Pins DCCAL (pin 39) and VCXO (pin 40) can handle ESD, HBM of maximum value: 500V

NOTE 3: Charge Device Model tested to JESD2-C101

Table 5A. Power Supply DC Characteristics, V_{CC} = 3.3V±5%, V_{EE} = 0V, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.08	3.3	V_{CC}	V
I_{CC}	Power Supply Current	Outputs Unloaded (Note 1)		165	206.5	mA
I_{CCA}	Analog Supply Current				8	mA

NOTE 1: Refer to Power Considerations on page 16.

Table 5B. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V±5%, V_{EE} = 0V, TA = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current; NOTE 1	SEL1:SEL5, VCOSEL1, VCOSEL2, OEAA, OEAB, OEA2, OEA4, OENA8, OEA16	V_{CC} = V_{IN} = 3.465V			200	µA
I_{IL}	Input Low Current; NOTE 1	SEL1:SEL5, VCOSEL1, VCOSEL2, OEAA, OEAB, OEA2, OEA4, OENA8, OEA16	V_{CC} = 3.465V, V_{IN} = 0V	-500			µA
V_{OL}	Output Low Voltage		I_{OL} = -1mA	0		0.4	V
V_{OH}	Output High Voltage		I_{OH} = 3mA	2.1		V_{CC}	V
V_{REF}	Internal LVT Reference			1.33	1.4	1.54	V
I_OOCHP	Charge Pump Output Current; NOTE 1			-155		155	µA
V_OOCHP	Charge Pump Output Voltage; NOTE 1, 2			0.3		V_{CC} - 0.3	V

NOTE 1: Under the condition of typical supply voltage.
NOTE 2: Assuming a purely capacitive load.

TABLE 5C. DIFFERENTIAL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, V_{EE} = 0V, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	V_{CC} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1, 2		0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 2, 3		V_{EE} + 0.5		V_{CC} - 0.85	V
R_{TERM}	Internal Termination Resistor			50		Ω

NOTE 1: V_{PP} = VREF_CLK[1:3] – VnREF_CLK[1:3].
NOTE 2: V_{IL} should not be less than -0.3V.
NOTE 3: Common mode voltage is defined as V_{IH}. Refer to parameter measurement information, *Differential Input Level* Diagram on page 10.

TABLE 5D. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, V_{EE} = 0V, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output Voltage High; NOTE 1		V_{CC} - 1.2		V_{CC} - 0.9	V
V_{OL}	Output Voltage Low; NOTE 1		V_{CC} - 2.0		V_{CC} - 1.6	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V
V_{REF}	Internal LVPECL Reference for VCXO Input		1.8	2.0	2.2	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V. Refer to Parameter Measurement information, *Output Load AC Test Circuit* Drawing on page 10.

TABLE 6. AC CHARACTERISTICS, V_{CC} = 3.3V±5%, V_{EE} = 0V, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{VCO}	VCO Tuning Range; NOTE 1			560		662	MHz
f_{IN}	Maximum Input Frequency			19	622.08	662	MHz
K_{VCO}	VCO Gain Constant		@ 622MHz		187		MHz/V
$J_{INTRINSIC}$	Intrinsic Jitter; NOTE 2		@ 622MHz Ref. Clock Frequency		0.17		mUI_{RMS}
$J_{TRANSFER}$	Jitter Transfer Function; NOTE 3 As an example, refer to Figure 5, pg 11		F_{JITTER} < 2MHz			0	dB
			F_{JITTER} > 2MHz			-20	dB/dec
D_{OUT}	Output Delay from Ref. Clock (REF_CLKx) to Clock Output (FOUTx); NOTE 6, 8	FOUTA, FOUTB		-75	75	225	ps
		FOUT2,4,8,16; NOTE 4		25	175	325	ps
Duty Cycle	Output Duty Cycle; NOTE 5 Refer to Parameter Measurement Information (Rise/Fall Time), See page 10 for drawing.			48	50	52	%
t_R / t_F	LVPECL Output Rise/Fall Time; See page 10 for drawing		20% to 80% differential			300	ps
*t*sk(o)	Output Skew; NOTE 7, 8					200	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: VCOSEL set to divide by 4.
NOTE 2: Measurement range 12kHz to 20MHz.
NOTE 3: The loop filter is dependent on the frequency of the reference clock signal in order to exceed ITU-T jitter masks.
NOTE 4: Parameter D_{OUT} is leakage current depent and only defined when the PLL is locked using the recommended loop filter; D_{OUT} is only defined for input and output signals of equal frequency.
NOTE 5: When external, the VCXO (divide by 1) is selected,
DCCAL can be used to obtain the duty cycle requirements.
NOTE 6: Reference Figure 3 on page 10.
NOTE 7: Output Skew measured from falling edge to falling edge. Refer to page 10.
NOTE 8: See Figure 4 to understand *Total Output Uncertainty.*

Parameter Measurement Information

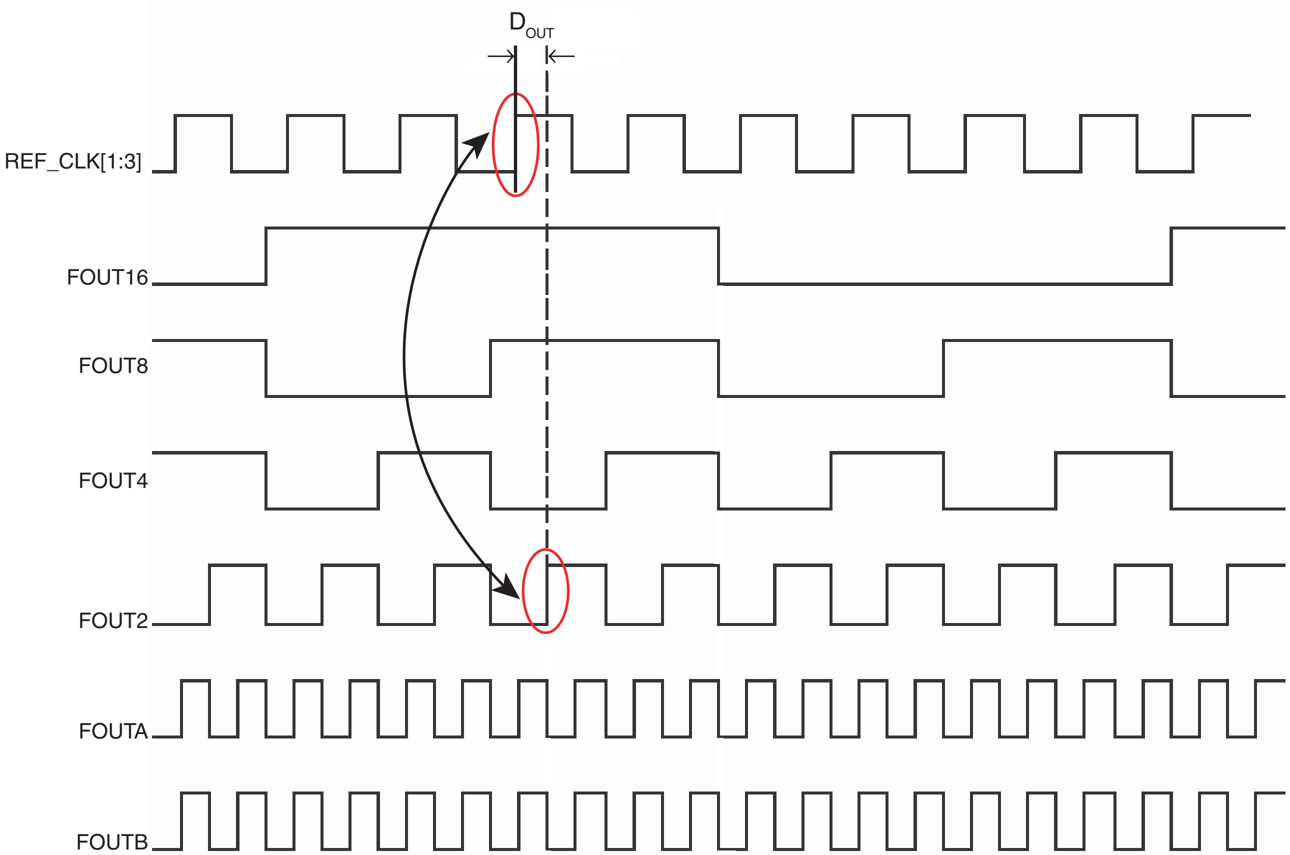


Figure 3. Timing of Output Clocks with Definition of Output Delay and Peak-to-Peak Skew, (see Note 4 on Page 8) (Example for REF_CLK to FOUT2)

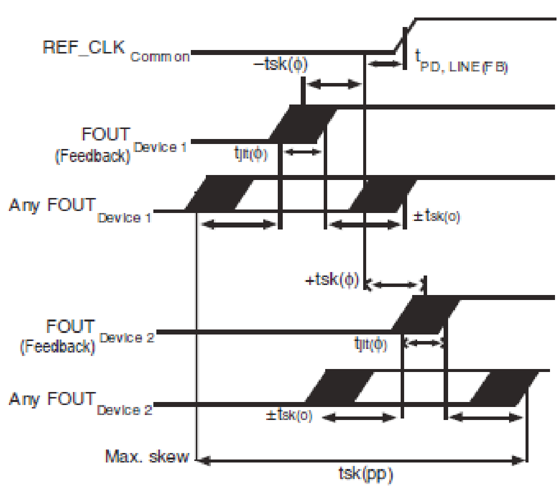
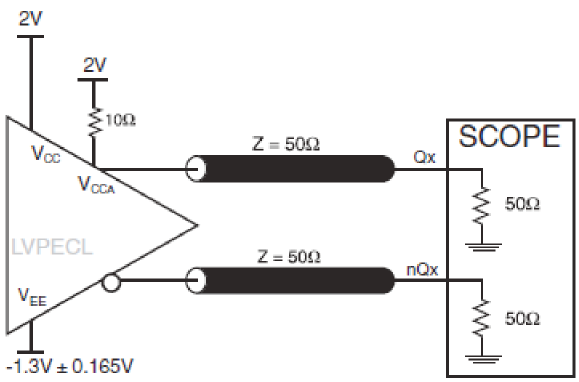
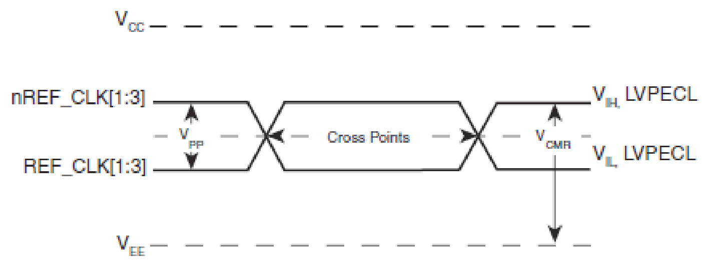


Figure 4. Total Output Uncertainty

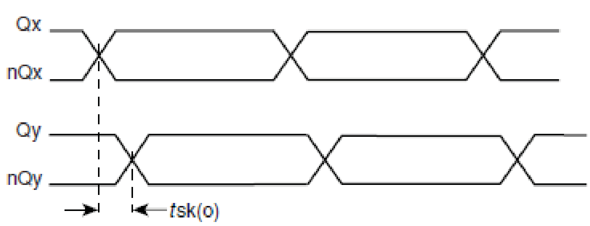
Parameter Measurement Information



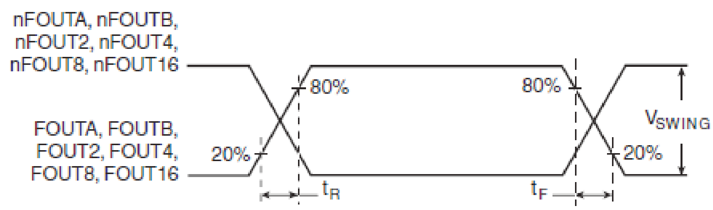
3.3V LVPECL Output Load Test Circuit



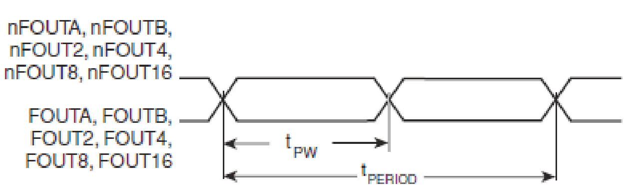
Differential Input Level



Output Skew



Output Rise/Fall Time



$$\text{Output Duty Cycle} = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

Output Duty Cycle/Pulse Width/Period

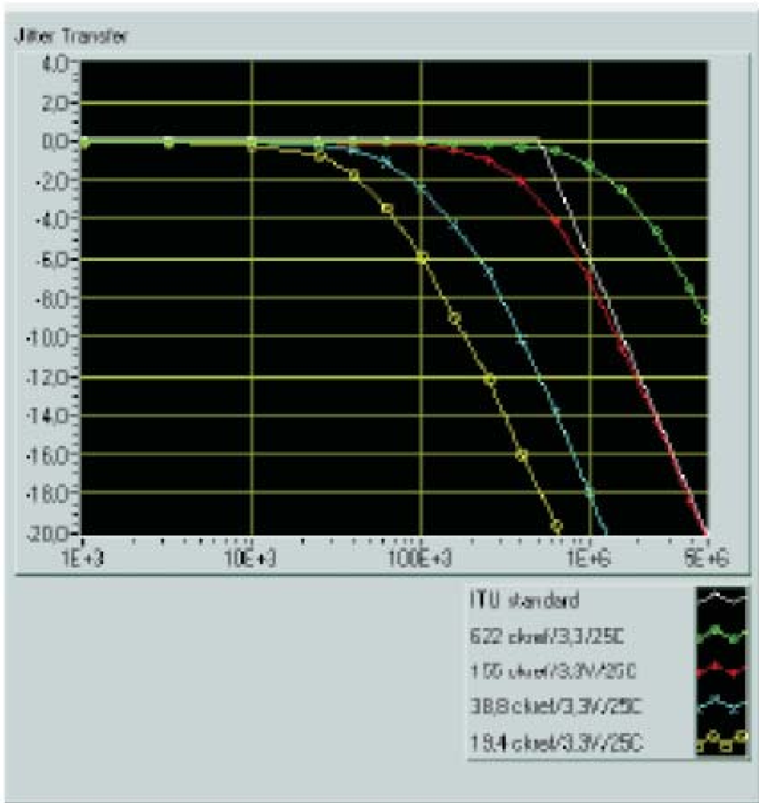


FIGURE 5. EXAMPLE OF JITTER TRANSFER BANDWIDTH VS. REFERENCE CLOCK FREQUENCY

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 843S06 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC} and V_{CCA} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 6* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional10Ω resistor along with a 10µF bypass capacitor be connected to the V_{CCA} pin. The 10Ω resistor can also be replaced by a ferrite bead.

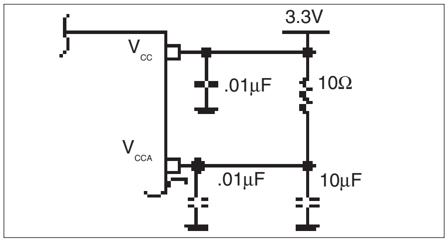


FIGURE 6. POWER SUPPLY FILTERING

3.3V DIFFERENTIAL INPUT WITH BUILT-IN 50Ω TERMINATION UNUSED INPUT HANDLING

To prevent oscillation and to reduce noise, it is recommended to have pullup and pulldown connect to true and complement of the unused input as shown in *Figure 7.*

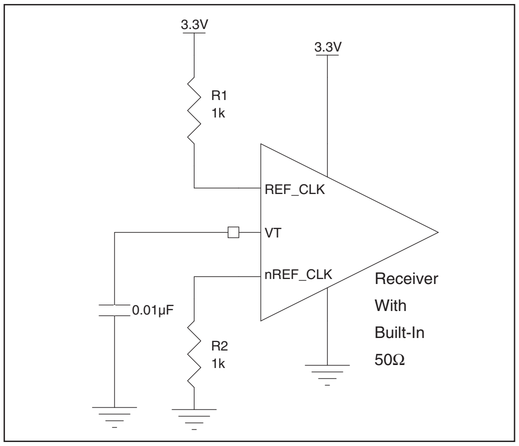


FIGURE 7. UNUSED INPUT HANDLING

Recommendations for Unused Input and Output Pins

Inputs:

REF_CLK/nREF_CLK Inputs

For applications not requiring the use of the differential input, both REF_CLK and nREF_CLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from REF_CLK to ground. See Figure 7.

LVCMOS/LVTTL Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ pull-up resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 8A and 8B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

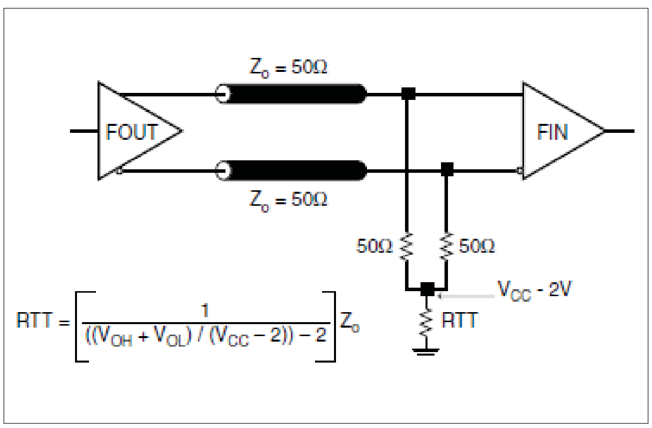


Figure 8A. LVPECL Output Termination

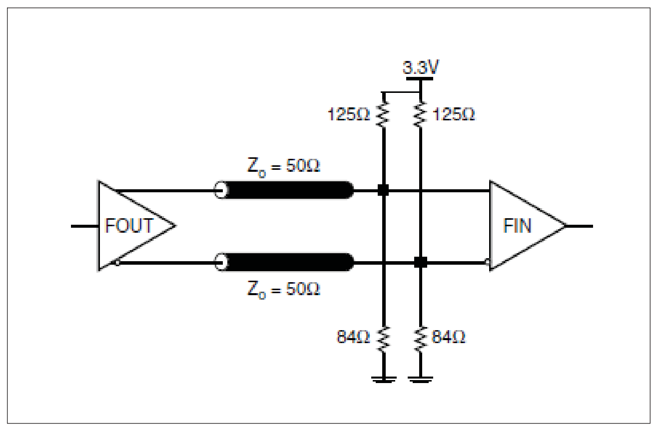


Figure 8B. LVPECL Output Termination

Practical Considerations

When designing the PCB it is important to consider noise issues. Decoupling capacitors should be applied to each supply pin. Output clock lines must be routed as transmission lines.

The reference clock inputs are terminated on-chip by 50Ω to the positive supply. The termination pins REF_CLK[1:3] are biased on-chip to 2V. The input impedance seen into REF_CLK[1:3] equals 1kΩ.

The LVPECL clock outputs are terminated according to *Figures 9B and 9C.*

NOTE: See page 13, *Recommendations for Unused Input and Output Pins.*

LVTTL select pins are terminated on-chip with a 16kΩ pull-up resistor giving a logic “1” when not connected.

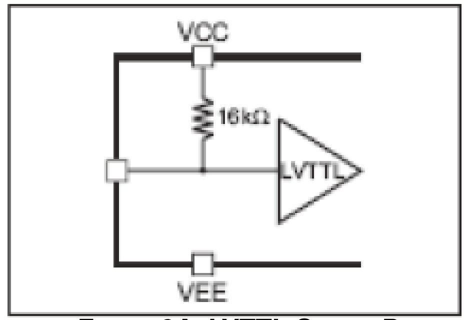


Figure 9A. LVTTL Select Pin

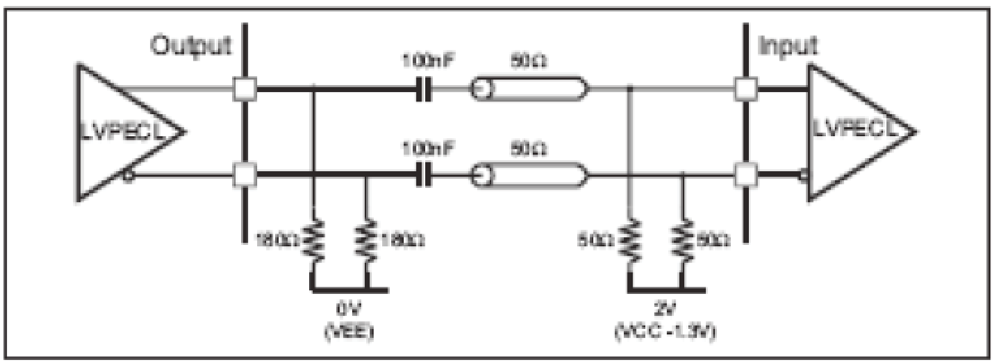


Figure 9B. LVPECL Output Termination, AC-Coupled

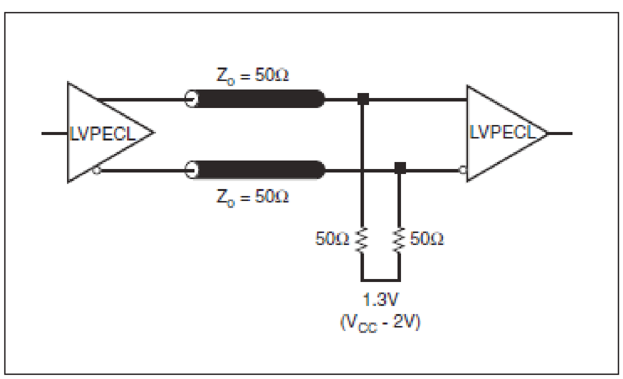


Figure 9C. LVPECL Output Termination, DC-Coupled

Application Note: IDT will provide an application note to allow the end-user to approximate the maximum time delay for NLock to be triggered when:

Within VCXO tuning range, the 843S06 will track VCXO rate of change according to bandwidth curve of PLL.

Outside of VCXO tuning range, the 843S06 will trigger NLOCK with a maximum time delay based on rate of change of input and time delay of NLOCK trigger mechanism (including noise immunity mechanism).

EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 10.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/ shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadfame Base Package, Amkor Technology.

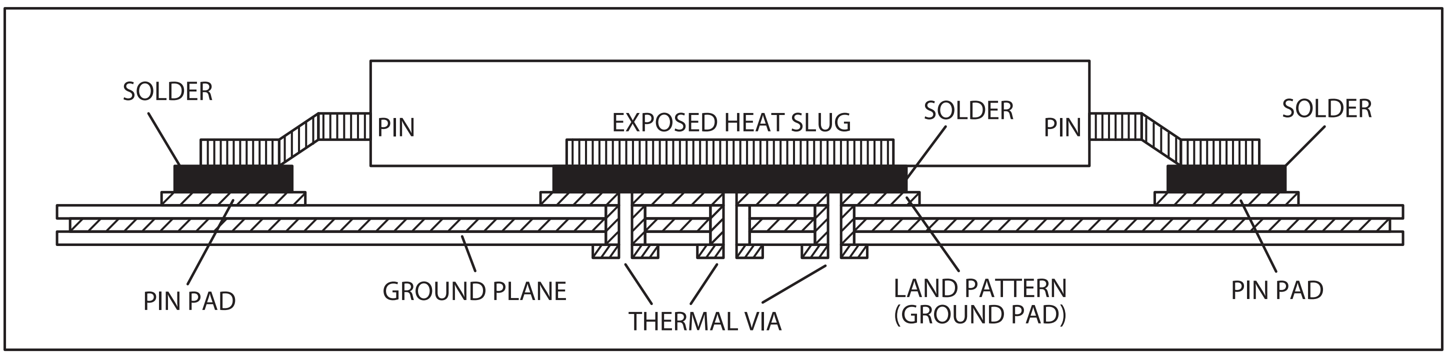


Figure 10. Assembly for Exposed Pad Thermal Release Path –Side View (Drawing not to Scale)

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 843S06.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the 843S06 is the sum of the core power plus the analog power, plus the power dissipated in the load(s). The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * (I_{CC_MAX} + I_{CCA_MAX}) = 3.465V * (206.5mA + 8mA) = **743.2mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 6 * 30mW = **180mW**

Total Power $_{\_MAX}$ (3.465V, with all outputs switching) = 743.2mW + 180mW = **923.2mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 42.5°C/W per Table 7A below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.923W * 42.5°C/W = 124.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 7A. THERMAL RESISTANCE θ_{JA} FOR 48-PIN LQFP, EDQUAD FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)	
	0
Multi-Layer PCB, JEDEC Standard Test Boards	42.5°C/W

TABLE 7B. THERMAL RESISTANCE θ_{JA} FOR PROPOSED 48-PIN TQFP, E-PAD FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	41.0°C/W	35.9°C/W	33.6°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 11.*

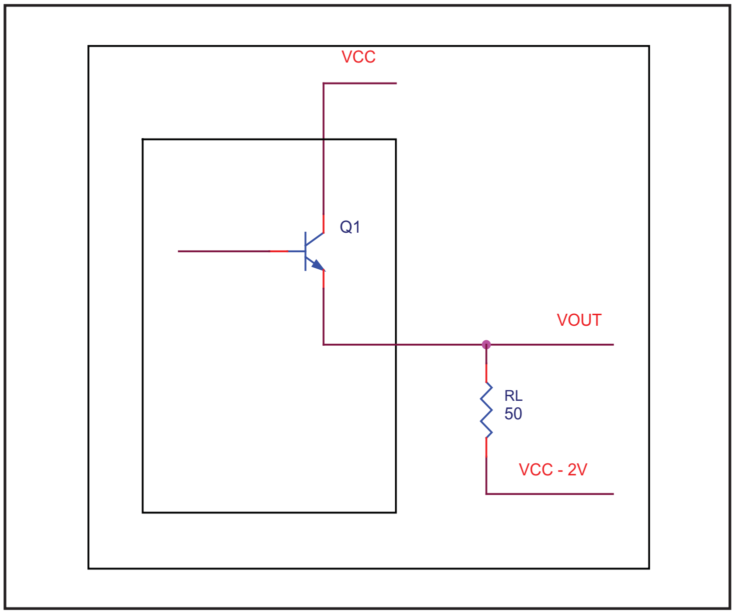


FIGURE 11. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.9V}$

  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.7V}$

  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC} - V_{OH\_MAX}))/R_L] * (V_{CC} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$

$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC} - V_{OL\_MAX}))/R_L] * (V_{CC} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 8A. θ_{JA} vs. Air Flow Table for 48 Lead LQFP, EQUAD

θ_{JA} by Velocity (Linear Feet per Minute)	
	0
Multi-Layer PCB, JEDEC Standard Test Boards	42.5°C/W

Table 8B. θ_{JA} vs. Air Flow Table for Proposed 48 Lead TQFP, E-Pad

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	41.0°C/W	35.9°C/W	33.6°C/W

Transistor Count

The transistor count for 843S06 is: 10,264

MTBF

25,470 years @ 60% C_L, 10,135 years @ 90% C_L

FIT will be closed after Rev. 1

PACKAGE OUTLINE - Y SUFFIX FOR 48 LEAD TQFP, E-PAD

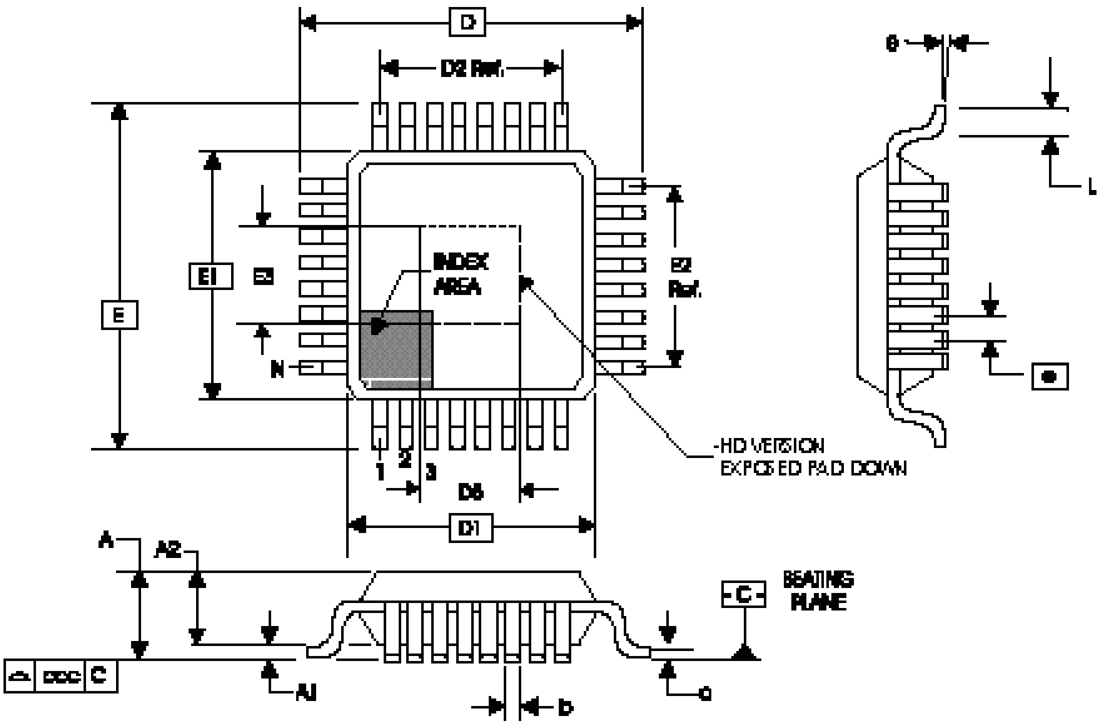


TABLE 9B. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	ABC - HD		
	MINIMUM	NOMINAL	MAXIMUM
N		48	
A	--	--	1.20
A1	0.05	--	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09		0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.50 BASIC	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.50 BASIC	
e		0.5 BASIC	
L	0.45	0.60	0.75
θ	0°		7°
ccc	--	--	0.08
D3 & E3		2.95	

Reference Document: JEDEC Publication 95, MS-026

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843S06FYLF	ICS843S06FYL	Proposed 48 Lead “Lead-Free” TQFP, E-Pad	Tray	-40°C to 85°C
843S06FYLFT	ICS843S06FYL	Proposed 48 Lead “Lead-Free” TQFP, E-Pad	Tape & Reel	-40°C to 85°C

Top Mark Information

ICS 843S06FYL <Lot/Date Code> <Lot Number>

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
10	T8B T9B T10	1 19 21 22	Added 48 TQFP, E-Pad package and information. Added 48 TQFP, E-Pad Thermal information. Added 48 Lead TQFP, E-Pad package outline and dimensions. Ordering Information Table - added 48 Lead TQFP, E-Pad part number and marking.	1/7/09
11	T7B T9B 10	17 21 22	Thermal Resistance Table - updated thermal numbers for new TQFP package. TQFP Package Dimensions - updated D3 & E3 dimension. Ordering Information Table - changed TQFP revision from “E” to “F”.	4/22/09
11	7B, 8B, 9B	1 17, 19, 21 17 22	Deleted HiPerClockS references. Deleted “Proposed” from Pin Assignment. Deleted “Proposed” Deleted HiPerClockS references. Deleted “Proposed” from 2nd top mark info box	4/29/13
11	T10	1, 20 21	Removed 48 Lead LQFP EDQUAD package information. Ordering Information - removed 48 lead EDQUAD orderable part number and Top Mark information. Updated data sheet format.	10/23/15

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