700MHz, Low Jitter, Crystal-To-3.3V LVPECL Frequency Synthesizer

84330-01

PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES MAY 6, 2017 (84330CV-01)

DATA SHEET

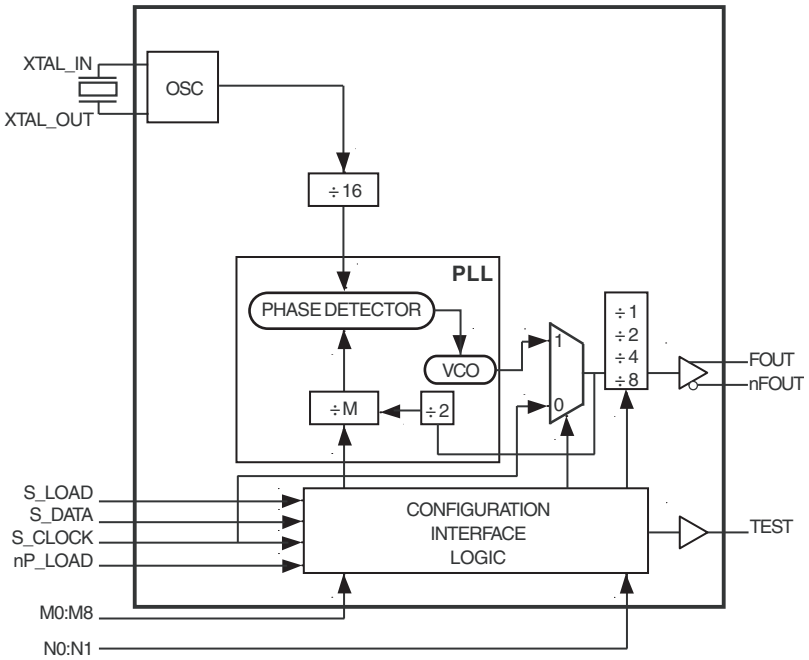
General Description

The 84330-01 is a general purpose, single output high frequency synthesize. The VCO operates at a frequency range of 250MHz to 700MHz. The VCO and output frequency can be programmed using the serial or parallel interfaces to the configuration logic. The output can be configured to divide the VCO frequency by 1, 2, 4, and 8. Output frequency steps from 250kHz to 2MHz can be achieved using a 16MHz crystal depending on the output divider setting.

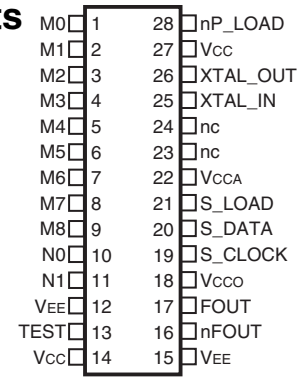
Features

- Fully integrated PLL, no external loop filter requirements
- One differential 3.3V LVPECL output
- Crystal oscillator interface: 10MHz – 25MHz
- Output frequency range: 31.25MHz – 700MHz
- VCO range: 250MHz – 700MHz
- Parallel or serial interface for programming M and N dividers during power-up
- RMS period jitter: 5ps (maximum)
- Cycle-to-cycle jitter: 40ps (maximum)
- 3.3V supply voltage
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package
- For functional replacement part use 8T49N242

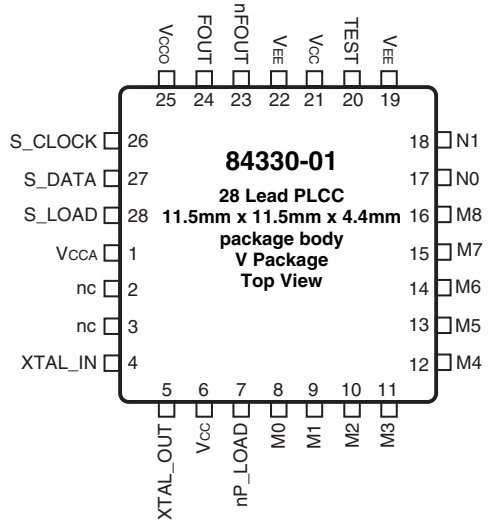
Block Diagram



Pin Assignments



84330-01
28 Lead SOIC
7.5mm x 18.05mm x 2.25mm package body
M Package
Top View



84330-01
28 Lead PLCC
11.5mm x 11.5mm x 4.4mm package body
V Package
Top View

Functional Description

NOTE: The functional description that follows describes operation using a 16MHz crystal. Valid PLL loop divider values for different crystal or input frequencies are defined in the Input Frequency Characteristics, Table 5, NOTE 1.

The 84330-01 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A parallel-resonant, fundamental crystal is used as the input to the on-chip oscillator. The output of the oscillator is divided by 16 prior to the phase detector. With a 16MHz crystal, this provides a 1MHz reference frequency. The VCO of the PLL operates over a range of 250MHz to 700MHz. The output of the M divider is also applied to the phase detector.

The phase detector and the M divider force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to each of the LVPECL output buffers. The divider provides a 50% output duty cycle.

The programmable features of the 84330-01 support two input modes and to program the M divider and N output divider. The two input operational modes are parallel and serial. *Figure 1* shows the timing diagram for each mode. In parallel mode, the nP_LOAD input is initially LOW. The data on inputs M0 through M8 and N0 through N1 is passed directly to the M divider and N output divider. On the LOW-to-HIGH transition of the nP_LOAD input, the data is latched and the M divider remains loaded until the next LOW transition on nP_LOAD or until a serial event occurs. The TEST output is Mode 000 (shift register out) when operating in the parallel input mode. The relationship between the VCO frequency, the crystal frequency and the M divider is defined as follows:

$$fVCO = \frac{fXTAL \times 2M}{16}$$

The M value and the required values of M0 through M8 are shown in Table 3B, Programmable VCO Frequency Function Table. Valid M values for which the PLL will achieve lock are defined as $125 \leq M \leq 350$. The frequency out is defined as follows:

$$fout = \frac{fVCO}{N} = \frac{fXTAL \times 2M}{16 \quad N}$$

Serial operation occurs when nP_LOAD is HIGH and S_LOAD is LOW. The shift register is loaded by sampling the S_DATA bits with the rising edge of S_CLOCK. The contents of the shift register are loaded into the M divider when S_LOAD transitions from LOW-to-HIGH. The M divide and N output divide values are latched on the HIGH-to-LOW transition of S_LOAD. If S_LOAD is held HIGH, data at the S_DATA input is passed directly to the M divider on each rising edge of S_CLOCK. The serial mode can be used to program the M and N bits and test bits T2:T0. The internal registers T2:T0 determine the state of the TEST output as follows in the table below:

T2	T1	T0	TEST Output	fOUT
0	0	0	Shift Register Out	fOUT
0	0	1	HIGH	fOUT
0	1	0	PLL Reference XTAL ÷16	fOUT
0	1	1	(VCO ÷ M) /2 (non 50% Duty Cycle M Divider)	fOUT
1	0	0	fOUT, LVCMOS Output Frequency < 200MHz	fOUT
1	0	1	LOW	fOUT
1	1	0	(S_CLOCK ÷ M) /2 (non 50% Duty Cycle M Divider)	S_CLOCK ÷ N Divider
1	1	1	fOUT ÷ 4	fOUT

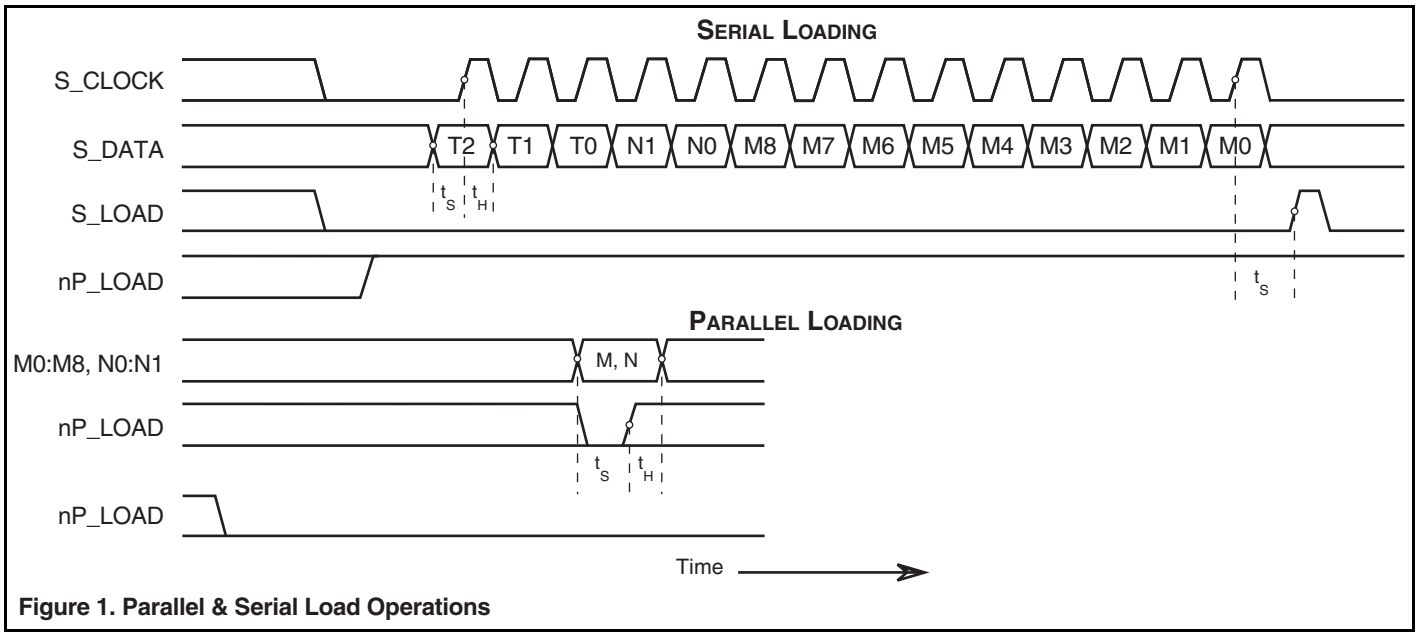


Figure 1. Parallel & Serial Load Operations

Table 1. Pin Descriptions

Name	Type		Description
M0, M1, M2, M3, M4, M5, M6, M7, M8	Input	Pullup	M divider inputs. Data latched on LOW-to-HIGH transition of nP_LOAD input. LVCMOS/LVTTL interface levels.
N0, N1	Input	Pullup	Determines output divider value as defined in Table 3C, Function Table. LVCMOS/LVTTL interface levels.
V_{EE}	Power		Negative supply pins.
TEST	Output		Test output which is used in the serial mode of operation. Single-ended LVPECL interface levels.
V_{CC}	Power		Core supply pins.
FOUT, nFOUT	Output		Differential output pair for the synthesizer. LVPECL interface levels.
V_{CCO}	Power		Output supply pin for LVPECL outputs.
nc	Unused		No connect.
S_CLOCK	Input	Pulldown	Clocks the serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK. LVCMOS/LVTTL interface levels.
S_DATA	Input	Pulldown	Shift register serial input. Data sampled on the rising edge of S_CLOCK. LVCMOS/LVTTL interface levels.
S_LOAD	Input	Pulldown	Controls transition of data from shift register into the M divider. LVCMOS/LVTTL interface levels.
V_{CCA}	Power		Analog supply pin.
XTAL_IN XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
nP_LOAD	Input	Pullup	Parallel load input. Determines when data present at M8:M0 is loaded into M divider, and when data present at N1:N0 sets the N output divider value. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Parallel and Serial Mode Function Table

Inputs						Conditions
nP_LOAD	M	N	S_LOAD	S_CLOCK	S_DATA	
X	X	X	X	X	X	Reset. M and N bits are all set HIGH.
L	Data	Data	X	X	X	Data on M and N inputs passed directly to the M divider and N output divider. TEST mode 000.
↑	Data	Data	L	X	X	Data is latched into input registers and remains loaded until next LOW transition or until a serial event occurs.
H	X	X	L	↑	Data	Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK.
H	X	X	↑	L	Data	Contents of the shift register are passed to the M divider and N output divider.
H	X	X	↓	L	Data	M divider and N output divider values are latched.
H	X	X	L	X	X	Parallel or serial input do not affect shift registers.
H	X	X	H	↑	Data	S_DATA passed directly to M divider as it is clocked.

NOTE: L = LOW
H = HIGH
X = Don't care
↑ = Rising edge transition
↓ = Falling edge transition

Table 3B. Programmable VCO Frequency Function Table

VCO Frequency (MHz)	M Divide	256	128	64	32	16	8	4	2	1
		M8	M7	M6	M5	M4	M3	M2	M1	M0
250	125	0	0	1	1	1	1	1	0	1
252	126	0	0	1	1	1	1	1	1	0
254	127	0	0	1	1	1	1	1	0	1
256	128	0	1	0	0	0	0	0	1	0
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
696	348	1	0	1	0	1	1	1	0	0
698	349	1	0	1	0	1	1	1	0	1
700	350	1	0	1	0	1	1	1	1	0

NOTE 1: These M divide values and the resulting frequencies correspond to a TEST_CLK or crystal frequency of 16MHz.

Table 3C. Programmable Output DividerFunction Table

Inputs		N Divider Value	Output Frequency (MHz)	
N1	N0		Minimum	Maximum
0	0	2	125	350
0	1	4	62.5	175
1	0	8	31.25	87.5
1	1	1	250	700

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to V_{CC} -0.5V to V_{CC} + 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA} 28 Lead SOIC 28 Lead PLCC	 57°C/W (0 mps) 45.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				160	mA
I_{CCA}	Analog Supply Current				16	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	S_CLOCK, S_DATA, S_LOAD	$V_{CC} = V_{IN} = 3.465V$			150	µA
		nP_LOAD, M0:M8, N0, N1	$V_{CC} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	S_CLOCK, S_DATA, S_LOAD	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-5			µA
		nP_LOAD, M0:M8, N0, N1	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{OH}	Output High Voltage	TEST; NOTE 1	$V_{CCO} = 3.3V±5\%$	2.6			V
V_{OL}	Output Low Voltage	TEST; NOTE 1	$V_{CCO} = 3.3V±5\%$			0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{CCO}/2$. See Parameter Measurement Information section. *Load Test Circuit diagrams.*

Table 4C. LVPECL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Current; NOTE 1		$V_{CCO} – 1.4$		$V_{CCO} – 0.9$	µA
V_{OL}	Output Low Current; NOTE 1		$V_{CCO} – 2.0$		$V_{CCO} – 1.7$	µA
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to $V_{CCO} – 2V$.

Table 5. Input Frequency Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	XTAL_IN, XTAL_OUT; NOTE 1		10		25	MHz
		S_CLOCK				50	MHz

NOTE 1: For the crystal frequency range, the M value must be set to achieve the minimum or maximum VCO frequency range of 250MHz to 700MHz range. Using the minimum input frequency of 10MHz, valid values of M are $200 \le M \le 511$. Using the maximum input frequency of 25MHz, valid values of M are $80 \le M \le 224$.

Table 6. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		10		25	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

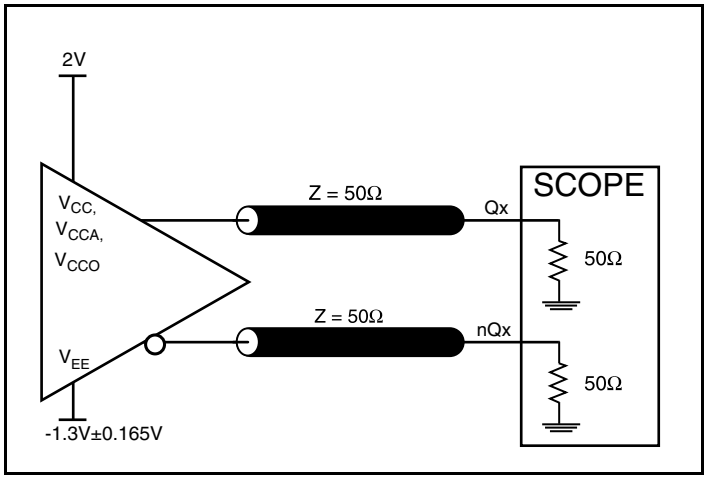
AC Electrical Characteristics

Table 7. AC Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to $70°C$

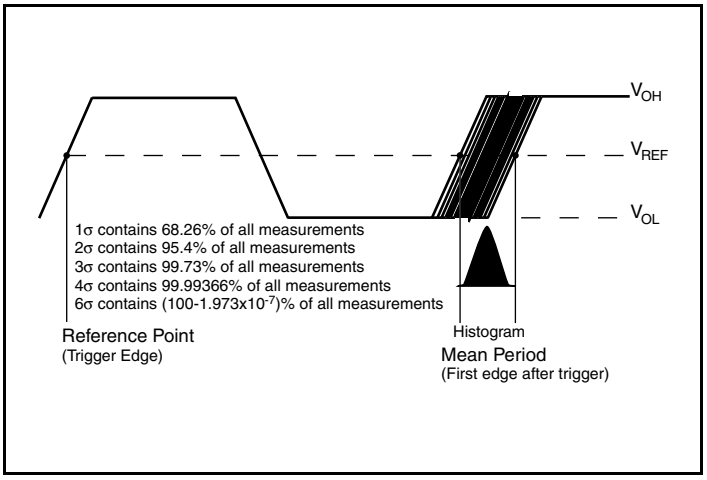
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency					700	MHz
$t_{jit(cc)}$	Cycle-to-Cycle Jitter; NOTE 1, 2					40	ps
$t_{jit(per)}$	Period Jitter, RMS; NOTE 1, 2					5	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	200		600	ps
t_S	Setup Time	M, N to nP_LOAD		20			ns
		S_DATA to S_CLOCK		20			ns
		S_CLOCK to S_LOAD		20			ns
t_H	Hold Time	M, N to nP_LOAD		20			ns
		S_DATA to S_CLOCK		20			ns
odc	Output Duty Cycle			45		55	%
t_{LOCK}	PLL Lock Time					10	ms

See Parameter Measurement Information section.
Characterized using XTAL inputs.
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: See Applications Section.

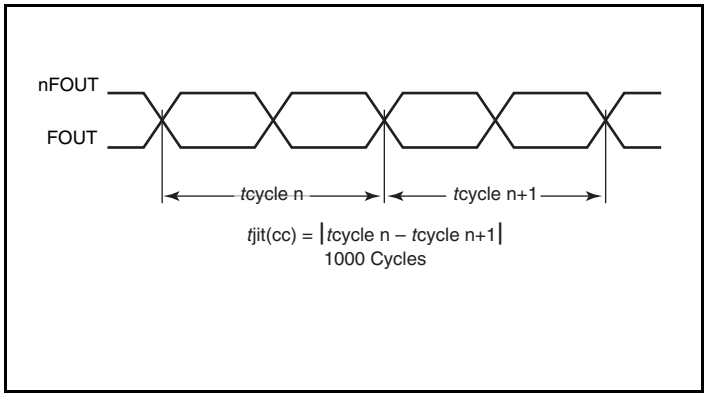
Parameter Measurement Information



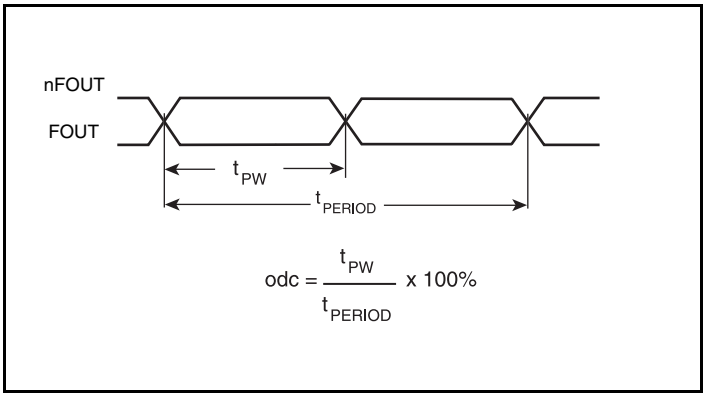
3.3/3.3V LVPECL Output Load AC Test Circuit



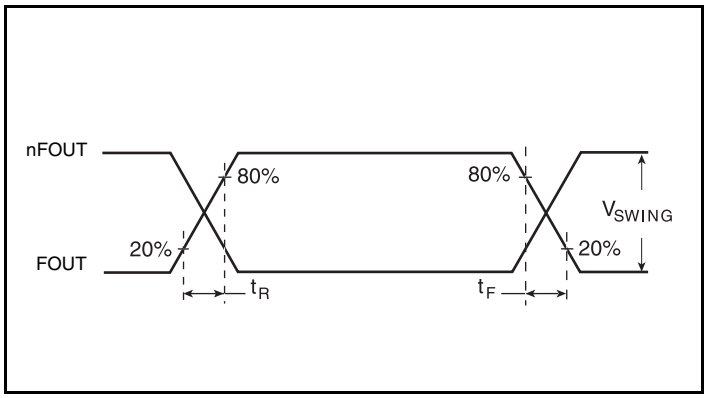
Period Jitter



Cycle-to-Cycle Jitter



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 84330-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA} and V_{CCO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 2* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{CCA} pin. The 10Ω resistor can also be replaced by a ferrite bead.

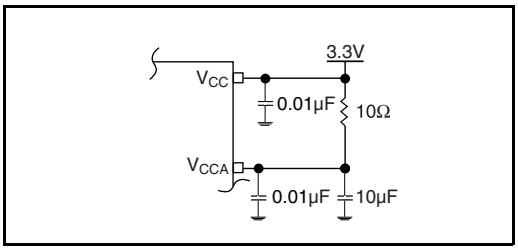


Figure 2. Power Supply Filtering

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

TEST Output

The unused TEST output can be left floating. There should be no trace attached.

LVPECL Output

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Crystal Input Interface

The 84330-01 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 3* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error. These same capacitor values will tune any 18pF parallel resonant crystal over the frequency range and other parameters specified in this data sheet. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

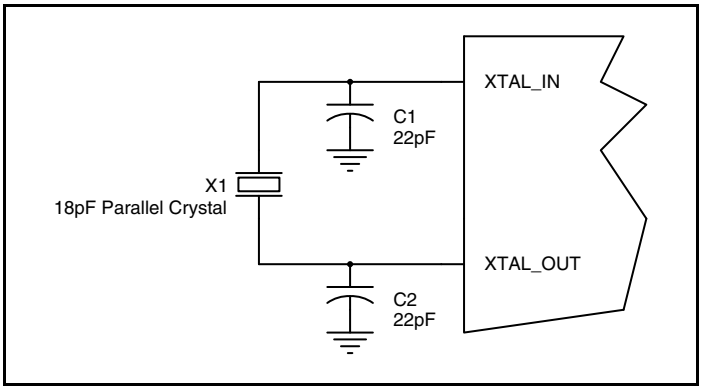


Figure 3. Crystal Input Interface

Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 4A.* The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

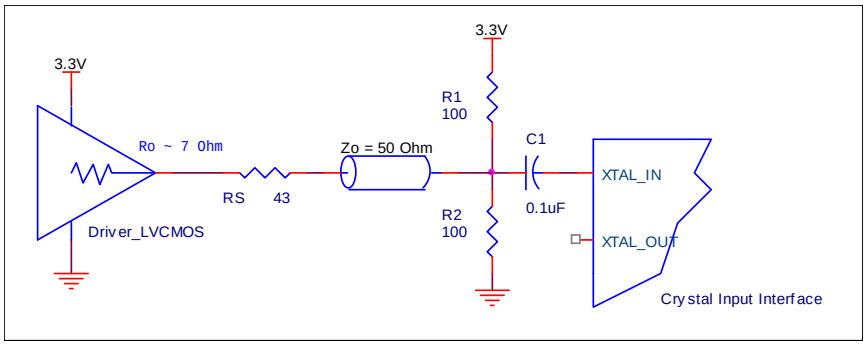


Figure 4A. General Diagram for LVCMOS Driver to XTAL Input Interface

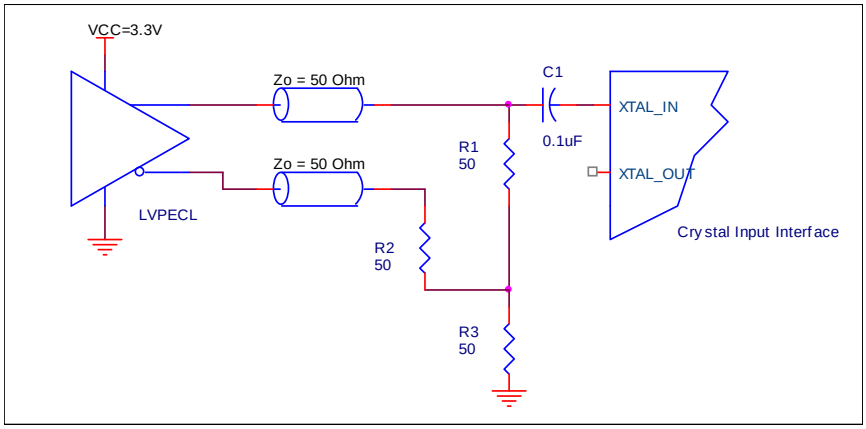


Figure 4B. General Diagram for LVPECL Driver to XTAL Input Interface

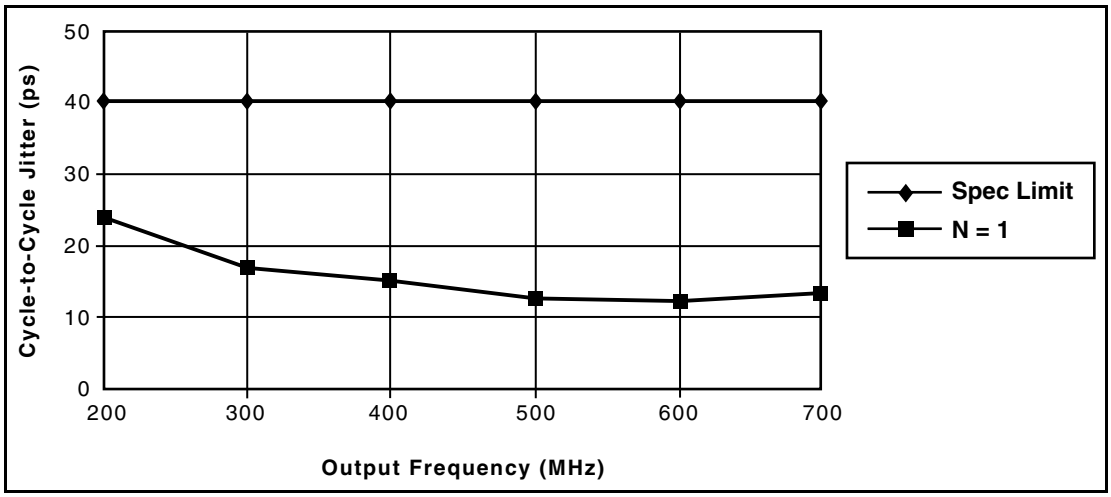


Figure 5. Cycle-to-Cycle Jitter vs. fOUT (using a 16MHz crystal)

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 6A and 6B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

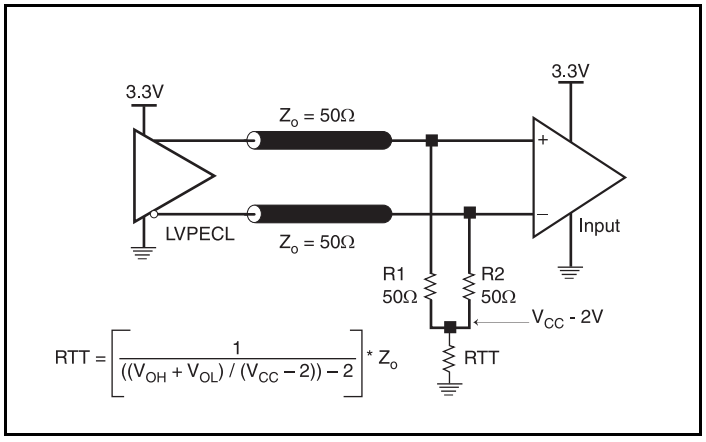


Figure 6A. 3.3V LVPECL Output Termination

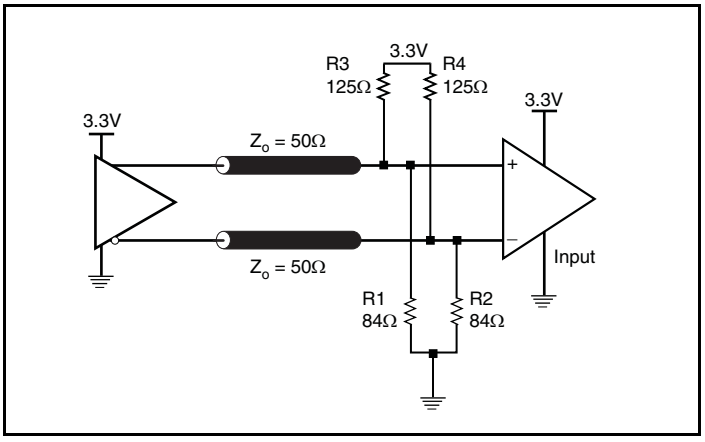


Figure 6B. 3.3V LVPECL Output Termination

Schematic Example

Figure 7 shows a schematic example of using an 84330-01. The crystal inputs are parallel resonant crystals with load capacitor C_L = 18pF. The frequency fine tuning capacitors C1 and C2 are approximately 22pF. The tuning capacitor value can be slightly adjusted to optimize the frequency accuracy. This schematic example shows hardwired logic control input handling. The logic inputs can also be driven by 3.3V LVCMOS drivers. It is recommended to have one bypass capacitor per power pin. In general, the bypass capacitor values are ranged from 0.01µF to 0.1µF. Each bypass capacitor should be located as close as possible to the power pin. The low pass filter R7, C11 and C16 for clean analog supply should also be located as close to the V_{CCA} pin as possible. Only one example of LVPECL termination is shown in this schematic. Additional LVPECL terminations can be found in the LVPECL Termination Application Note.

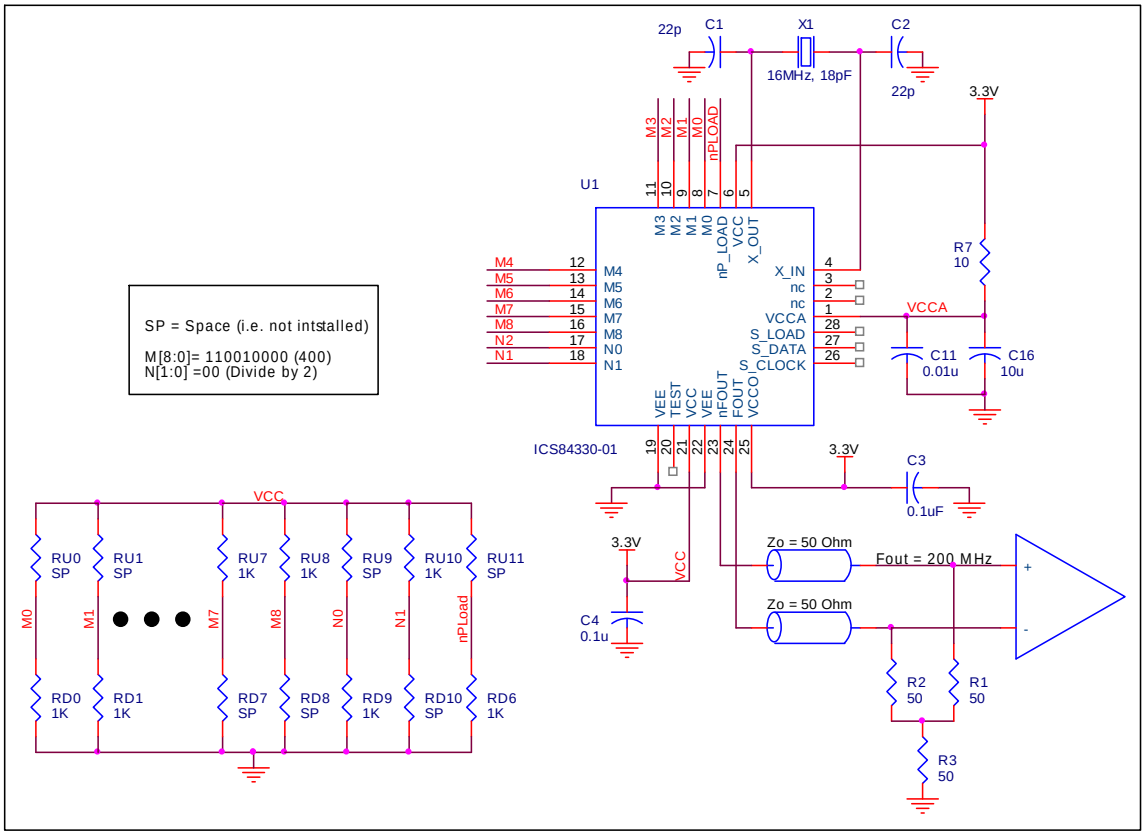


Figure 7. 84330-01 Schematic of Recommended Layout

Power Considerations

This section provides information on power dissipation and junction temperature for the 84330-01.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 84330-01 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 160mA = **554.4mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**

Total Power$_{\_MAX}$ (3.3V, with all outputs switching) = 554.4mW + 30mW = **584.4mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 57°C/W per Table 8A below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.584W * 57°C/W = 103.3°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 8A. Thermal Resistance θ_{JA} for 28 Lead SOIC, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**		
Multi-Layer PCB, JEDEC Standard Test Boards	57°C/W		

Table 8B. Thermal Resistance θ_{JA} for 28 Lead PLCC, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**		
Multi-Layer PCB, JEDEC Standard Test Boards	45.7°C/W		

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 8.*

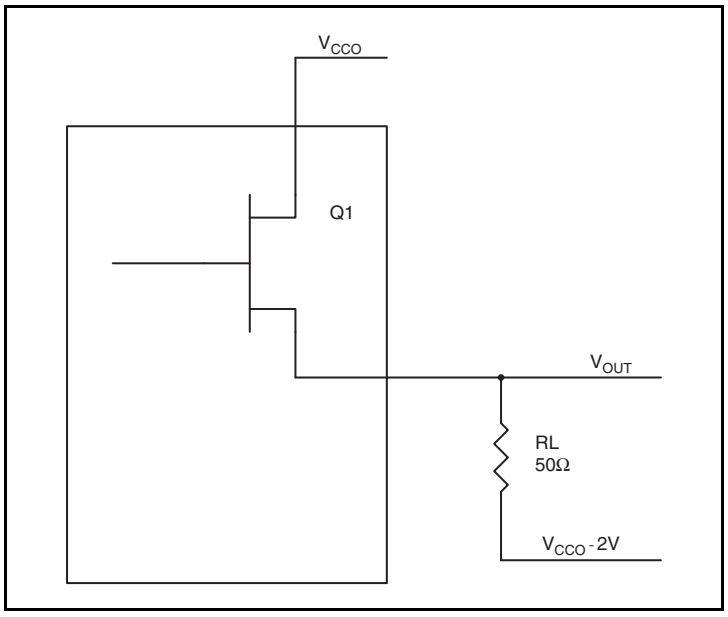


Figure 8. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} – 0.9V}$
  $(V_{CCO\_MAX} – V_{OH\_MAX}) = \mathbf{0.9V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CO\_MAX} – 1.7V}$
  $(V_{CCO\_MAX} – V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – 0.9V)/50Ω] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – 1.7V)/50Ω] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 9A. θ_{JA} vs. Air Flow Table for a 28 Lead SOIC

θ_{JA} vs. Air Flow			
Meters per Second	**0**		
Multi-Layer PCB, JEDEC Standard Test Boards	57°C/W		

Table 9B. θ_{JA} vs. Air Flow Table for a 28 Lead PLCC

θ_{JA} vs. Air Flow			
Meters per Second	**0**		
Multi-Layer PCB, JEDEC Standard Test Boards	45.7°C/W		

Transistor Count

The transistor count for 84330-01 is: 4498

Pin compatible with the SY89430V

Package Outline and Package Dimensions

Package Outline - M Suffix for 28 Lead SOIC

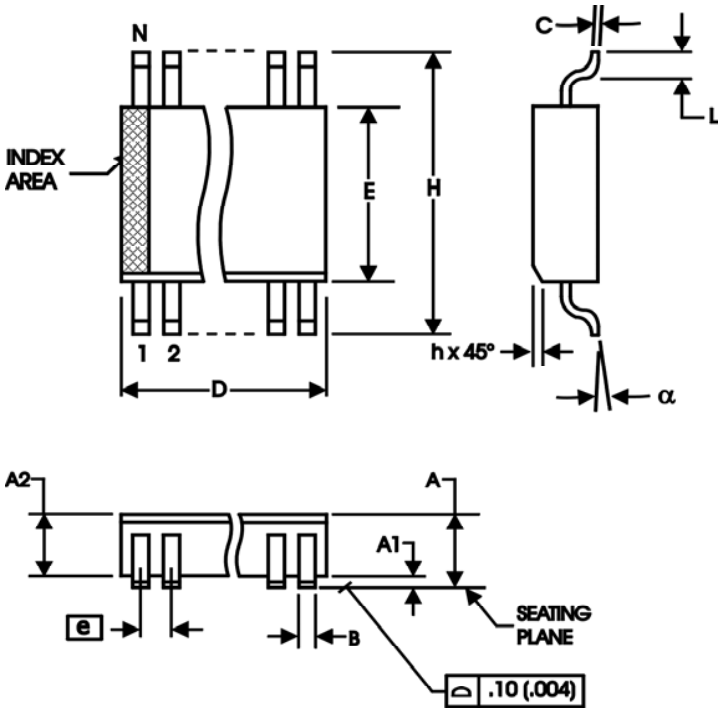


Table 10A. Package Dimensions for 28 Lead SOIC

JEDEC: 300 MIL All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	28	
A		2.65
A1	0.10	
A2	2.05	2.55
B	0.33	0.51
C	0.18	0.32
D	17.70	18.40
E	7.40	7.60
e	1.27 Basic	
H	10.0	10.65
h	0.25	0.75
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-013, MS-119

Package Outline - V Suffix for 28 Lead PLCC

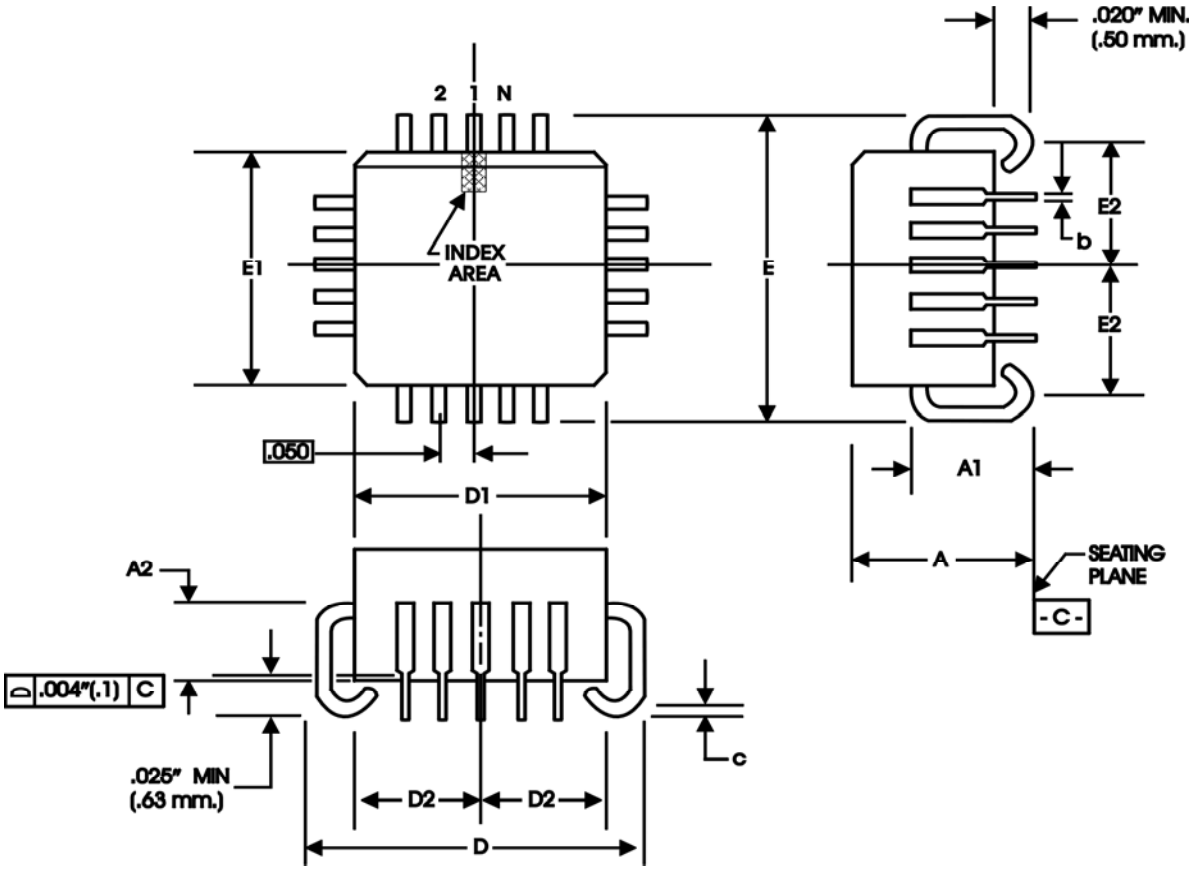


Table 10B. Package Dimensions for 28 Lead PLCC

JEDEC All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	28	
A	4.19	4.57
A1	2.29	3.05
A2	1.57	2.11
b	0.33	0.53
c	0.19	0.32
D & E	12.32	12.57
D1 & E1	11.43	11.58
D2 & E2	4.85	5.56

Reference Document: JEDEC Publication 95, MS-018

Ordering Information

Table 11. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
84330CV-01LF	ICS84330CV-01LF	“Lead-Free” 28 Lead PLCC	Tube	0°C to 70°C
84330CV-01LFT	ICS84330CV-01LF	“Lead-Free” 28 Lead PLCC	1000 Tape & Reel	0°C to 70°C
84330CM-01LF	ICS84330CM-01LF	“Lead-Free” 28 Lead SOIC	Tube	0°C to 70°C
84330CM-01LFT	ICS84330CM-01LF	“Lead-Free” 28 Lead SOIC	1000 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T7 T11	7 10 17	AC Electrical Characteristics - Added Thermal Note. Updated Overdriving the XTAL Interface section. Ordering Information - Added “Lead Free” Marking to lead-free 28 Lead SOIC. Updated head/footer throughout the datasheet.	2/23/10
A	T11	17	Ordering Information - removed leaded devices. Updated data sheet format.	4/22/15
A			Product Discontinuation Notice - Last time buy expires May 6, 2017. PDN CQ-16-01	5/26/16

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