

General Description

The 843251I-15 is an Ethernet Clock Generator. The 843251I-15 uses an 18pF parallel resonant crystal over the range of 23.2MHz - 30MHz. For Ethernet applications, a 25MHz crystal is used. The 843251I-15 uses IDT's 3rd generation low phase noise VCO technology, and can achieve <1ps rms phase jitter performance over the 1.875MHz – 20MHz integration range. The 843251I-15 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

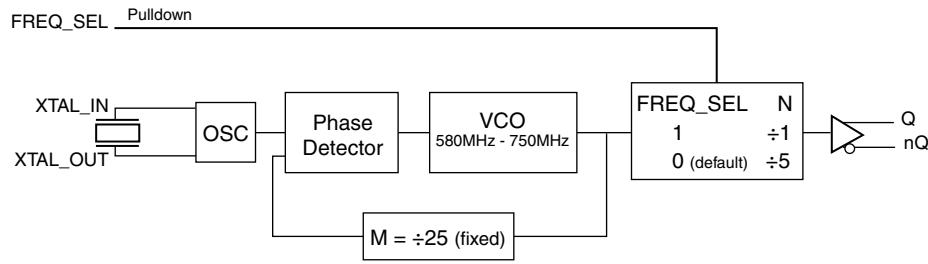
Features

- One differential 3.3V LVPECL output pair
- Crystal oscillator interface, 18pF parallel resonant crystal (23.2MHz – 30MHz)
- Output frequency range: 116MHz – 150MHz and 580MHz – 750MHz
- VCO range: 580MHz – 750MHz
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz – 20MHz): 0.45ps (typical), 3.3V
- Full 3.3V or 2.5V supply modes
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

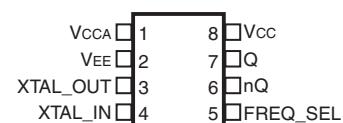
Common Configuration Table

| Crystal Frequency (MHz) | Inputs | | | | Output Frequency (MHz) |
|-------------------------|----------|----|---|--------------------------|------------------------|
| | FREQ_SEL | M | N | Multiplication Value M/N | |
| 25 | 1 | 25 | 1 | 25 | 625 |
| 26.667 | 1 | 25 | 1 | 25 | 666.67 |
| 25 | 0 | 25 | 5 | 5 | 125 |
| 26.667 | 0 | 25 | 5 | 5 | 133.33 |

Block Diagram



Pin Assignment



843251I-15
8 Lead TSSOP
4.40mm x 3.0mm x 0.925mm
package body
G Package
Top View

Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

| Number | Name | Type | Description | | | |
|--------|---------------------|--------|---|--|--|--|
| 1 | V _{CCA} | Power | Analog supply pin. | | | |
| 2 | V _{EE} | Power | Negative supply pin. | | | |
| 3, 4 | XTAL_OUT XTAL_IN | Input | Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output. | | | |
| 5 | FREQ_SEL | Input | Pulldown | Frequency select pin. LVCMOS/LVTTL interface levels. | | |
| 6, 7 | nQ, Q | Output | Differential output pair. LVPECL interface levels. | | | |
| 8 | V _{CC} | Power | Core supply pin. | | | |

NOTE: Pulldown refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | 4 | | pF |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 51 | | kΩ |

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed

in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|---|--------------------------|
| Supply Voltage, V_{CC} | 4.6V |
| Inputs, V_I | -0.5V to $V_{CC} + 0.5V$ |
| Outputs, I_O Continuous Current Surge Current | 50mA 100mA |
| Package Thermal Impedance, θ_{JA} | 129.5°C/W (0 mps) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|-----------------|---------|----------|-------|
| V_{CC} | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{CCA} | Analog Supply Voltage | | $V_{CC} - 0.10$ | 3.3 | V_{CC} | V |
| I_{EE} | Power Supply Current | | | | 83 | mA |
| I_{CCA} | Analog Supply Current | | | | 10 | mA |

Table 3B. Power Supply DC Characteristics, $V_{CC} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|-----------------|---------|----------|-------|
| V_{CC} | Core Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| V_{CCA} | Analog Supply Voltage | | $V_{CC} - 0.08$ | 2.5 | V_{CC} | V |
| I_{EE} | Power Supply Current | | | | 78 | mA |
| I_{CCA} | Analog Supply Current | | | | 8 | mA |

Table 3C. LVCMOS/LVTTL DC Characteristics, $V_{CC} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|--------------------|---|---------|---------|----------------|---------|
| V_{IH} | Input High Voltage | $V_{CC} = 3.3V$ | 2 | | $V_{CC} + 0.3$ | V |
| | | $V_{CC} = 2.5V$ | 1.7 | | $V_{CC} + 0.3$ | V |
| V_{IL} | Input Low Voltage | $V_{CC} = 3.3V$ | -0.3 | | 0.8 | V |
| | | $V_{CC} = 2.5V$ | -0.3 | | 0.7 | V |
| I_{IH} | Input High Current | $V_{CC} = V_{IN} = 3.465V$ or $2.625V$ | | | 150 | μA |
| I_{IL} | Input Low Current | $V_{CC} = 3.465V$ or $2.625V$, $V_{IN} = 0V$ | -5 | | | μA |

Table 3D. LVPECL DC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|-----------------------------------|-----------------|----------------|---------|----------------|-------|
| V_{OH} | Output High Current; NOTE 1 | | $V_{CC} - 1.4$ | | $V_{CC} - 0.9$ | V |
| V_{OL} | Output Low Current; NOTE 1 | | $V_{CC} - 2.0$ | | $V_{CC} - 1.7$ | V |
| V_{SWING} | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

NOTE 1: Outputs termination with 50Ω to $V_{CC} - 2V$.

Table 3E. LVPECL DC Characteristics, $V_{CC} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|-----------------------------------|-----------------|----------------|---------|----------------|-------|
| V_{OH} | Output High Current; NOTE 1 | | $V_{CC} - 1.4$ | | $V_{CC} - 0.9$ | V |
| V_{OL} | Output Low Current; NOTE 1 | | $V_{CC} - 2.0$ | | $V_{CC} - 1.5$ | V |
| V_{SWING} | Peak-to-Peak Output Voltage Swing | | 0.4 | | 1.0 | V |

NOTE 1: Outputs termination with 50Ω to $V_{CC} - 2V$.

Table 4. Crystal Characteristics

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | 23.2 | | 30 | MHz |
| Equivalent Series Resistance (ESR) | | | | 40 | Ω |
| Shunt Capacitance | | | | 7 | pF |

NOTE: It is not recommended to overdrive the crystal input with an external clock.

AC Electrical Characteristics

Table 5A. AC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------------------------|----------------------------------|--|---------|---------|---------|-------|
| fout | Output Frequency | FREQ_SEL = 0 | 116 | | 150 | MHz |
| | | FREQ_SEL = 1 | 580 | | 750 | MHz |
| t _{jit} (\emptyset) | RMS Phase Jitter, Random; NOTE 1 | 125MHz, (Integration Range: 1.875MHz – 20MHz) | | 0.45 | | ps |
| | | 625MHz, (Integration Range: 1.875MHz – 20MHz) | | 0.34 | | ps |
| t _R / t _F | Output Rise/Fall Time | 20% to 80% | 100 | | 600 | ps |
| odc | Output Duty Cycle | | 47 | | 53 | % |

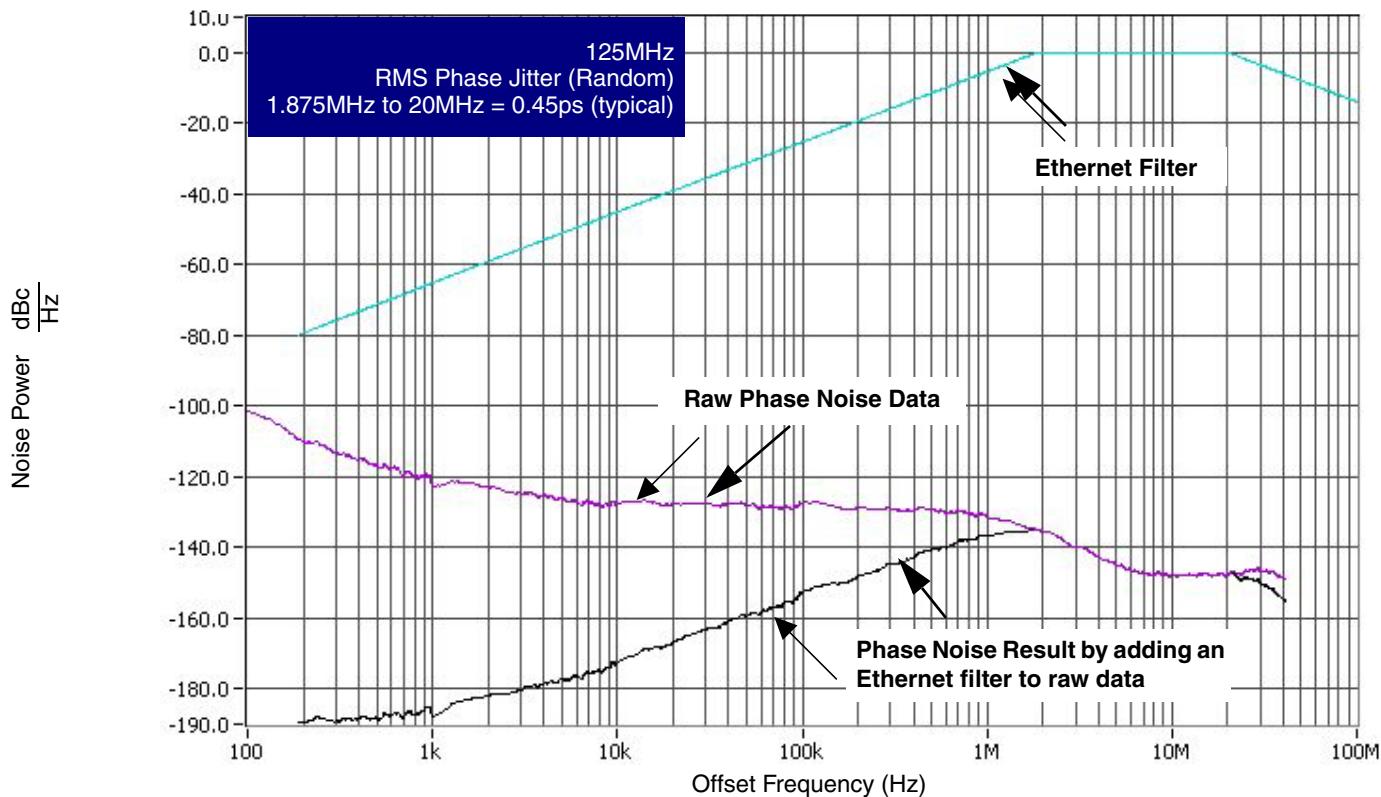
NOTE 1: Refer to Phase Noise Plots.

Table 5B. AC Characteristics, $V_{CC} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

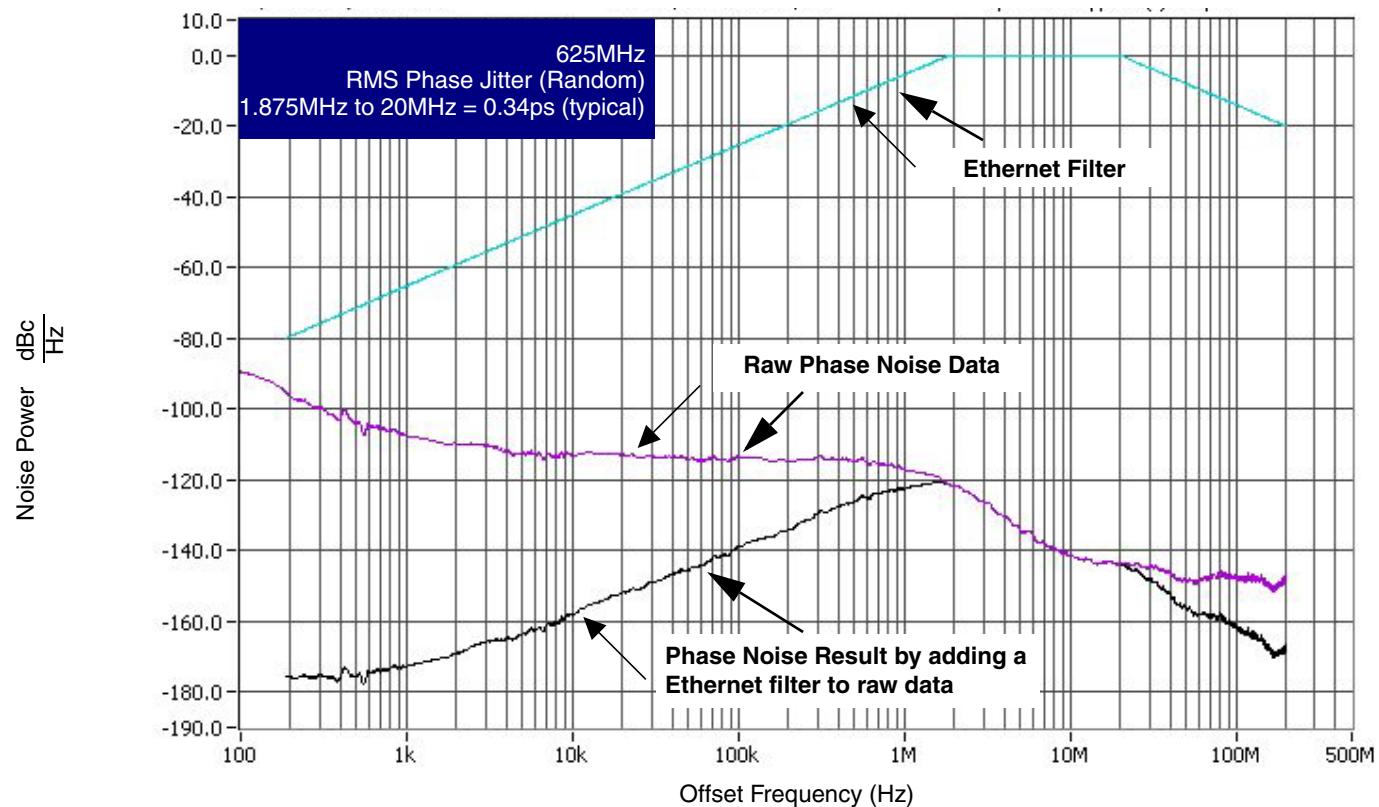
| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------------------------|----------------------------------|--|---------|---------|---------|-------|
| fout | Output Frequency | FREQ_SEL = 0 | 116 | | 150 | MHz |
| | | FREQ_SEL = 1 | 580 | | 750 | MHz |
| t _{jit} (\emptyset) | RMS Phase Jitter, Random; NOTE 1 | 125MHz, (Integration Range: 1.875MHz – 20MHz) | | 0.44 | | ps |
| | | 625MHz, (Integration Range: 1.875MHz – 20MHz) | | 0.33 | | ps |
| t _R / t _F | Output Rise/Fall Time | 20% to 80% | 100 | | 600 | ps |
| odc | Output Duty Cycle | | 45 | | 55 | % |

NOTE 1: Refer to Phase Noise Plots.

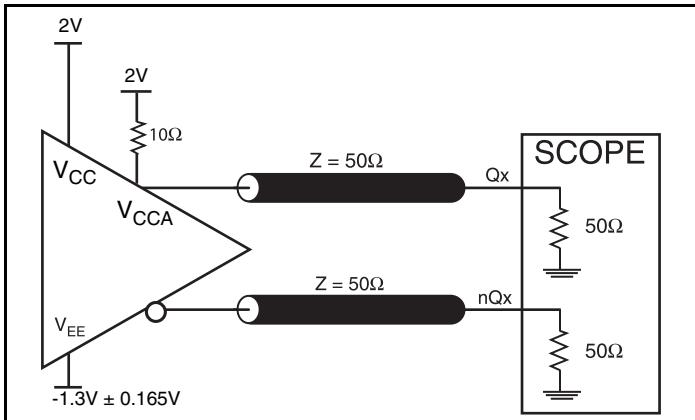
Typical Phase Noise at 125MHz @ 3.3V



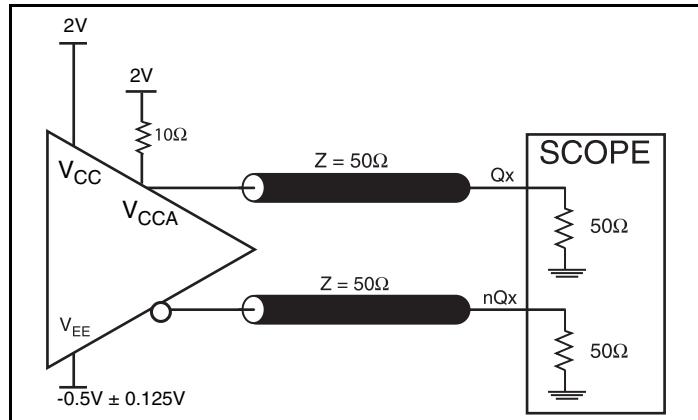
Typical Phase Noise at 625MHz @ 3.3V



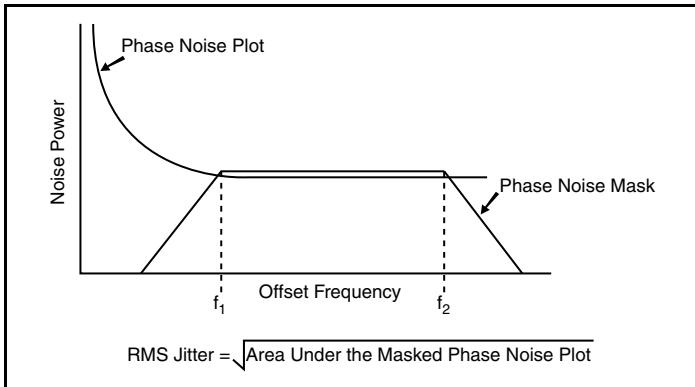
Parameter Measurement Information



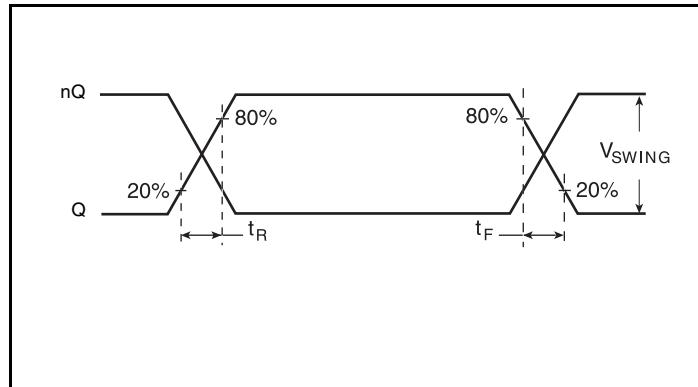
3.3V LVPECL Output Load AC Test Circuit



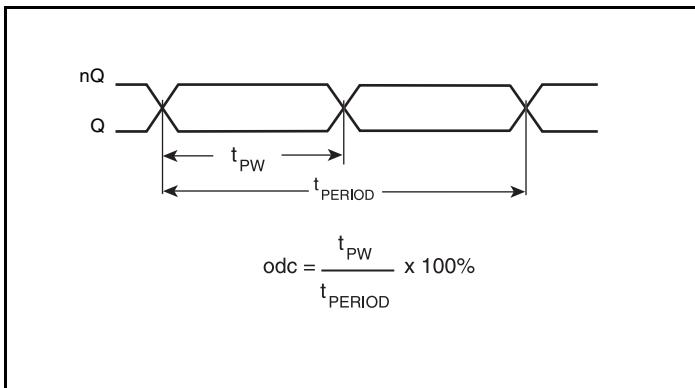
2.5V LVPECL Output Load AC Test Circuit



RMS Phase Jitter



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 843251I-15 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC} and V_{CCA} should be individually connected to the power supply plane through vias, and $0.01\mu F$ bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional 10Ω resistor along with a $10\mu F$ bypass capacitor be connected to the V_{CCA} pin.

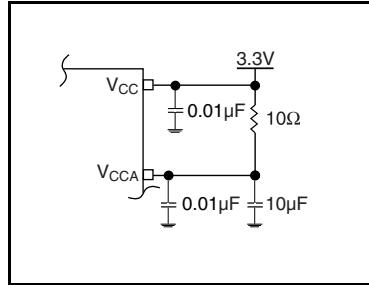


Figure 1. Power Supply Filtering

Crystal Input Interface

The 843251I-15 has been characterized with 18pF parallel resonant crystals. The capacitor values, C_1 and C_2 , shown in *Figure 2* below were determined using a 25MHz , 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C_1 and C_2 values can be slightly adjusted for different board layouts.

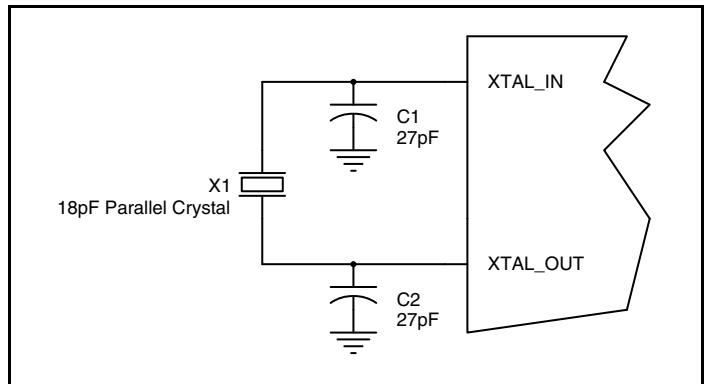


Figure 2. Crystal Input Interface

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVCMS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 3A* shows an example of the interface diagram for a high speed 3.3V LVCMS driver. This configuration requires that the sum of the output impedance of the driver (Z_o) and the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two

ways. First, R_1 and R_2 in parallel should equal the transmission line impedance. For most 50Ω applications, R_1 and R_2 can be 100Ω . This can also be accomplished by removing R_1 and changing R_2 to 50Ω . The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMS driver. *Figure 3B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

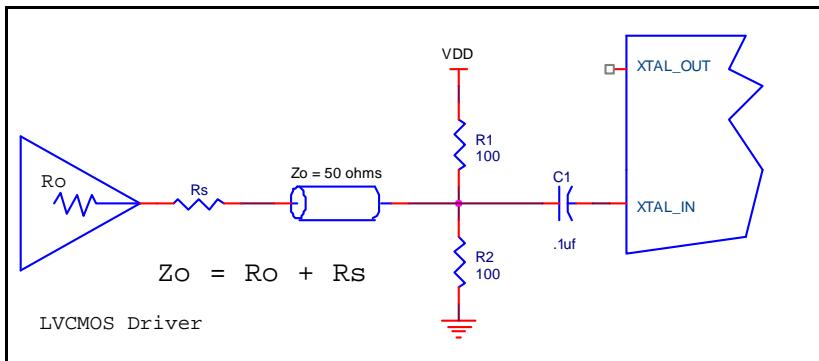


Figure 3A. General Diagram for LVCMS Driver to XTAL Input Interface

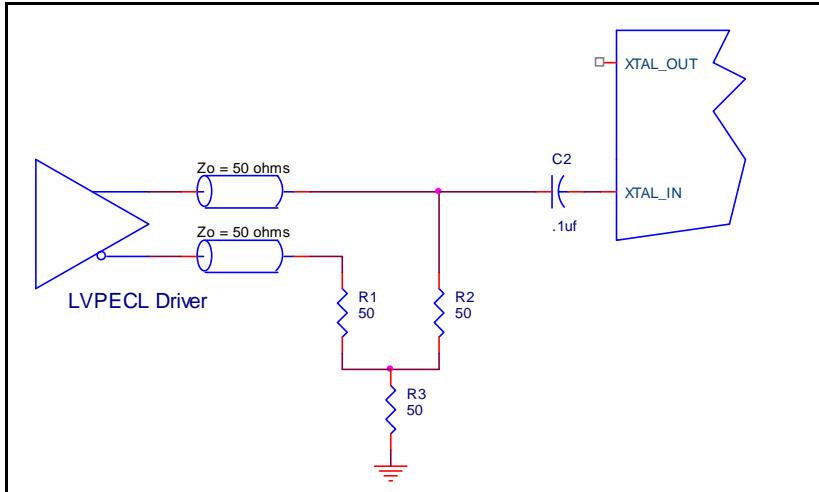


Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

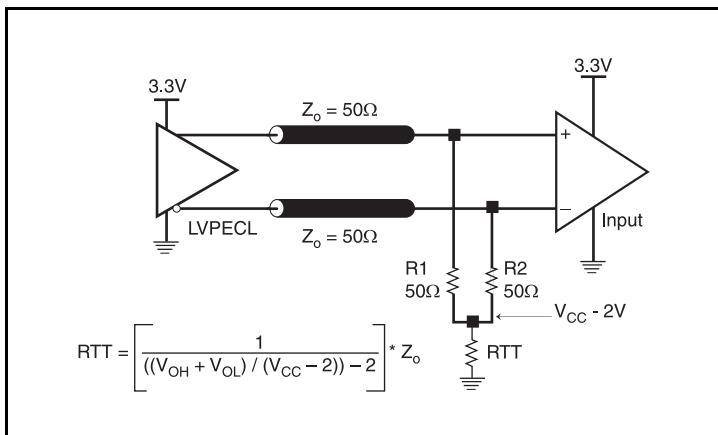


Figure 4A. 3.3V LVPECL Output Termination

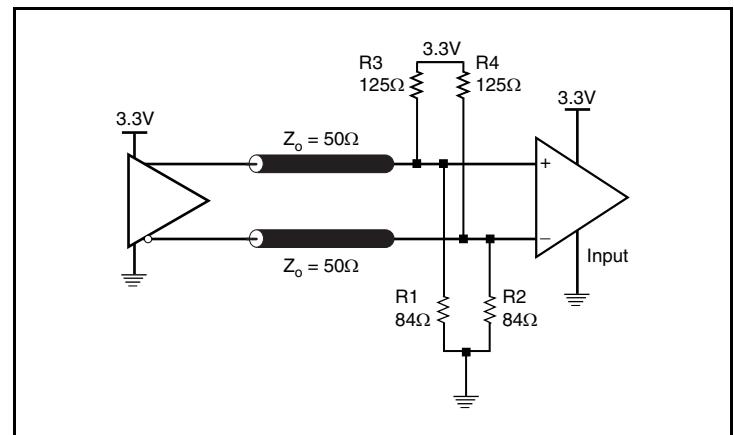


Figure 4B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 5A and Figure 5B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{CC} - 2V$. For $V_{CC} = 2.5V$, the $V_{CC} - 2V$ is very close to

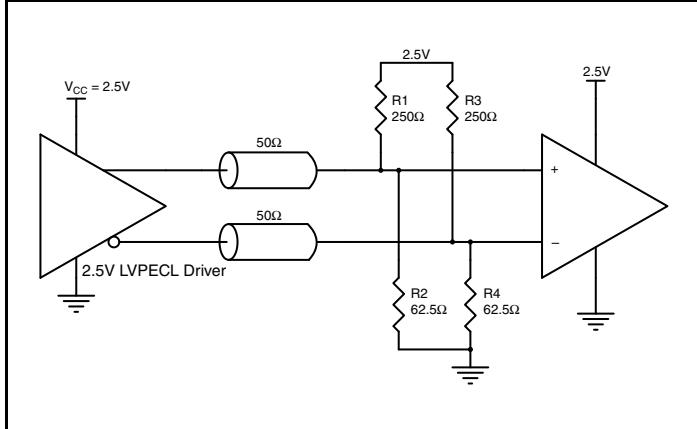


Figure 5A. 2.5V LVPECL Driver Termination Example

ground level. The R3 in Figure 5B can be eliminated and the termination is shown in Figure 5C.

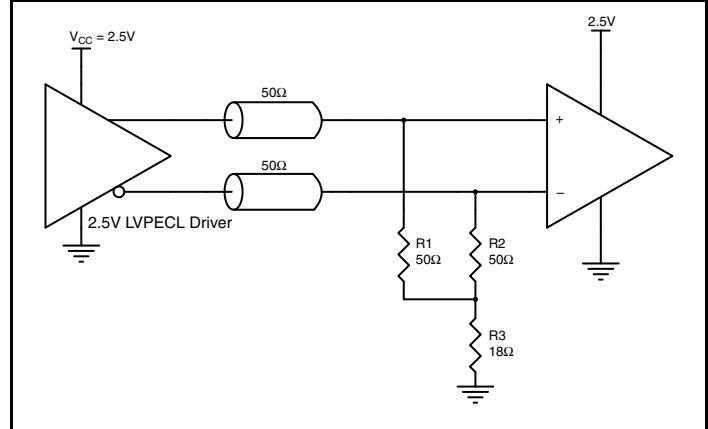


Figure 5B. 2.5V LVPECL Driver Termination Example

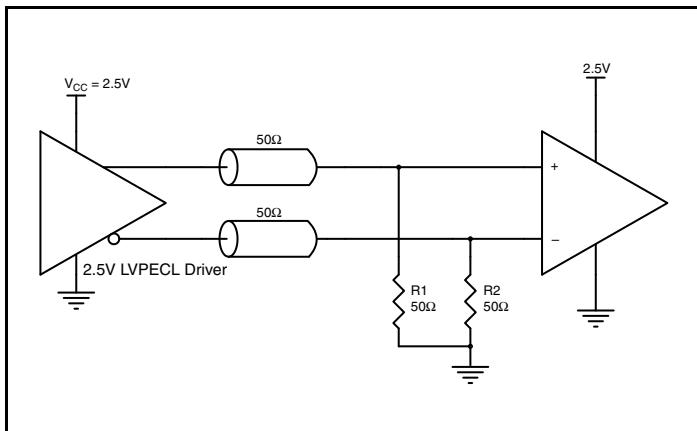


Figure 5C. 2.5V LVPECL Driver Termination Example

Schematic Example

Figure 6 shows an example of 843251I-15 application schematic. In this example, the device is operated at $V_{CC} = 3.3V$. The 18pF parallel resonant 25MHz crystal is used. The $C1 = 27pF$ and $C2 = 27pF$ are recommended for frequency accuracy. For different board layout, the $C1$ and $C2$ may be slightly adjusted for optimizing

frequency accuracy. Two examples of LVPECL termination are shown in this schematic. Additional termination approaches are shown in the *LVPECL Termination Application Note*.

Note: Thermal pad (E-pad) must be connected to ground (V_{EE}).

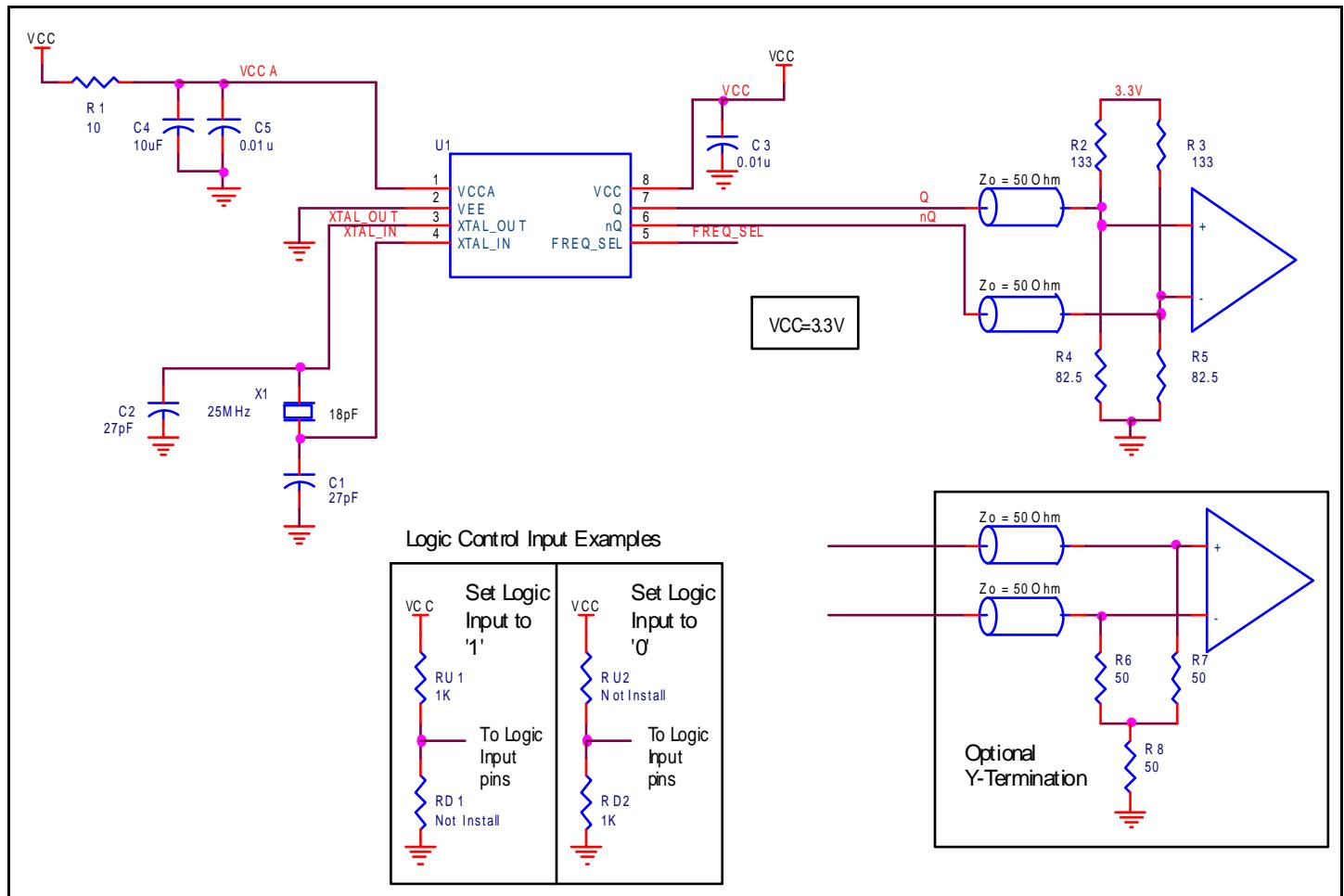


Figure 6. 843251I-15 Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 843251I-15. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 843251I-15 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.465V * 83mA = 287.60\text{mW}$
- Power (outputs)_{MAX} = **30mW/Loaded Output pair**

Total Power_{MAX} (3.3V, with all outputs switching) = $287.60\text{mW} + 30\text{mW} = 317.60\text{mW}$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * P_{d_total} + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

P_{d_total} = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 125.5°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$85^\circ\text{C} + 0.318\text{W} * 125.5^\circ\text{C/W} = 124.9^\circ\text{C}$. This is below the limit of 125°C.

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 8 Lead TSSOP, Forced Convection

| θ_{JA} vs. Air Flow | | | |
|---|-----------|-----------|-----------|
| Meters per Second | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 129.5°C/W | 125.5°C/W | 123.5°C/W |

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 7*.

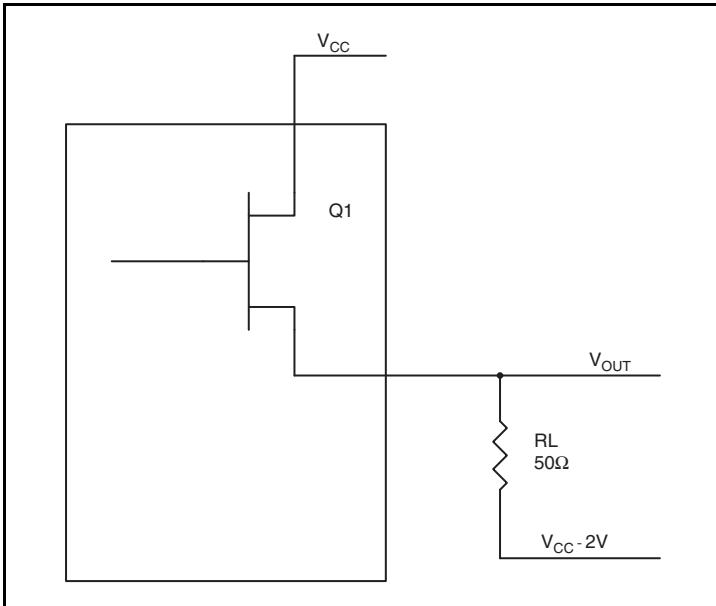


Figure 7. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CC_MAX} - 0.9V$
 $(V_{CC_MAX} - V_{OH_MAX}) = 0.9V$
- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CC_MAX} - 1.7V$
 $(V_{CC_MAX} - V_{OL_MAX}) = 1.7V$

P_{d_H} is power dissipation when the output drives high.

P_{d_L} is the power dissipation when the output drives low.

$$P_{d_H} = [(V_{OH_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - (V_{CC_MAX} - V_{OH_MAX}))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$P_{d_L} = [(V_{OL_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - (V_{CC_MAX} - V_{OL_MAX}))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

Total Power Dissipation per output pair = $P_{d_H} + P_{d_L} = 30mW$

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 8 Lead TSSOP

| θ_{JA} vs. Air Flow | | | |
|---|-----------|-----------|-----------|
| Meters per Second | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 129.5°C/W | 125.5°C/W | 123.5°C/W |

Transistor Count

The transistor count for 843251I-15 is: 2395

Package Outline and Package Dimensions

Package Outline - G Suffix for 8 Lead TSSOP

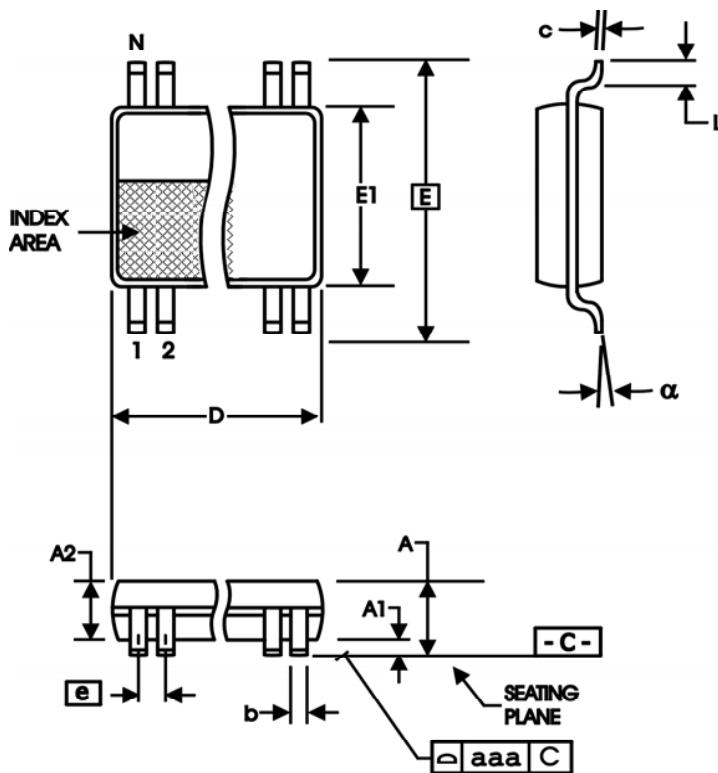


Table 8. Package Dimensions

| All Dimensions in Millimeters | | |
|-------------------------------|------------|-----------|
| Symbol | Minimum | Maximum |
| N | 8 | |
| A | | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 2.90 | 3.10 |
| E | 6.40 Basic | |
| E1 | 4.30 | 4.50 |
| e | 0.65 Basic | |
| L | 0.45 | 0.75 |
| α | 0° | 8° |
| aaa | | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|---------|-------------------------|--------------------|---------------|
| 843251BGI-15LF | BI15L | 8 Lead TSSOP, Lead-Free | Tube | -40°C to 85°C |
| 843251BGI-15LFT | BI15L | 8 Lead TSSOP, Lead-Free | Tape & Reel | -40°C to 85°C |

Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|-----|-------|------|--|----------|
| A | T4 | 1 | Deleted HiPerClockS references. | 11/2/12 |
| | | 3 | Crystal Characteristics Table - added note. | |
| | | 7 | Deleted application note, <i>LVCMOS to XTAL Interface</i> . | |
| | T9 | 10 | Added Note: Thermal pad (E-pad) must be connected to ground (VEE). | |
| | | 14 | Deleted quantity from tape and reel. | |
| B | T9 | 9 | Updated header/footer throughout the datasheet. | 10/29/15 |
| | | 10 | Deleted <i>IDT</i> prefix from part number. | |
| | | 11 | Application Information: added <i>Overdriving the XTAL Interface</i> , | |
| | | 18 | updated <i>Termination for 3.3V LVPECL Outputs</i> Ordering Information Table - deleted: leaded part rows and table note. | |

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