

FEMTOCLOCK™ CRYSTAL-TO-3.3V LVPECL FREQUENCY SYNTHESIZER

ICS843204I

GENERAL DESCRIPTION

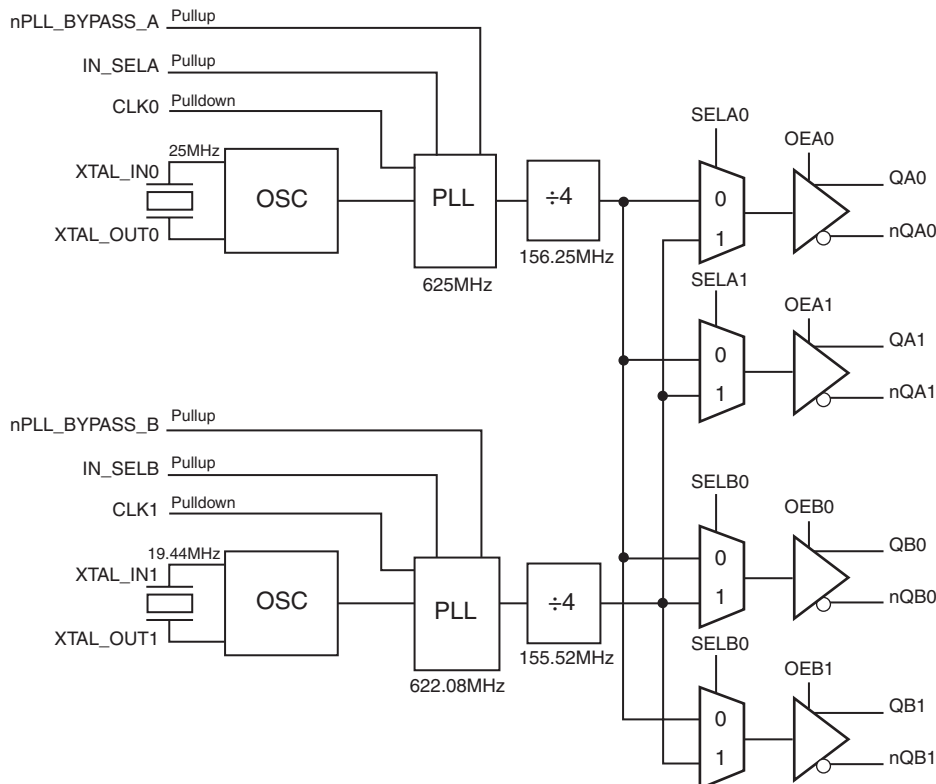


The ICS843204I is a 4 output LVPECL Synthesizer optimized to generate Gigabit Ethernet and SONET reference clock frequencies and is a member of the HiPerClocks™ family of high performance clock solutions from IDT. Using a 19.44MHz and 25MHz, 18pF parallel resonant crystal, 155.52MHz and 156.25MHz frequencies can be generated. The ICS843204I uses IDT's FemtoClock™ low phase noise VCO technology and can achieve 1ps or lower typical RMS phase jitter. The ICS843204I is packaged in a 48-pin TSSOP package.

FEATURES

- Four 3.3V LVPECL outputs
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- Supports the following output frequencies: 155.52MHz and 156.25MHz
- VCO range: 560MHz - 680MHz
- RMS phase jitter @ 155.52MHz, using a 19.44MHz crystal (12kHz - 20MHz): 0.98ps (typical)
- RMS phase jitter @ 156.25MHz, using a 19.44MHz crystal (1.875MHz - 20MHz): 0.52ps (typical)
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

BLOCK DIAGRAM



PIN ASSIGNMENT

| | | | |
|---------------|----|----|-----------|
| nQA1 | 1 | 48 | IN_SEL_A |
| QA1 | 2 | 47 | CLK0 |
| nQA0 | 3 | 46 | XTAL_IN0 |
| QA0 | 4 | 45 | XTAL_OUT0 |
| nc | 5 | 44 | nc |
| Vcco_A | 6 | 43 | VEE |
| SELA1 | 7 | 42 | OEA0 |
| SELA0 | 8 | 41 | OEA1 |
| nPLL_BYPASS_A | 9 | 40 | Vcc |
| nc | 10 | 39 | VCCA_A |
| nc | 11 | 38 | nc |
| nc | 12 | 37 | nc |
| nc | 13 | 36 | SELB0 |
| XTAL_IN1 | 14 | 35 | VEE |
| XTAL_OUT1 | 15 | 34 | OEB0 |
| CLK1 | 16 | 33 | OEB1 |
| IN_SEL_B | 17 | 32 | Vcc |
| nPLL_BYPASS_B | 18 | 31 | SELB1 |
| Vcco_B | 19 | 30 | VCCA_B |
| nc | 20 | 29 | nc |
| QB0 | 21 | 28 | nc |
| nQB0 | 22 | 27 | nc |
| QB1 | 23 | 26 | nc |
| nQB1 | 24 | 25 | nc |

ICS843204I

48 Lead TSSOP

6.1mm x 12.5mm x 0.925mm
package body

G Package

Top View

TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | | Description |
|--|------------------------|--------|----------|---|
| 1, 2 | nQA1, QA1 | Output | | Differential output pair. LVPECL interface levels. |
| 3, 4 | nQA0, QA0 | Output | | Differential output pair. LVPECL interface levels. |
| 5, 10, 11, 12, 13, 20, 25, 26, 27, 28, 29, 37, 38, 44 | nc | Unused | | No connect. |
| 6 | V _{CCO_A} | Power | | Output supply pin for Bank A outputs. |
| 7 | SELA1 | Input | Pulldown | Select pin. When HIGH, selects QA1/nQA1 at 155.52MHz. When LOW, selects QA1/nQA1 at 156.25MHz. LVCMOS/LVTTL interface levels. |
| 8 | SELA0 | Input | Pulldown | Select pin. When HIGH, selects QA0/nQA0 at 155.52MHz. When LOW, selects QA1/nQA1 at 156.25MHz. LVCMOS/LVTTL interface levels. |
| 9 | nPLL_BYPASS_A | Input | Pullup | When LOW, PLL is bypassed. When HIGH, PLL output is active. LVCMOS/LVTTL interface levels. |
| 14, 15 | XTAL_IN1, XTAL_OUT1 | Input | | Parallel resonant crystal interface. XTAL_OUT1 is the output, XTAL_IN1 is the input. |
| 16, 47 | CLK1, CLK0 | Input | Pulldown | LVCMOS/LVTTL clock inputs. |
| 21, 22 | QB0, nQB0 | Output | | Differential output pair. LVPECL interface levels. |
| 17 | IN_SEL_B | Input | Pullup | Select pin. When HIGH, selects XTAL1 inputs. When LOW, selects CLK1 input. LVCMOS/LVTTL interface levels. |
| 18 | nPLL_BYPASS_B | Input | Pullup | When LOW, PLL is bypassed. When HIGH, PLL output is active. LVCMOS/LVTTL interface levels. |
| 19 | V _{CCO_B} | Power | | Output supply pin for Bank B outputs. |
| 23, 24 | QB1, nQB1 | Output | | Differential output pair. LVPECL interface levels. |
| 31 | SELB1 | Input | Pullup | Select pin. When HIGH, selects QB1/nQB1 at 155.52MHz. When LOW, selects QB1/nQB1 at 156.25MHz. LVCMOS/LVTTL interface levels. |
| 30 | V _{CCA_B} | Power | | Analog supply pin for Bank B outputs. |
| 32, 40 | V _{CC} | Power | | Core supply pins. |
| 33 | OEB1 | Input | Pullup | Output enable pin. When HIGH, QB1/nQB1 outputs are enable. LVCMOS/LVTTL interface levels. |
| 34 | OEB0 | Input | Pullup | Output enable pin. When HIGH, QB0/nQB0 outputs are enabled. LVCMOS/LVTTL interface levels. |
| 35, 43 | V _{EE} | Power | | Negative supply pins. |
| 36 | SELB0 | Input | Pullup | Select pin. When HIGH, selects QB0/nQB0 at 155.52MHz. When LOW, selects QB0/nQB0 at 156.25MHz. LVCMOS/LVTTL interface levels. |
| 39 | V _{CCA_A} | Power | | Analog supply pin for Bank A outputs. |
| 41 | OEA1 | Input | Pullup | Output enable pin. When HIGH, QA1/nQA1 outputs are enabled. LVCMOS/LVTTL interface levels. |
| 42 | OEA0 | Input | Pullup | Output enable pin. When HIGH, QA0/nQA0 outputs are enabled. LVCMOS/LVTTL interface levels. |
| 45, 46 | XTAL_OUT0, XTAL_IN0 | Input | | Parallel resonant crystal interface. XTAL_OUT0 is the output, XTAL_IN0 is the input. |
| 48 | IN_SEL_A | Input | Pullup | Select pin. When HIGH, selects XTAL0 inputs. When LOW, selects CLK0 input. LVCMOS/LVTTL interface levels. |

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | 4 | | pF |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 51 | | kΩ |
| R _{PULLUP} | Input Pullup Resistor | | | 51 | | kΩ |

ABSOLUTE MAXIMUM RATINGS

| | |
|--|--------------------------|
| Supply Voltage, V_{CC} | 4.6V |
| Inputs, V_I | -0.5V to $V_{CC} + 0.5V$ |
| Outputs, I_O | |
| Continuous Current | 50mA |
| Surge Current | 100mA |
| Package Thermal Impedance, θ_{JA} | 54.8°C/W (0 mps) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCO_A} = V_{CCO_B} = 3.3V \pm 10\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---------------------------|-----------------------|-----------------|-----------------|---------|----------|-------|
| V_{CC} | Core Supply Voltage | | 2.97 | 3.3 | 3.63 | V |
| $V_{CCA_A} + V_{CCA_B}$ | Analog Supply Voltage | | $V_{CC} - 0.22$ | 3.3 | V_{CC} | V |
| V_{CCO_A}, V_{CCO_B} | Output Supply Voltage | | 2.97 | 3.3 | 3.63 | V |
| I_{EE} | Power Supply Current | | | | 170 | mA |
| I_{CC} | Core Supply Current | | | | 125 | mA |
| $I_{CCA_A} + I_{CCA_B}$ | Analog Supply Current | | | | 22 | mA |
| $I_{CCO_A} + I_{CCO_B}$ | Output Supply Current | | | | 23 | mA |

TABLE 3B. LVCMOS / LVTTTL DC CHARACTERISTICS, $V_{CC} = V_{CCO_A} = V_{CCO_B} = 3.3V \pm 10\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|--------------------|---|---------|---------|----------------|---------|
| V_{IH} | Input High Voltage | | 2 | | $V_{CC} + 0.3$ | V |
| V_{IL} | Input Low Voltage | | -0.3 | | 0.8 | V |
| I_{IH} | Input High Current | CLK0, CLK1, SELA0, SELA1 $V_{CC} = V_{IN} = 3.63V$ | | | 150 | μA |
| | | nPLL_BYPASS_A, nPLL_BYPASS_B, IN_SEL_A, IN_SEL_B, SELB1, SELB0, OEB0, OEB1, OEA0, OEA1 $V_{CC} = V_{IN} = 3.63V$ | | | 5 | μA |
| I_{IL} | Input Low Current | CLK0, CLK1, SELA0, SELA1 $V_{CC} = 3.63V, V_{IN} = 0V$ | -5 | | | μA |
| | | nPLL_BYPASS_A, nPLL_BYPASS_B, IN_SEL_A, IN_SEL_B, SELB1, SELB0, OEB0, OEB1, OEA0, OEA1 $V_{CC} = 3.63V, V_{IN} = 0V$ | -150 | | | μA |

TABLE 3C. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCO_A} = V_{CCO_B} = 3.3V \pm 10\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|-----------------------------------|-----------------|-----------------|---------|-----------------|-------|
| V_{OH} | Output High Voltage; NOTE 1 | | $V_{CCO} - 1.4$ | | $V_{CCO} - 0.9$ | V |
| V_{OL} | Output Low Voltage; NOTE 1 | | $V_{CCO} - 2.0$ | | $V_{CCO} - 1.7$ | V |
| V_{SWING} | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{CCO} - 2V$.**TABLE 4. CRYSTAL CHARACTERISTICS**

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | 19.44 | | 25 | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 5. AC CHARACTERISTICS, $V_{CC} = V_{CCO_A} = V_{CCO_B} = 3.3V \pm 10\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------------|-----------------------------------|-------------------------------|---------|---------|---------|-------|
| f_{OUT} | Output Frequency | SELB0 = 1; OEB0 = 1 | | 155.52 | | MHz |
| | | SELA0 = 0; OEA0 = 1 | | 156.25 | | MHz |
| $t_{sk}(b)$ | Bank Skew; NOTE 1, 2 | | | | 50 | ps |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter (Random); NOTE 3 | 155.52MHz, (12kHz - 20MHz) | | 0.98 | | ps |
| | | 156.25MHz, (1.875MHz - 20MHz) | | 0.52 | | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 250 | | 600 | ps |
| odc | Output Duty Cycle | | 47 | | 53 | % |

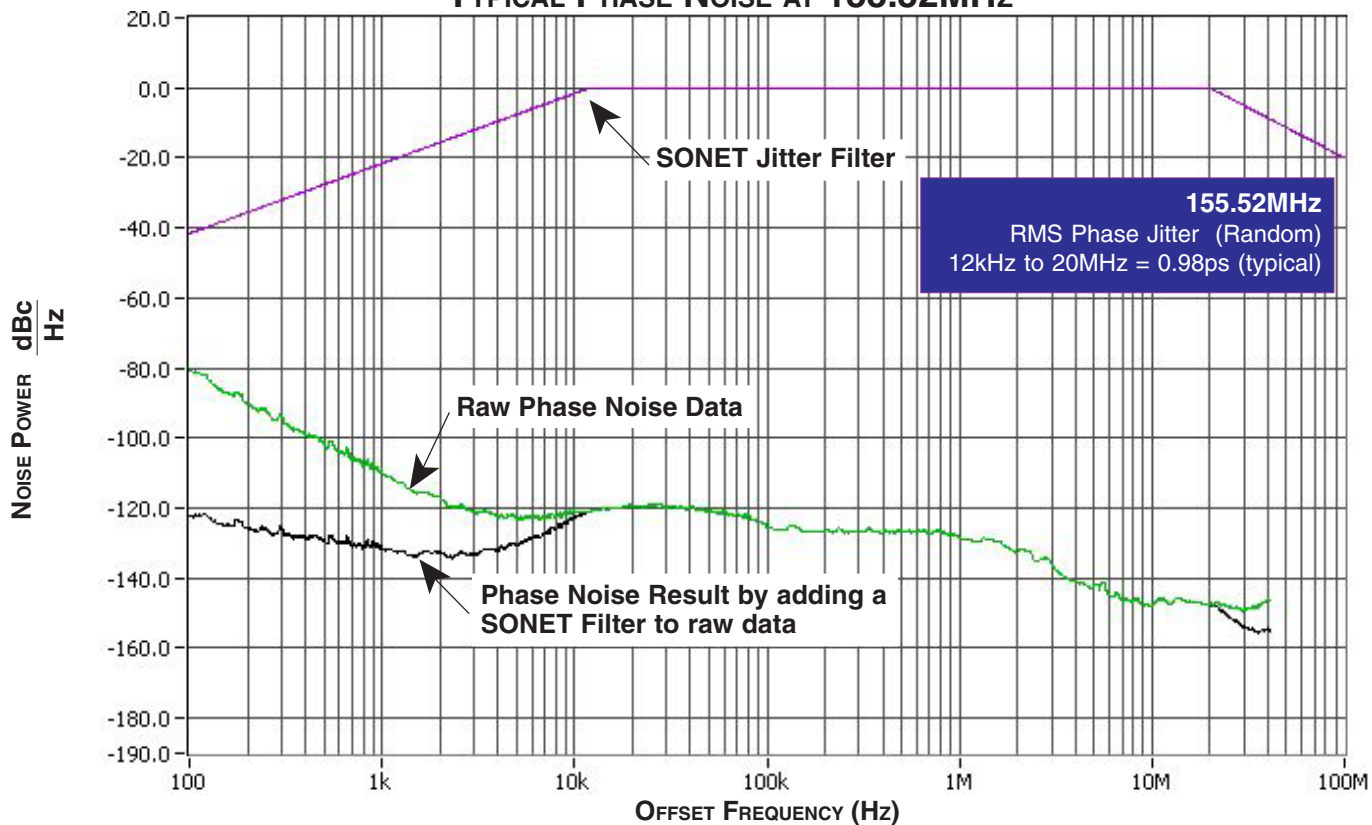
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.

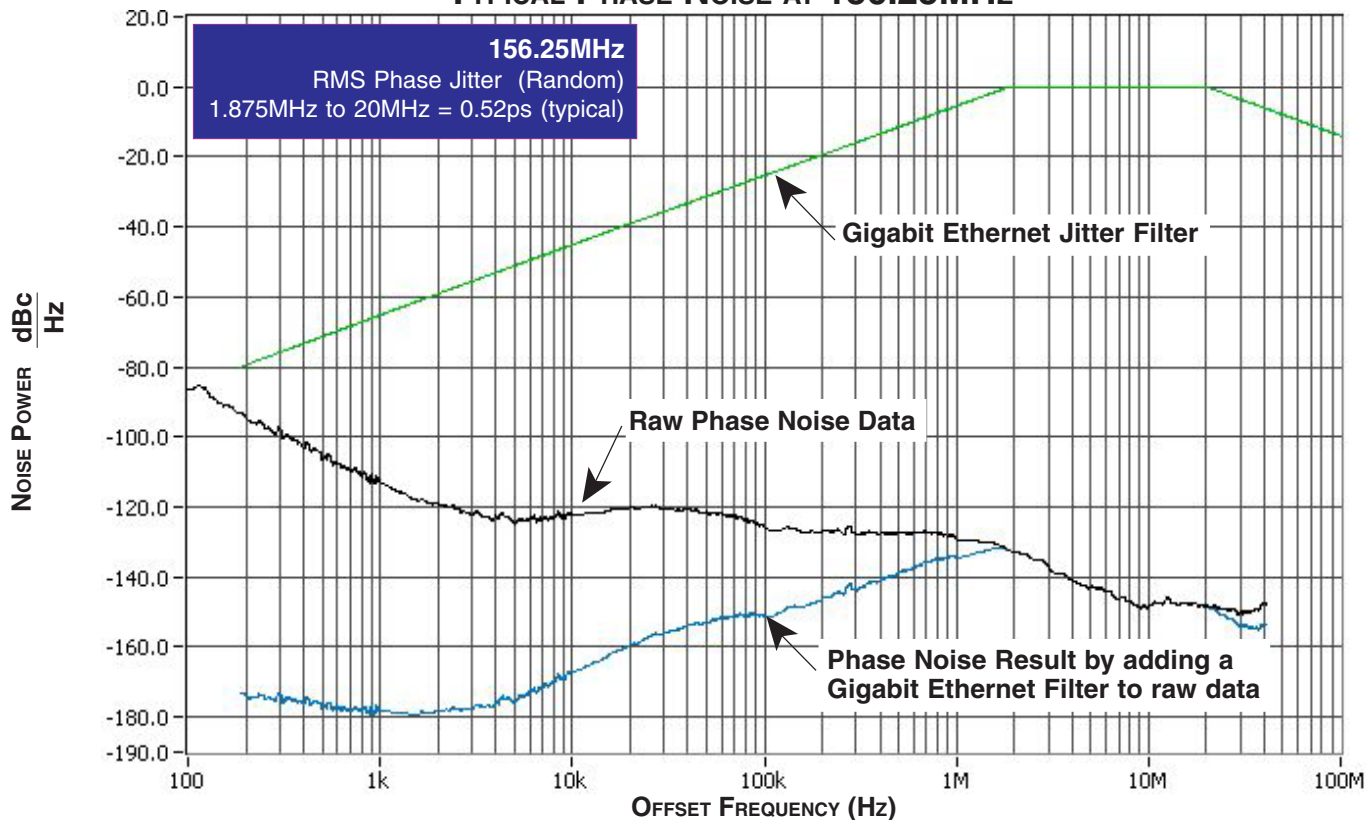
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: See Phase Noise plot.

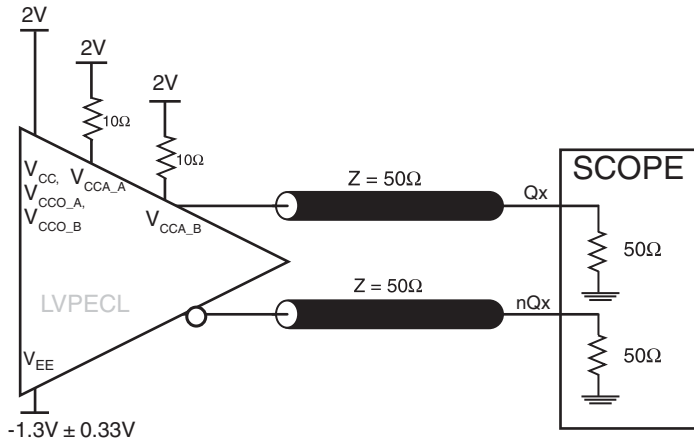
TYPICAL PHASE NOISE AT 155.52MHz



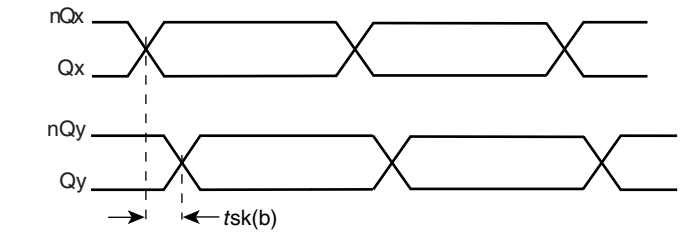
TYPICAL PHASE NOISE AT 156.25MHz



PARAMETER MEASUREMENT INFORMATION

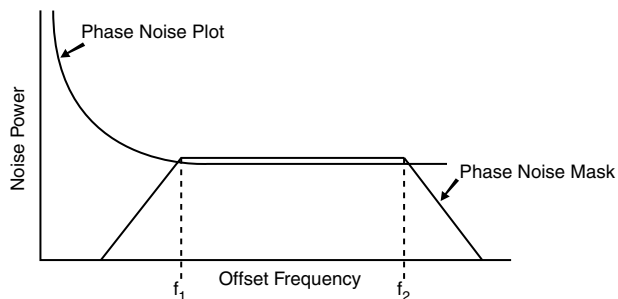


3.3V Core/3.3V Output Load AC Test Circuit



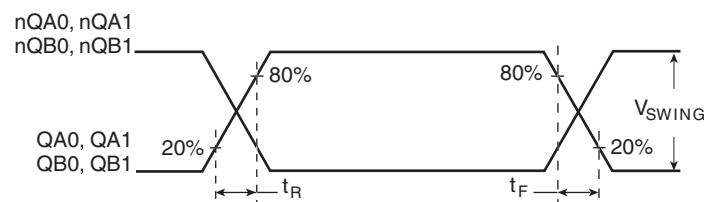
Where X = A or B outputs

BANK SKEW

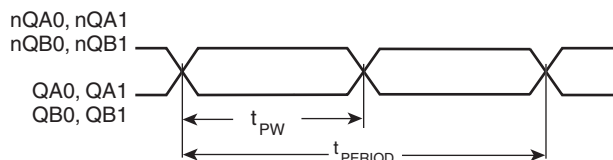


$$\text{RMS Jitter} = \sqrt{\text{Area Under the Masked Phase Noise Plot}}$$

RMS PHASE JITTER



OUTPUT RISE/FALL TIME



$$\text{odc} = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS843204I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC} , V_{CCA_A} , V_{CCA_B} , V_{CCO_A} and V_{CCO_B} should be individually connected to the power supply plane through vias, and $0.01\mu\text{F}$ bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional 10Ω resistor along with a $10\mu\text{F}$ bypass capacitor be connected to the V_{CCA} pin.

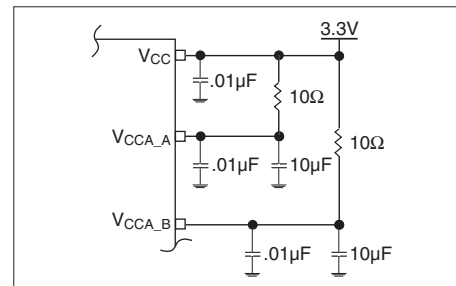


FIGURE 1. POWER SUPPLY FILTERING

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUTS

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a $1\text{k}\Omega$ resistor can be tied from XTAL_IN to ground.

CLK INPUTS

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a $1\text{k}\Omega$ resistor can be tied from the CLK input to ground.

LVC MOS CONTROL PINS

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A $1\text{k}\Omega$ resistor can be used.

OUTPUTS:

LVPECL OUTPUTS

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

CRYSTAL INPUT INTERFACE

The ICS843204I has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below

were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error.

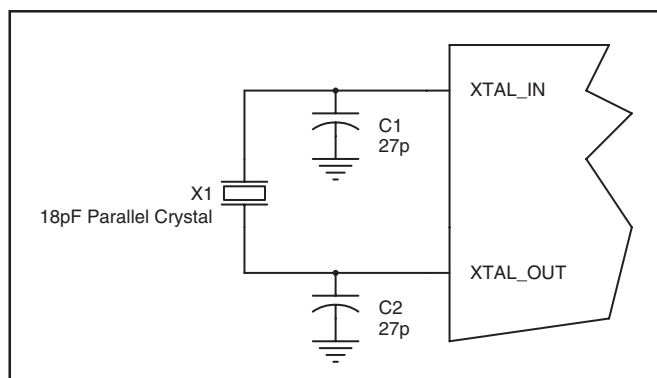


FIGURE 2. CRYSTAL INPUT INTERFACE

LVC MOS TO XTAL INTERFACE

The XTAL_IN input can accept a single-ended LVC MOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3*. The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVC MOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output

impedance of the driver (R_o) plus the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R_1 and R_2 in parallel should equal the transmission line impedance. For most 50Ω applications, R_1 and R_2 can be 100Ω . This can also be accomplished by removing R_1 and making R_2 50Ω .

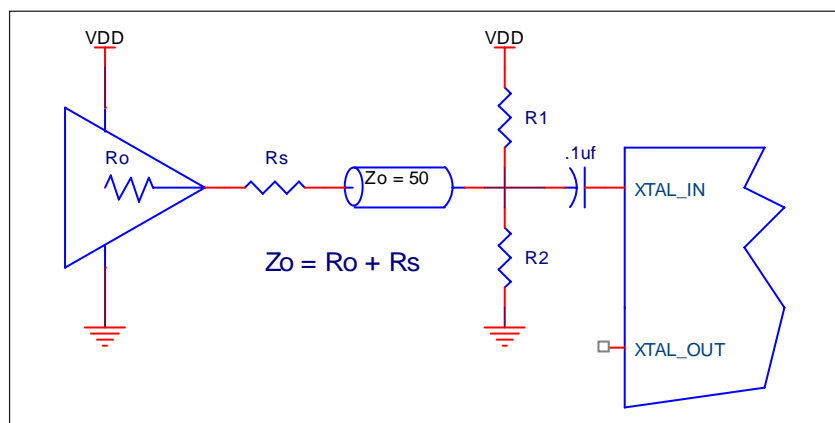


FIGURE 3. GENERAL DIAGRAM FOR LVC MOS DRIVER TO XTAL INPUT INTERFACE

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are

designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

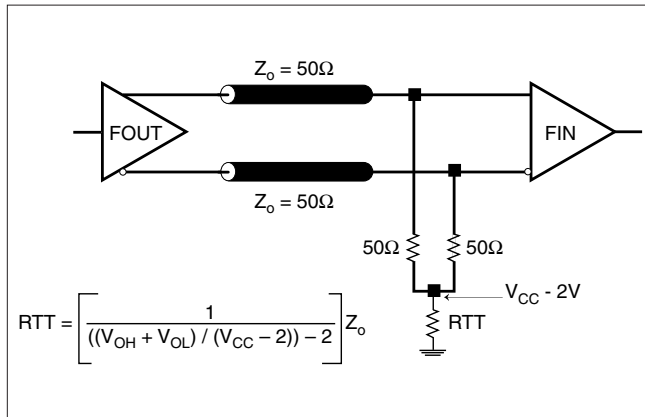


FIGURE 4A. LVPECL OUTPUT TERMINATION

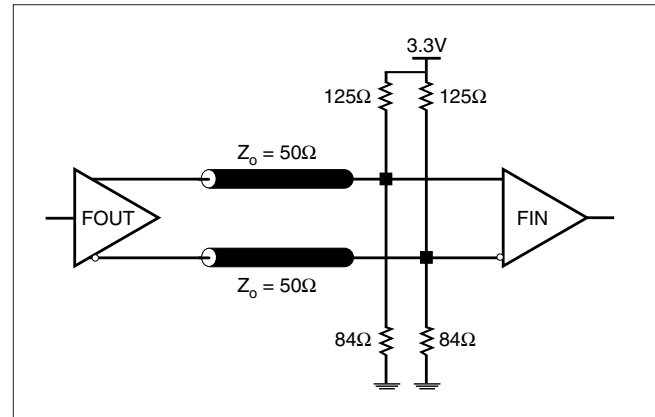


FIGURE 4B. LVPECL OUTPUT TERMINATION

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843204I. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS843204I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.3V + 10\% = 3.63V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.63V * 170mA = 617.10mW$
- Power (outputs)_{MAX} = **30mW/Loaded Output pair**
If all outputs are loaded, the total power is $4 * 30mW = 120mW$

$$\text{Total Power}_{MAX} (3.63V, \text{ with all outputs switching}) = 617.10mW + 120mW = 737.10mW$$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 51°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:
 $85^\circ C + 0.737W * 51^\circ C/W = 122.6^\circ C$. This is below the limit of 125°C.

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 48-PIN TSSOP, FORCED CONVECTION

| θ_{JA} by Velocity (Meters Per Second) | | | |
|---|----------|----------|----------|
| | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 54.8°C/W | 51.0°C/W | 49.1°C/W |

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 5*.

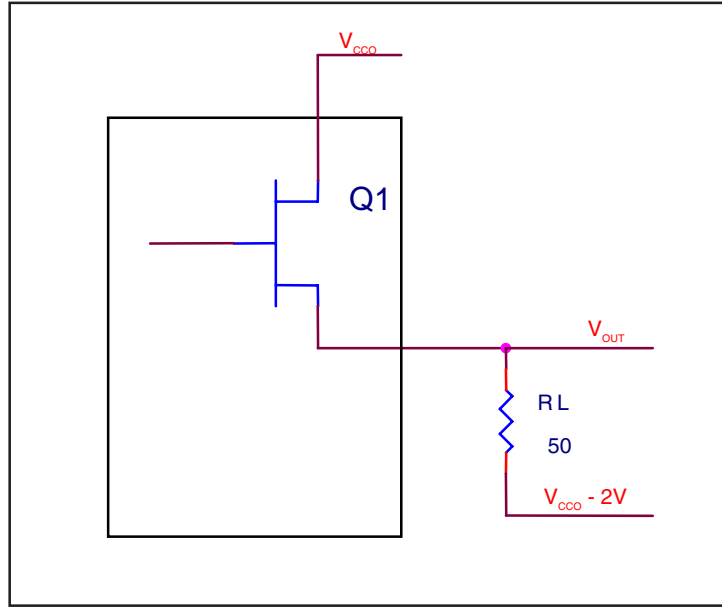


FIGURE 5. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CCO_MAX} - 0.9V$

$$(V_{CCO_MAX} - V_{OH_MAX}) = 0.9V$$

- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CCO_MAX} - 1.7V$

$$(V_{CCO_MAX} - V_{OL_MAX}) = 1.7V$$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - (V_{CCO_MAX} - V_{OH_MAX}))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd_L = [(V_{OL_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - (V_{CCO_MAX} - V_{OL_MAX}))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = 30mW$$

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 48 LEAD TSSOP

| θ_{JA} by Velocity (Meters Per Second) | | | |
|---|----------|----------|----------|
| | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 54.8°C/W | 51.0°C/W | 49.1°C/W |

TRANSISTOR COUNT

The transistor count for ICS843204I is: 4090

PACKAGE OUTLINE - G SUFFIX FOR 48 LEAD TSSOP

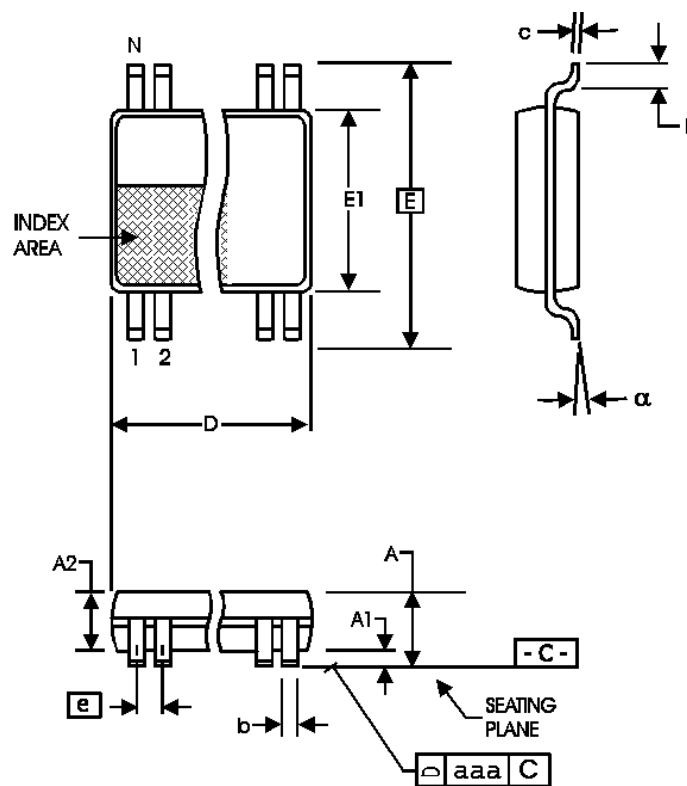


TABLE 8. PACKAGE DIMENSIONS

| SYMBOL | Millimeters | |
|----------|-------------|---------|
| | Minimum | Maximum |
| N | 48 | |
| A | -- | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.17 | 0.27 |
| c | 0.09 | 0.20 |
| D | 12.40 | 12.60 |
| E | 8.10 BASIC | |
| E1 | 6.00 | 6.20 |
| e | 0.50 BASIC | |
| L | 0.45 | 0.75 |
| α | 0° | 8° |
| aaa | -- | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|----------------|---------------------------|--------------------|---------------|
| 843204AGI | ICS843204AGI | 48 Lead TSSOP | tube | -40°C to 85°C |
| 843204AGIT | ICS843204AGI | 48 Lead TSSOP | 1000 tape & reel | -40°C to 85°C |
| 843204AGILF | ICS843204AGILF | 48 Lead "Lead-Free" TSSOP | tube | -40°C to 85°C |
| 843204AGILFT | ICS843204AGILF | 48 Lead "Lead-Free" TSSOP | 1000 tape & reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET

| Rev | Table | Page | Description of Change | Date |
|-----|-------|---------|---|---------|
| A | T9 | 8 14 | Crystal Input Interface, Figure 2, changed Cq/C2 to 27pF. Ordering Information Table - deleted "ICS" prefix from part/order number column. | 3/18/09 |
| | | | | |
| | | | | |

ICS843204I

FEMTOCLOCK™ CRYSTAL-TO-3.3V LVPECL FREQUENCY SYNTHESIZER

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