

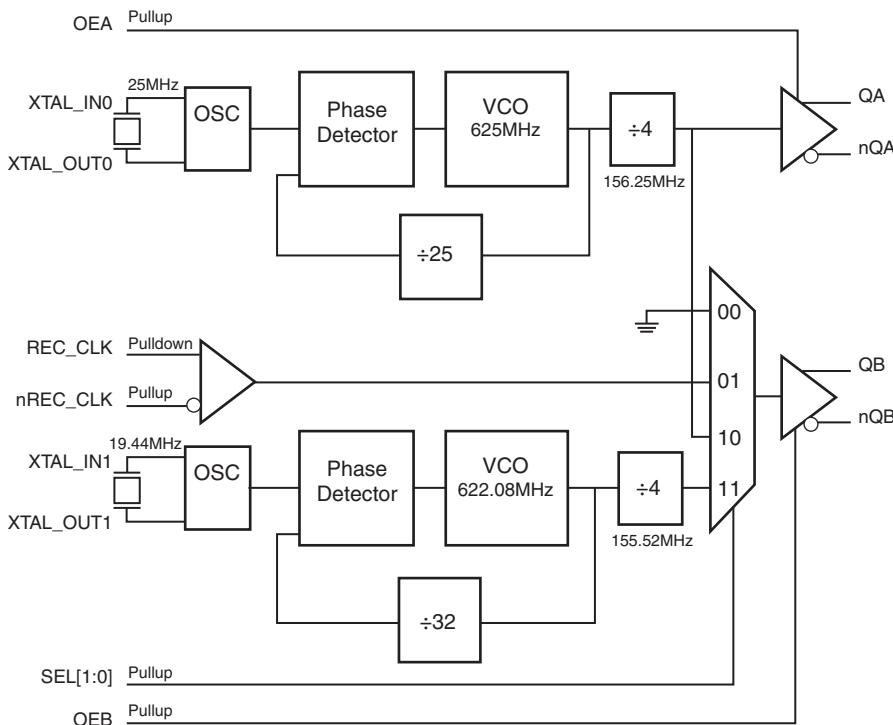
## GENERAL DESCRIPTION

The 843202I is a 2 output LVPECL Synthesizer optimized to generate Gigabit Ethernet and SONET reference clock frequencies and is a member of the family of high performance clock solutions from IDT. Using a 19.44MHz and 25MHz, 18pF parallel resonant crystal, 155.52MHz and 156.25MHz frequencies can be generated. The part also allows the use of a recovered clock at QB output. The 843202I uses IDT's FemtoClock™ low phase noise VCO technology and can achieve 1ps or lower typical RMS phase jitter. The 843202I is packaged in a 32-pin LQFP package.

## SELBx FUNCTION TABLE

| Control Inputs | Outputs                    |
|----------------|----------------------------|
| SEL[1:0]       | nQB, QB                    |
| 00             | High, Low                  |
| 01             | REC_CLK                    |
| 10             | 156.25MHz driven by XTAL_0 |
| 11             | 155.52MHz driven by XTAL_1 |

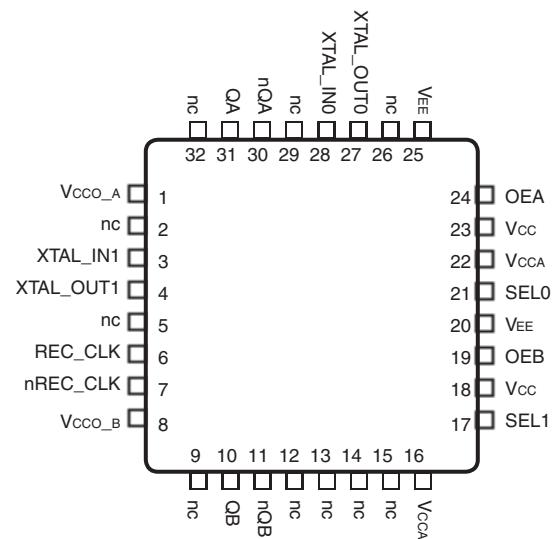
## BLOCK DIAGRAM



## FEATURES

- Two 3.3V LVPECL outputs
- Selectable crystal oscillator interface or one differential recovered clock inputs
- Supports the following output frequencies: 155.52MHz and 156.25MHz
- VCO range: 560MHz - 680MHz
- RMS phase jitter @ 155.52MHz, using a 19.44MHz crystal (12kHz – 1.3MHz): 0.86ps (typical)
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (1.875MHz -- 20MHz): 0.56ps (typical)
- Full 3.3V supply mode
- 40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package
- For functional replacement part use 8T49N242

## PIN ASSIGNMENT



**843202I**  
32-Lead LQFP  
7mm x 7mm x 1.4mm  
package body  
**Y Package**  
Top View

TABLE 1. PIN DESCRIPTIONS

| Number                              | Name                | Type   | Description                                                                          |                                                                             |  |  |  |
|-------------------------------------|---------------------|--------|--------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|--|--|--|
| 1                                   | $V_{CCO\_A}$        | Power  | Output supply pin for Bank A output.                                                 |                                                                             |  |  |  |
| 2, 5, 9, 12, 13, 14, 15, 26, 29, 32 | nc                  | Unused | No connect.                                                                          |                                                                             |  |  |  |
| 3, 4                                | XTAL_IN1, XTAL_OUT1 | Input  | Parallel resonant crystal interface. XTAL_OUT1 is the output, XTAL_IN1 is the input. |                                                                             |  |  |  |
| 6                                   | REC_CLK             | Input  | Pulldown                                                                             | Non-inverting differential recovered clock inputs.                          |  |  |  |
| 7                                   | nREC_CLK            | Input  | Pullup                                                                               | Inverting differential recovered clock inputs.                              |  |  |  |
| 8                                   | $V_{CCO\_B}$        | Power  | Output supply pin for Bank B output.                                                 |                                                                             |  |  |  |
| 10, 11                              | QB, nQB             | Output | Differential output pair. LVPECL interface levels.                                   |                                                                             |  |  |  |
| 16, 22                              | $V_{CCA}$           | Power  | Analog supply pins.                                                                  |                                                                             |  |  |  |
| 17, 21                              | SEL1, SEL0          | Input  | Pullup                                                                               | Select pins. See SELx Function Table. LVCMOS/LVTTL interface levels.        |  |  |  |
| 18, 23                              | $V_{CC}$            | Power  | Core supply pins.                                                                    |                                                                             |  |  |  |
| 19                                  | OEB                 | Input  | Pullup                                                                               | Output enable pin. QB/nQB output is enabled. LVCMOS/LVTTL interface levels. |  |  |  |
| 20, 25                              | $V_{EE}$            | Power  | Negative supply pins.                                                                |                                                                             |  |  |  |
| 24                                  | OEA                 | Input  | Pullup                                                                               | Output enable pin. QA/nQA output is enabled. LVCMOS/LVTTL interface levels. |  |  |  |
| 27, 28                              | XTAL_OUT0, XTAL_IN0 | Input  | Parallel resonant crystal interface. XTAL_OUT0 is the output, XTAL_IN0 is the input. |                                                                             |  |  |  |
| 30, 31                              | nQA, QA             | Output | Differential output pair. LVPECL interface levels.                                   |                                                                             |  |  |  |

NOTE: refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol         | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units      |
|----------------|-------------------------|-----------------|---------|---------|---------|------------|
| $C_{IN}$       | Input Capacitance       |                 |         | 4       |         | pF         |
| $R_{PULLUP}$   | Input Pullup Resistor   |                 |         | 51      |         | k $\Omega$ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor |                 |         | 51      |         | k $\Omega$ |

## ABSOLUTE MAXIMUM RATINGS

|                                          |                          |
|------------------------------------------|--------------------------|
| Supply Voltage, $V_{cc}$                 | 4.6V                     |
| Inputs, $V_i$                            | -0.5V to $V_{cc} + 0.5V$ |
| Outputs, $I_o$                           |                          |
| Continuous Current                       | 50mA                     |
| Surge Current                            | 100mA                    |
| Package Thermal Impedance, $\theta_{JA}$ | 80.8°C/W (0 mps)         |
| Storage Temperature, $T_{STG}$           | -65°C to 150°C           |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS,  $V_{cc} = V_{CCO_A} = V_{CCO_B} = 3.3V \pm 10\%$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$ 

| Symbol                       | Parameter             | Test Conditions | Minimum         | Typical | Maximum  | Units |
|------------------------------|-----------------------|-----------------|-----------------|---------|----------|-------|
| $V_{cc}$                     | Core Supply Voltage   |                 | 2.97            | 3.3     | 3.63     | V     |
| $V_{CCA}$                    | Analog Supply Voltage |                 | $V_{cc} - 0.22$ | 3.3     | $V_{cc}$ | V     |
| $V_{CCO_A}$ ,<br>$V_{CCO_B}$ | Output Supply Voltage |                 | 2.97            | 3.3     | 3.63     | V     |
| $I_{EE}$                     | Power Supply Current  |                 |                 |         | 138      | mA    |
| $I_{CCA}$                    | Analog Supply Current |                 |                 |         | 22       | mA    |

TABLE 3B. LVCMOS / LVTTL DC CHARACTERISTICS,  $V_{cc} = V_{CCO_A} = V_{CCO_B} = 3.3V \pm 10\%$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$ 

| Symbol   | Parameter          | Test Conditions         | Minimum | Typical | Maximum        | Units   |
|----------|--------------------|-------------------------|---------|---------|----------------|---------|
| $V_{IH}$ | Input High Voltage |                         | 2       |         | $V_{cc} + 0.3$ | V       |
| $V_{IL}$ | Input Low Voltage  |                         | -0.3    |         | 0.8            | V       |
| $I_{IH}$ | Input High Current | OEA, OEB,<br>SEL0, SEL1 |         |         | 5              | $\mu A$ |
| $I_{IL}$ | Input Low Current  | OEA, OEB,<br>SEL0, SEL1 | -150    |         |                | $\mu A$ |

TABLE 3C. DIFFERENTIAL DC CHARACTERISTICS,  $V_{cc} = V_{CCO_A} = V_{CCO_B} = 3.3V \pm 10\%$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$ 

| Symbol    | Parameter                            | Test Conditions | Minimum                          | Typical | Maximum         | Units   |
|-----------|--------------------------------------|-----------------|----------------------------------|---------|-----------------|---------|
| $I_{IH}$  | Input High Current                   | REC_CLK         | $V_{cc} = V_{in} = 3.465V$       |         |                 | $\mu A$ |
|           |                                      | nREC_CLK        | $V_{cc} = V_{in} = 3.465V$       |         |                 | $\mu A$ |
| $I_{IL}$  | Input Low Current                    | REC_CLK         | $V_{cc} = 3.63V$ , $V_{in} = 0V$ | -5      |                 | $\mu A$ |
|           |                                      | nREC_CLK        | $V_{cc} = 3.63V$ , $V_{in} = 0V$ | -150    |                 | $\mu A$ |
| $V_{PP}$  | Peak-to-Peak Input Voltage           |                 | 0.15                             |         | 1.3             | V       |
| $V_{CMR}$ | Common Mode Input Voltage;<br>NOTE 1 |                 | $V_{EE} + 0.5$                   |         | $V_{cc} - 0.85$ | V       |

NOTE 1: Common mode voltage is defined as  $V_{IH}$ .

**TABLE 3D. LVPECL DC CHARACTERISTICS,  $V_{cc} = V_{cc_{0,A}} = V_{cc_{0,B}} = 3.3V \pm 10\%$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$** 

| Symbol      | Parameter                         | Test Conditions | Minimum        | Typical | Maximum        | Units |
|-------------|-----------------------------------|-----------------|----------------|---------|----------------|-------|
| $V_{OH}$    | Output High Voltage; NOTE 1       |                 | $V_{cc} - 1.4$ |         | $V_{cc} - 0.9$ | V     |
| $V_{OL}$    | Output Low Voltage; NOTE 1        |                 | $V_{cc} - 2.0$ |         | $V_{cc} - 1.7$ | V     |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing |                 | 0.6            |         | 1.0            | V     |

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{cc_{0,A,B}} - 2V$ .

**TABLE 4. CRYSTAL CHARACTERISTICS**

| Parameter                          | Test Conditions | Minimum | Typical | Maximum | Units    |
|------------------------------------|-----------------|---------|---------|---------|----------|
| Mode of Oscillation                | Fundamental     |         |         |         |          |
| Frequency                          |                 | 19.44   |         | 25      | MHz      |
| Equivalent Series Resistance (ESR) |                 |         |         | 50      | $\Omega$ |
| Shunt Capacitance                  |                 |         |         | 7       | pF       |
| Drive Level                        |                 |         |         | 1       | mW       |

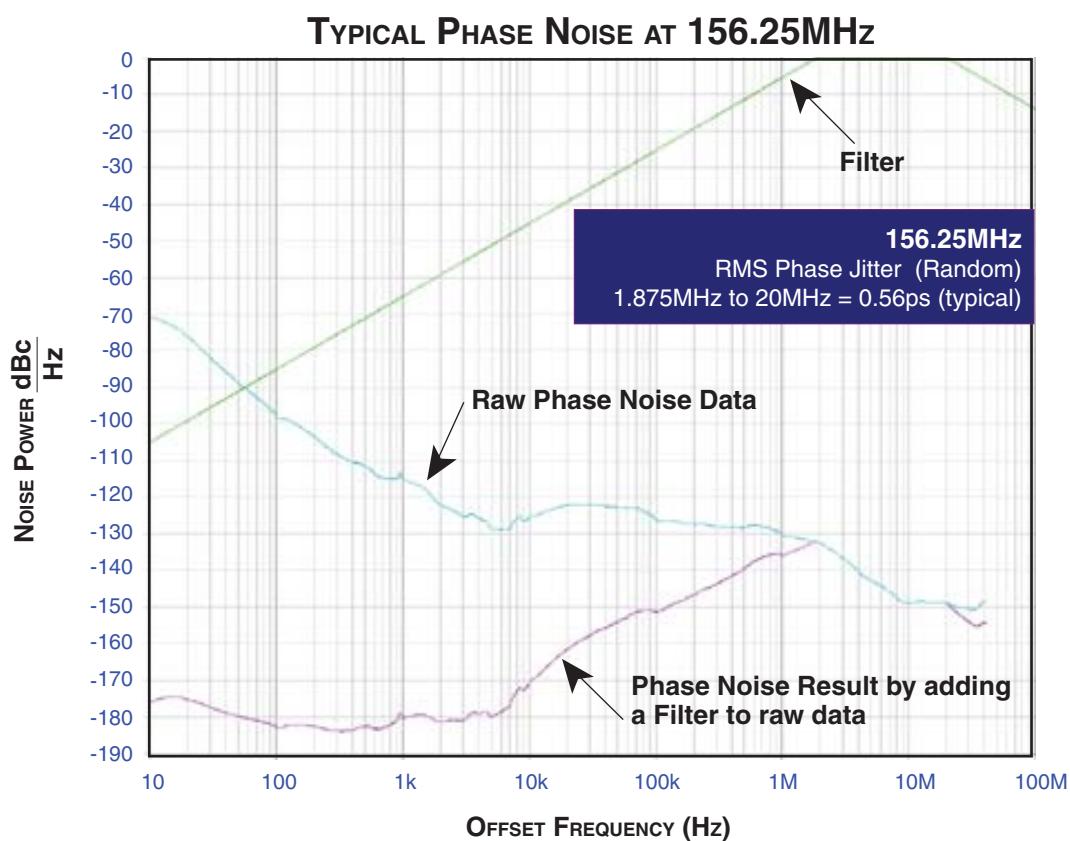
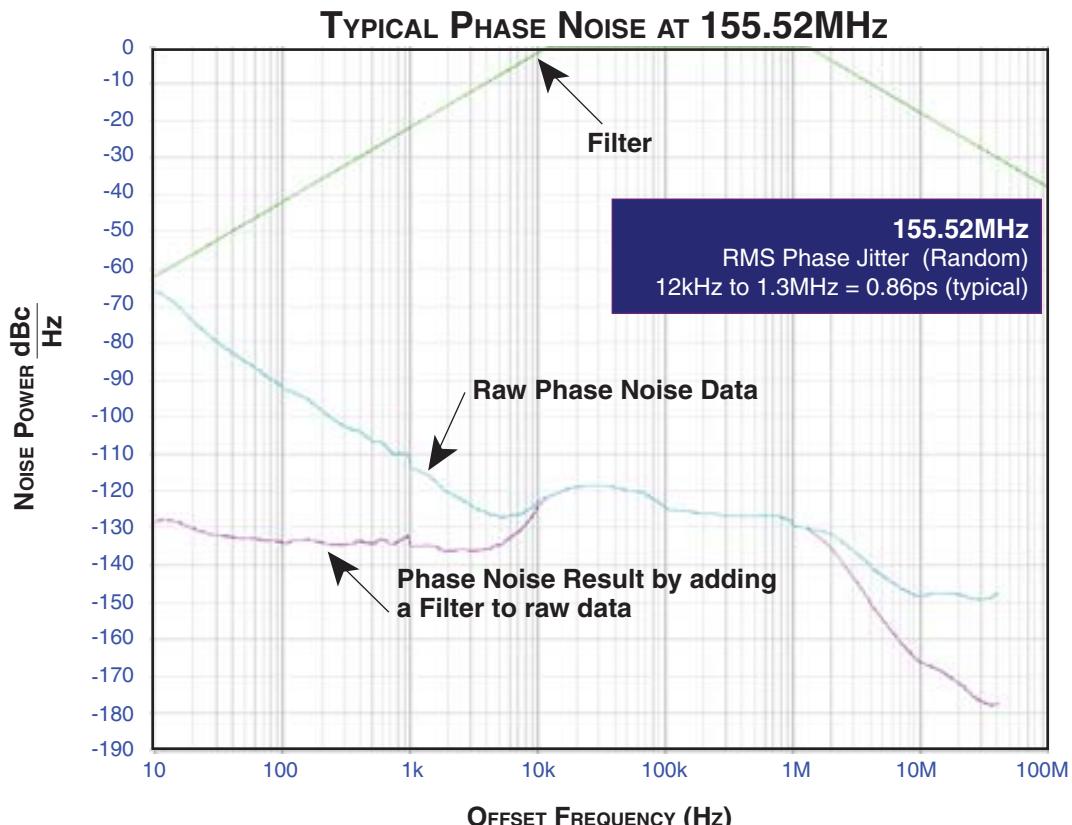
NOTE: Characterized using an 18pF parallel resonant crystal.

**TABLE 5. AC CHARACTERISTICS,  $V_{cc} = V_{cc_{0,A}} = V_{cc_{0,B}} = 3.3V \pm 10\%$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$** 

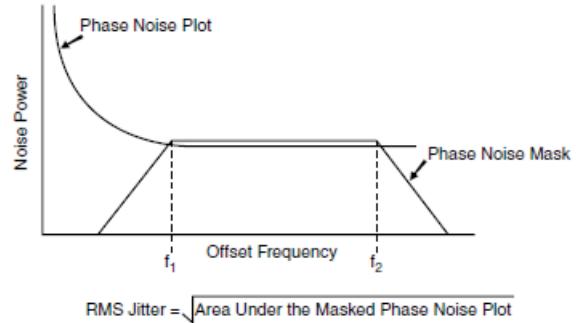
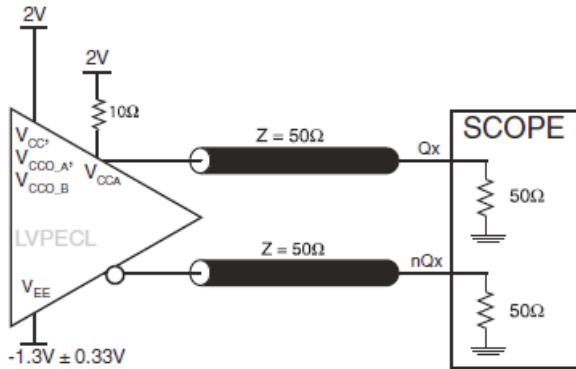
| Symbol                  | Parameter                            | Test Conditions      | Minimum                       | Typical | Maximum | Units |     |
|-------------------------|--------------------------------------|----------------------|-------------------------------|---------|---------|-------|-----|
| $f_{out}$               | Output Frequency                     | QB/nQB               | PLL Mode                      | 140     | 155.52  | 170   | MHz |
|                         |                                      | QA/nQA               |                               | 140     | 156.25  | 170   | MHz |
| $t_{jitter}(\emptyset)$ | RMS Phase Jitter (Random);<br>NOTE 1 |                      | 155.52MHz, (12kHz - 1.3MHz)   |         | 0.86    |       | ps  |
|                         |                                      |                      | 156.25MHz, (1.875MHz - 20MHz) |         | 0.56    |       | ps  |
| $t_r / t_f$             | Output Rise/Fall Time                | PLL Mode, 20% to 80% | 300                           |         | 550     | ps    |     |
| odc                     | Output Duty Cycle                    | PLL Mode             | 49                            |         | 51      | %     |     |

All parameters measured up to 170MHz unless otherwise specified.

NOTE 1: See Phase Noise plots.

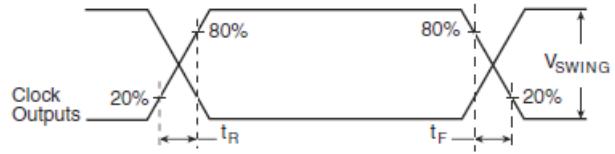
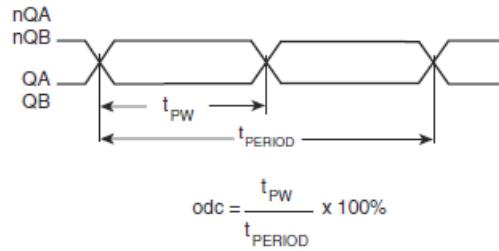


# PARAMETER MEASUREMENT INFORMATION



## 3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT

## RMS PHASE JITTER



## OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

## OUTPUT RISE/FALL TIME

## APPLICATION INFORMATION

### POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 843202I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{CC}$ ,  $V_{CCA}$ , and  $V_{CCO_X}$  should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a  $10\Omega$  resistor along with a  $10\mu F$  and a  $.01\mu F$  bypass capacitor should be connected to each  $V_{CCA}$ .

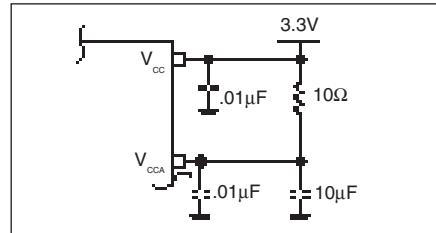


FIGURE 1. POWER SUPPLY FILTERING

### CRYSTAL INPUT INTERFACE

The 843202I has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below

were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error.

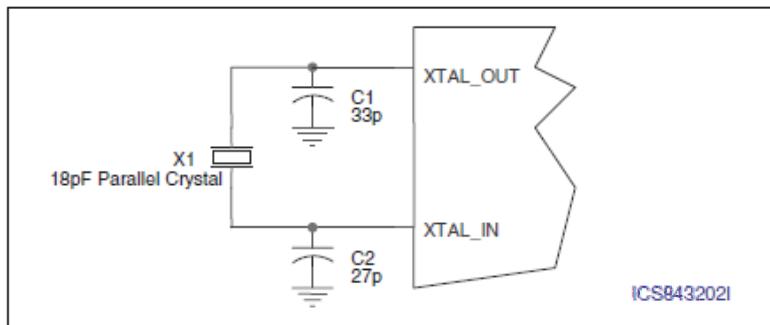


FIGURE 2. CRYSTAL INPUT INTERFACE

## LVC MOS TO XTAL INTERFACE

The XTAL\_IN input can accept a single-ended LVC MOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3*. The XTAL\_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVC MOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output

impedance of the driver ( $Ro$ ) plus the series resistance ( $Rs$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First,  $R1$  and  $R2$  in parallel should equal the transmission line impedance. For most  $50\Omega$  applications,  $R1$  and  $R2$  can be  $100\Omega$ . This can also be accomplished by removing  $R1$  and making  $R2$   $50\Omega$ .

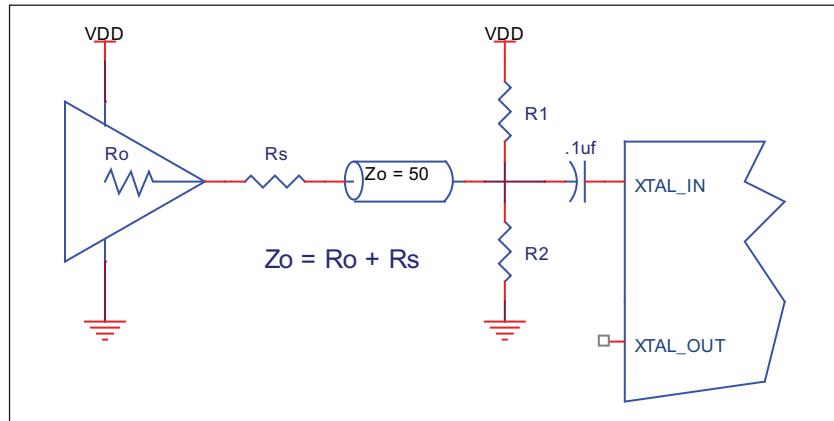


FIGURE 3. GENERAL DIAGRAM FOR LVC MOS DRIVER TO XTAL INPUT INTERFACE

## RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

### INPUTS:

#### CRYSTAL INPUT:

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. Though not required, but for additional protection, a  $1\text{k}\Omega$  resistor can be tied from XTAL\_IN to ground.

#### REC\_CLK/nREC\_CLK INPUT:

For applications not requiring the use of the differential input, both REC\_CLK and nREC\_CLK can be left floating. Though not required, but for additional protection, a  $1\text{k}\Omega$  resistor can be tied from REC\_CLK to ground.

#### LVC MOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A  $1\text{k}\Omega$  resistor can be used.

### OUTPUTS:

#### LVPECL OUTPUT

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

## TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive  $50\Omega$  transmission

lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figures 4A and 4B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

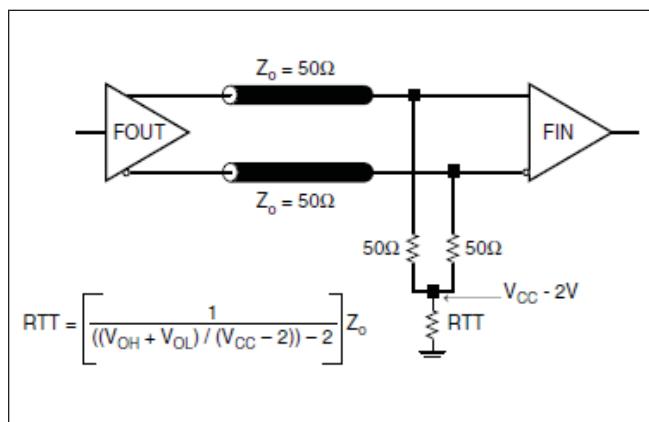


FIGURE 4A. LVPECL OUTPUT TERMINATION

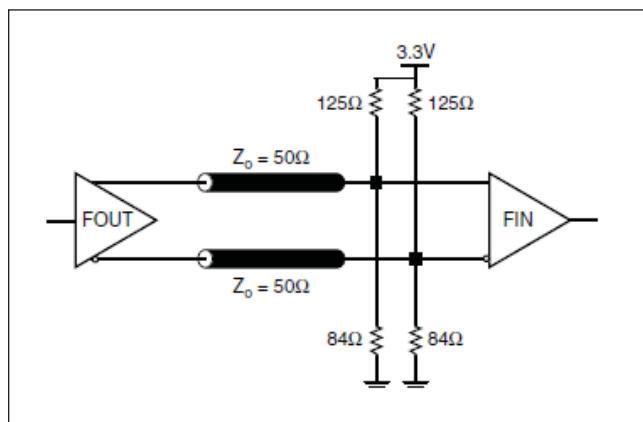


FIGURE 4B. LVPECL OUTPUT TERMINATION

## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 843202I. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 843202I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{cc} = 3.3V + 10\% = 3.63V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{cc\_MAX} * I_{EE\_MAX} = 3.63V * 138mA = 500.9\text{mW}$
- Power (outputs)<sub>MAX</sub> = **30mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $2 * 30\text{mW} = 60\text{mW}$

**Total Power<sub>MAX</sub>** (3.63V, with all outputs switching) =  $500.9\text{mW} + 60\text{mW} = 560.9\text{mW}$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * P_{d\_total} + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$P_{d\_total}$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 71.2°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$85^\circ\text{C} + 0.561\text{W} * 71.2^\circ\text{C/W} = 124.9^\circ\text{C}$ . This is below the limit of 125°C.

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 6. THERMAL RESISTANCE  $\theta_{JA}$  FOR 32-PIN LQFP, FORCED CONVECTION**

| <b><math>\theta_{JA}</math> by Velocity (Meter per Second)</b> |          |          |          |
|----------------------------------------------------------------|----------|----------|----------|
|                                                                | 0        | 1        | 2.5      |
| Multi-Layer PCB, JEDEC Standard Test Boards                    | 80.8°C/W | 71.2°C/W | 67.6°C/W |

### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 5*.

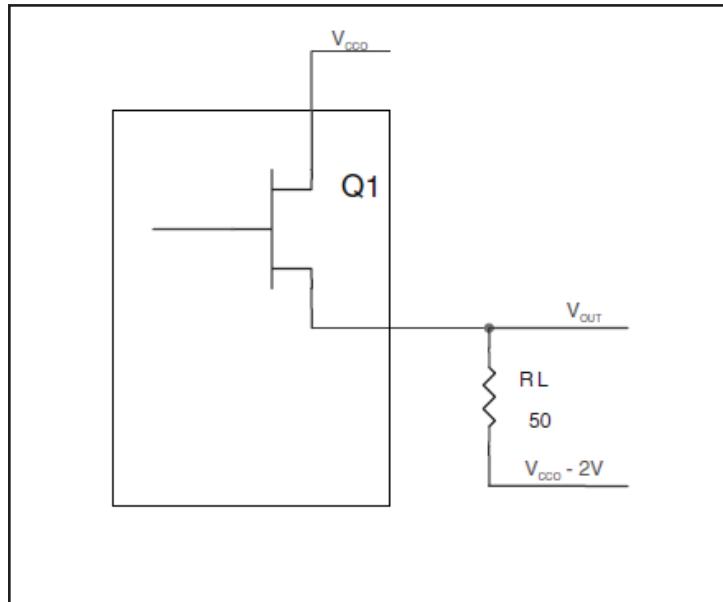


FIGURE 5. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a  $50\Omega$  load, and a termination voltage of  $V_{cco} - 2V$ .

- For logic high,  $V_{out} = V_{oh\_max} = V_{cco\_max} - 0.9V$

$$(V_{cco\_max} - V_{oh\_max}) = 0.9V$$

- For logic low,  $V_{out} = V_{ol\_max} = V_{cco\_max} - 1.7V$

$$(V_{cco\_max} - V_{ol\_max}) = 1.7V$$

$Pd_H$  is power dissipation when the output drives high.

$Pd_L$  is the power dissipation when the output drives low.

$$Pd_H = [(V_{oh\_max} - (V_{cco\_max} - 2V))/R_L] * (V_{cco\_max} - V_{oh\_max}) = [(2V - (V_{cco\_max} - V_{oh\_max}))/R_L] * (V_{cco\_max} - V_{oh\_max}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd_L = [(V_{ol\_max} - (V_{cco\_max} - 2V))/R_L] * (V_{cco\_max} - V_{ol\_max}) = [(2V - (V_{cco\_max} - V_{ol\_max}))/R_L] * (V_{cco\_max} - V_{ol\_max}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

Total Power Dissipation per output pair =  $Pd_H + Pd_L = 30mW$

## RELIABILITY INFORMATION

TABLE 7.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 32 LEAD LQFP

| Multi-Layer PCB, JEDEC Standard Test Boards | $\theta_{JA}$ by Velocity (Meter per Second) |          |          |
|---------------------------------------------|----------------------------------------------|----------|----------|
|                                             | 0                                            | 1        | 2.5      |
|                                             | 80.8°C/W                                     | 71.2°C/W | 67.6°C/W |

### TRANSISTOR COUNT

The transistor count for 843202I is: 3733

## PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD LQFP

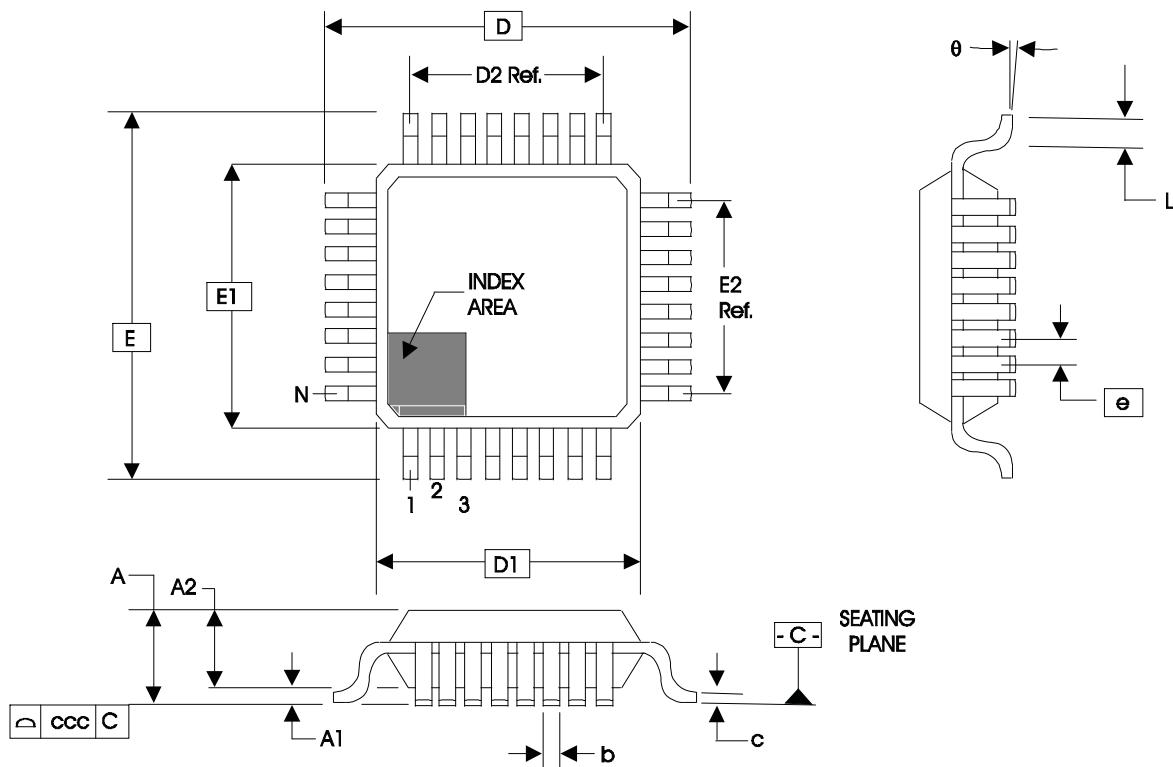


TABLE 8. PACKAGE DIMENSIONS

| JEDEC VARIATION<br>ALL DIMENSIONS IN MILLIMETERS |            |         |         |
|--------------------------------------------------|------------|---------|---------|
| SYMBOL                                           | BBA        |         |         |
|                                                  | MINIMUM    | NOMINAL | MAXIMUM |
| N                                                | 32         |         |         |
| A                                                | --         | --      | 1.60    |
| A1                                               | 0.05       | --      | 0.15    |
| A2                                               | 1.35       | 1.40    | 1.45    |
| b                                                | 0.30       | 0.37    | 0.45    |
| c                                                | 0.09       | --      | 0.20    |
| D                                                | 9.00 BASIC |         |         |
| D1                                               | 7.00 BASIC |         |         |
| D2                                               | 5.60 Ref.  |         |         |
| E                                                | 9.00 BASIC |         |         |
| E1                                               | 7.00 BASIC |         |         |
| E2                                               | 5.60 Ref.  |         |         |
| e                                                | 0.80 BASIC |         |         |
| L                                                | 0.45       | 0.60    | 0.75    |
| θ                                                | 0°         | --      | 7°      |
| ccc                                              | --         | --      | 0.10    |

Reference Document: JEDEC Publication 95, MS-026

**TABLE 9. ORDERING INFORMATION**

| Part/Order Number | Marking      | Package                  | Shipping Packaging | Temperature   |
|-------------------|--------------|--------------------------|--------------------|---------------|
| ICS843202AYILF    | ICS843202AIL | 32 Lead "Lead-Free" LQFP | tray               | -40°C to 85°C |
| ICS843202AYILFT   | ICS843202AIL | 32 Lead "Lead-Free" LQFP | tape & reel        | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

**REVISION HISTORY SHEET**

| <b>Rev</b> | <b>Table</b> | <b>Page</b> | <b>Description of Change</b>                                                        | <b>Date</b> |
|------------|--------------|-------------|-------------------------------------------------------------------------------------|-------------|
| A          | T9           | 14          | Ordering Information - removed leaded devices.<br>Updated data sheet format.        | 10/15/15    |
| A          |              |             | Product Discontinuation Notice - Last time buy expires May 6, 2017.<br>PDN CQ-16-01 | 5/26/16     |



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