FemtoClock® Crystal-to-3.3V LVPECL Clock Generator

843022

DATA SHEET

PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES MAY 6, 2017

General Description

The 843022 is a Gigabit Ethernet Clock Generator and a member of the HiPerClocks™ family of high performance devices from IDT. The 843022 uses a 25MHz crystal to synthesize 125MHz or 62.5MHz. The 843022 has excellent phase jitter performance, over the 1.875MHz – 20MHz integration range. The 843022 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

Features

- One differential 3.3V LVPECL output
- Crystal oscillator interface designed for 25MHz, 18pF parallel resonant crystal
- Output frequencies: 125MHz or 62.5MHz (selectable)
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.39ps (typical)

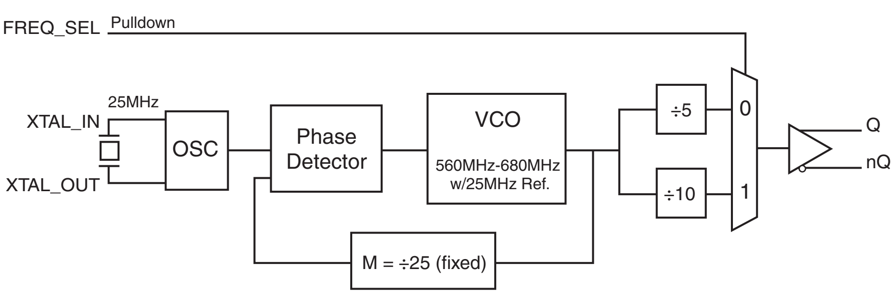
Offset	Noise Power
100Hz	-96.5 dBc/Hz
1kHz	-122.5 dBc/Hz
10kHz	-132.1 dBc/Hz
100kHz	-131.5 dBc/Hz

- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Available in lead-free (RoHS 6) package

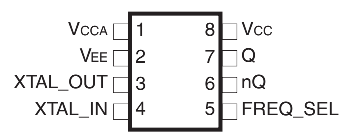
Function Table

Inputs FREQ_SEL	Output Frequencies (with a 25MHz crystal)
0	125MHz
1	62.5MHz

Block Diagram



Pin Assignment



843022

8-Lead TSSOP

4.40mm x 3.0mm x 0.925mm package body

G Package

Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{CCA}	Power		Analog supply pin.
2	V_{EE}	Power		Negative supply pin.
3, 4	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_in is the input, XTAL_OUT is the output.
5	FREQ_SEL	Input	Pulldown	Frequency select pin. LVCMOS/LVTTL interface levels.
6, 7	nQ, Q	Output		Differential clock outputs. LVPECL interface levels.
8	V_{CC}	Power		Core supply pin.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	101.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 3A. Power Supply DC Characteristics, $V_{CC} = V_{CCA}$ = 3.3V±5%, TA=0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.1	3.3	V_{CC}	V
I_{CCA}	Analog Supply Current				10	mA
I_{EE}	Power Supply Current				90	mA

Table 3B. LVCMOS/LVTTL DC Characteristics, $V_{CC} = V_{CCA}$ = 3.3V±5%, TA=0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	FREQ_SEL	$V_{CC} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	FREQ_SEL	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA

Table 3C. LVPECL DC Characteristics, $V_{CC} = V_{CCA}$ = 3.3V±5%, TA=0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.4		V_{CC} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

Table 4. Crystal Characteristics

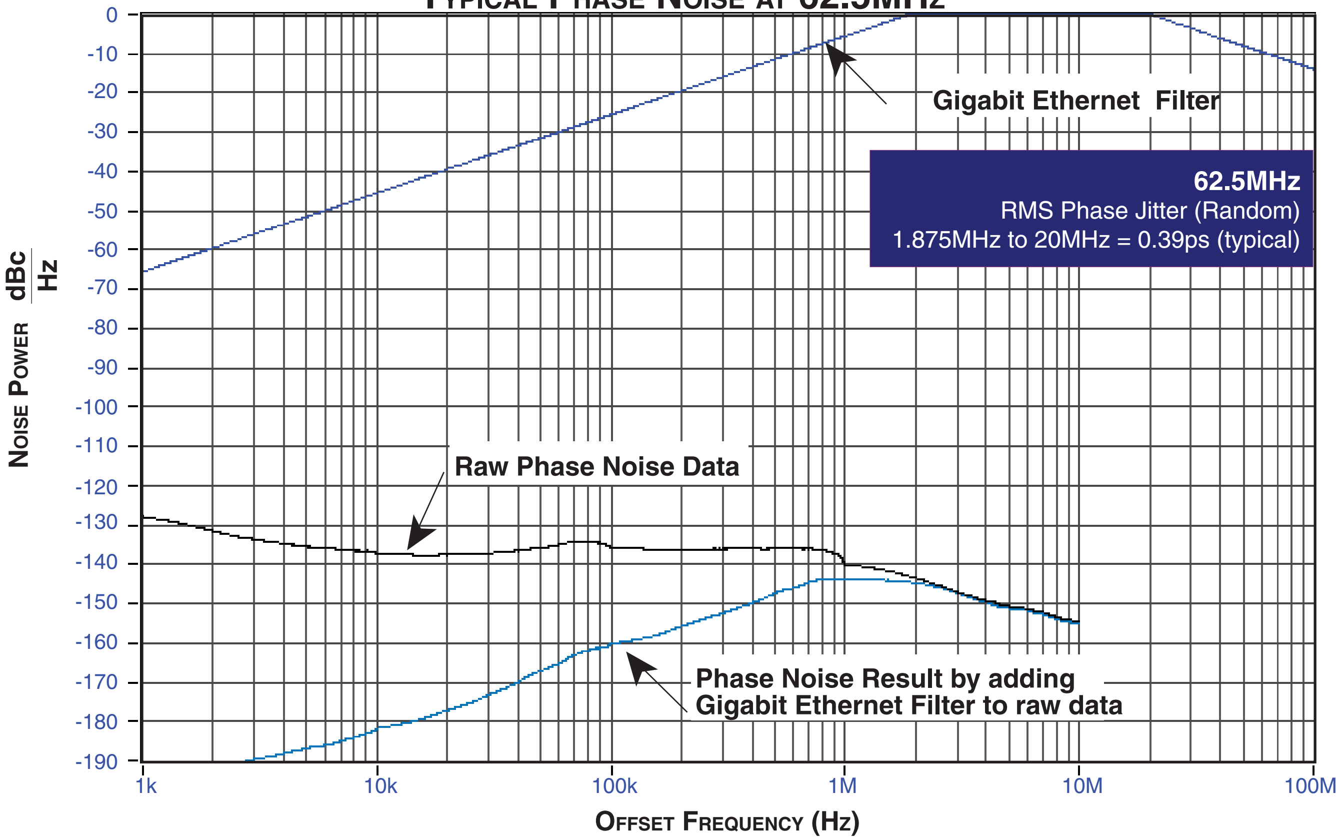
Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

TABLE 5. AC CHARACTERISTICS, $V_{CC} = V_{CCA}$ = 3.3V±5%, TA=0°C TO 70°C

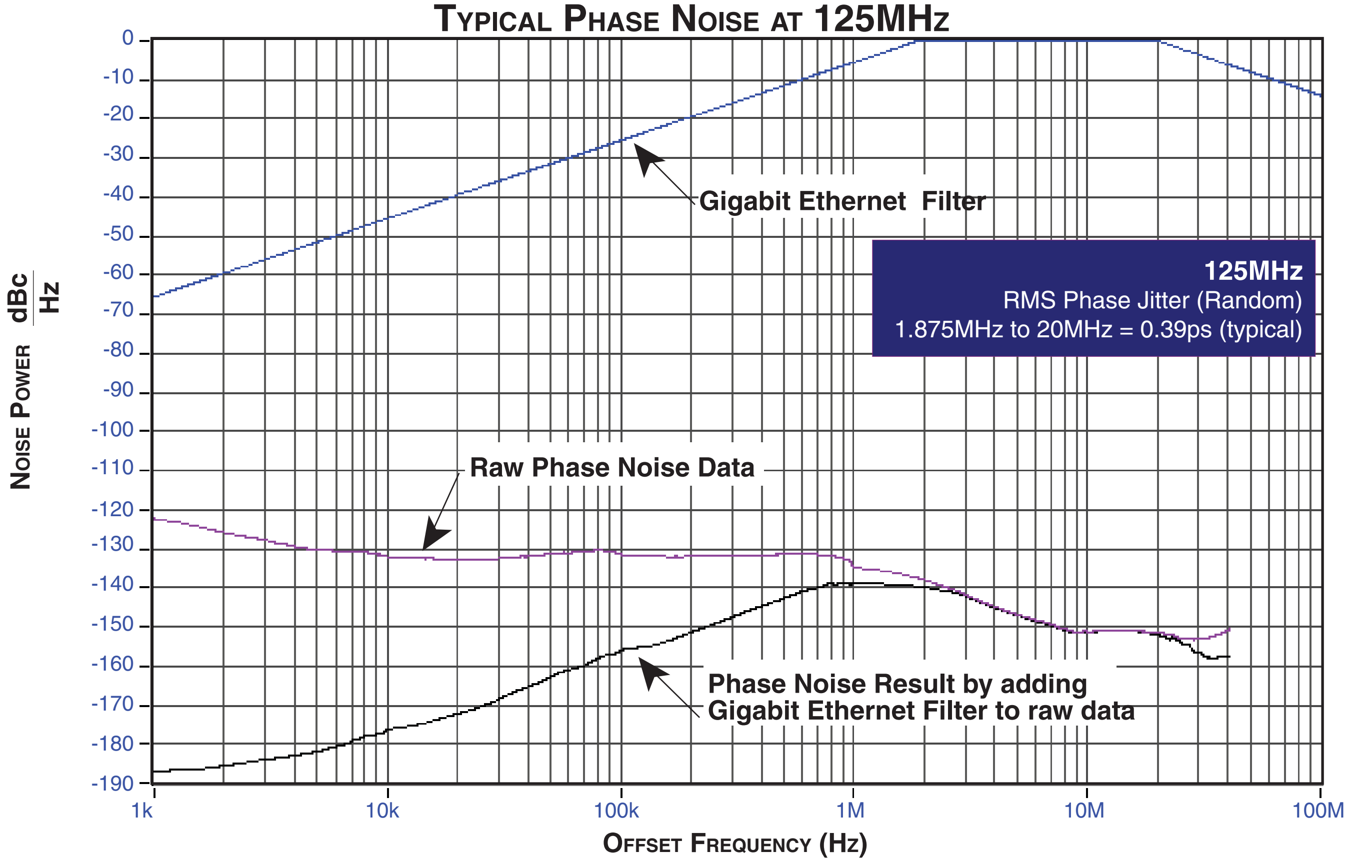
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL = 0		125		MHz
		F_SEL = 1		62.5		MHz
*t*jit(Ø)	RMS Phase Jitter; NOTE 1	125MHz, Integration Range: 1.875MHz - 20MHz		0.39		ps
		62.5MHz, Integration Range: 1.875MHz - 20MHz		0.39		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	300		600	ps
odc	Output Duty Cycle		48		52	%

NOTE 1: Please refer to the Phase Noise Plot.

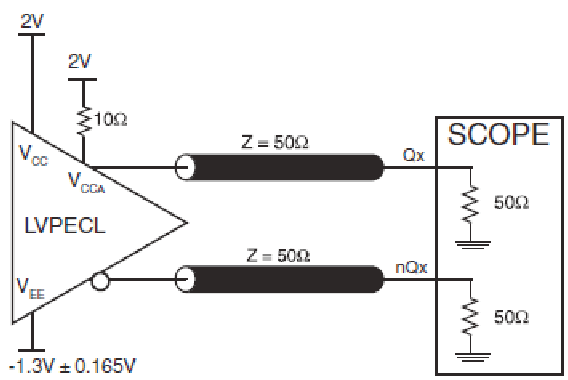
Typical Phase Noise at 62.5MHz



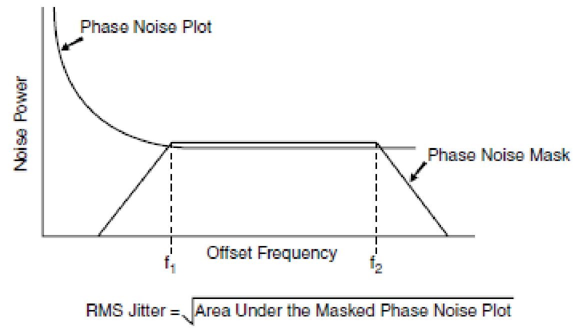
Typical Phase Noise at 125MHz



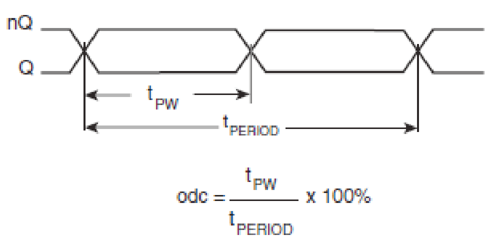
Parameter Measurement Information



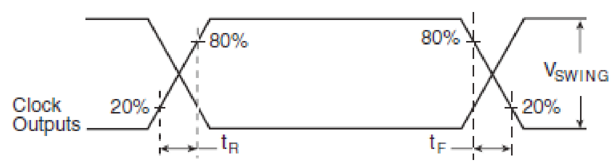
3.3V Output Load AC Test Circuit



RMS Phase Jitter



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 843022 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC} and V_{CCA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA} pin.

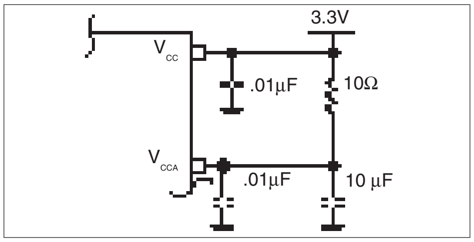


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The 843022 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

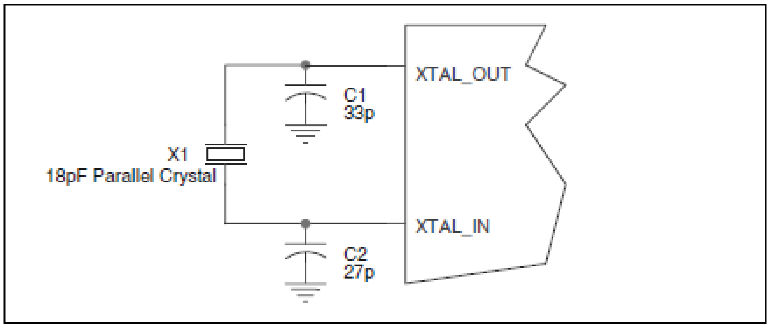


Figure 2. CRYSTAL INPUT INTERFACE

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

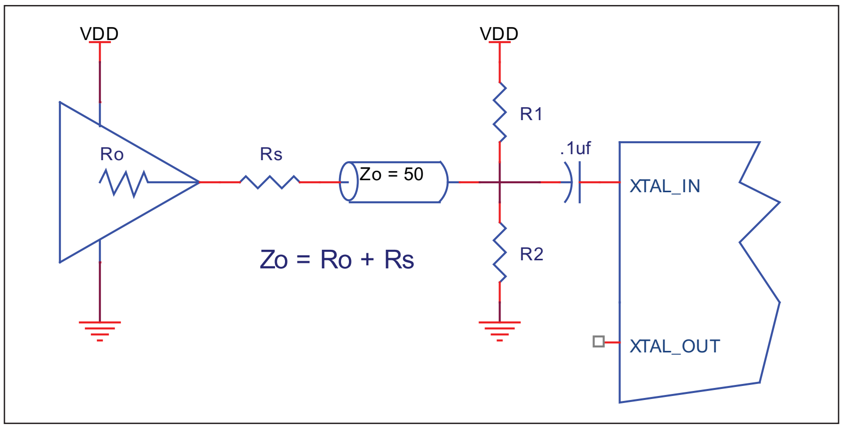


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

Application Schematic

Figure 4A shows a schematic example of the 843022. An example of LVEPCL termination is shown in this schematic. Additional LVPECL termination approaches are shown in the LVPECL Termination Application Note. In this example, an 18pF parallel resonant 25MHz crystal is used for generating 125MHz output frequency. The C1 = 27pF and C2 = 33pF are recommended for frequency accuracy. For different board layout, the C1 and C2 values may be slightly adjusted for optimizing frequency accuracy.

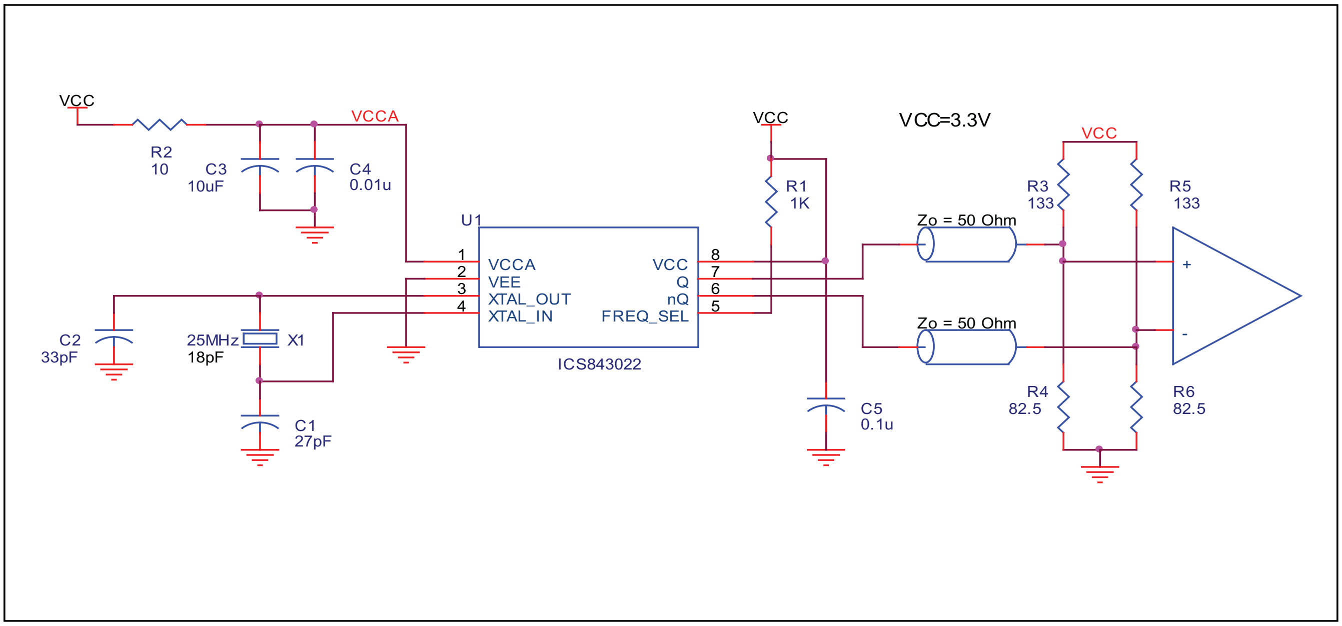


Figure 4A. 843022 Schematic Example

PC Board Layout Example

Figure 4B shows an example of P.C. board layout. The crystal X1 footprint in this example allows either surface mount (HC49S) or through hole (HC49) package. C3 is 0805. C1 and C2 are 0402. Other resistors and capacitors are 0603. This layout assumes that the board has clean analog power and ground planes.

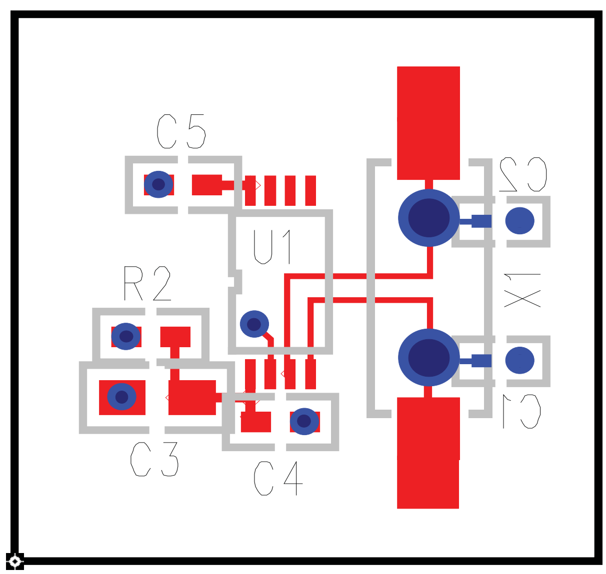


Figure 4B. 843022 PC Board Layout Example

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 843022.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the 843022 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 90mA = **311.85mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**

Total Power $_{\_MAX}$ (3.465V, with all outputs switching) = 311.85mW + 30mW = **341.85mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 90.5°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.342W * 90.5°C/W = 101°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 8-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 5.*

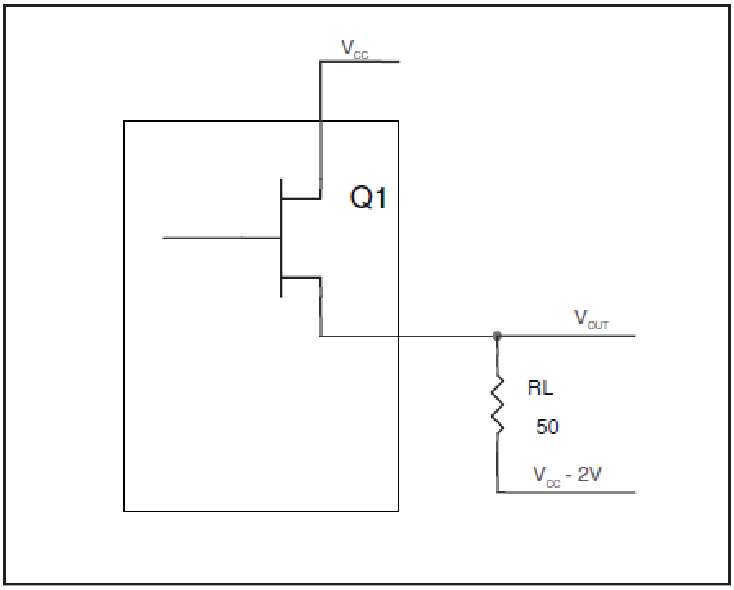


FIGURE 5. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.9V}$

  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.7V}$

  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$

$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for 8 Lead TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

Transistor Count

The transistor count for 843022 is: 1928

PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP

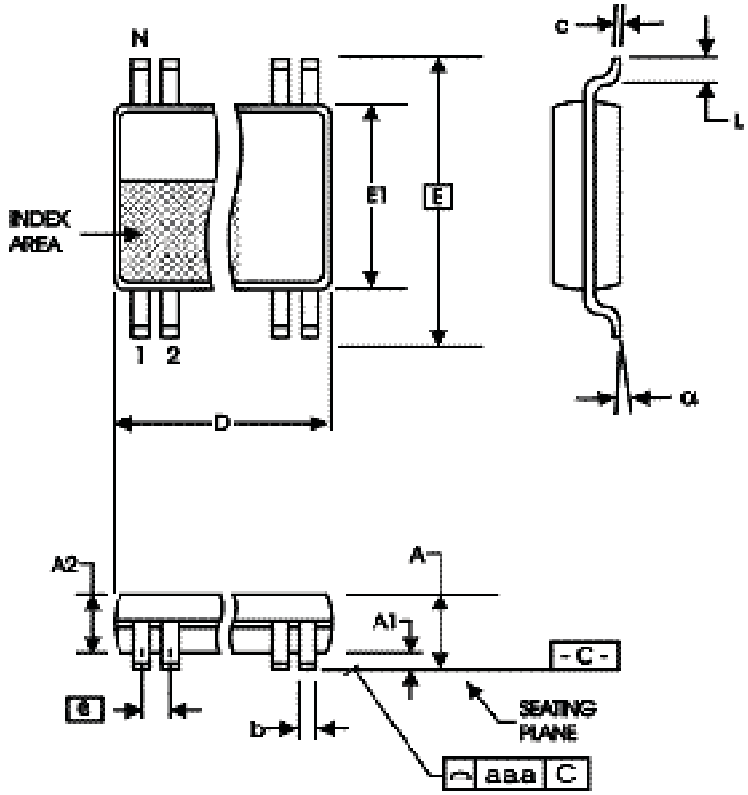


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843022AGLF	022AL	8 lead “Lead-Free” TSSOP	Tube	0°C to 70°C
843022AGLFT	022AL	8 lead “Lead-Free” TSSOP	Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T9	14	Ordering Information - removed leaded devices. Updated data sheet format.	11/16/15
A			Product Discontinuation Notice - Last time buy expires May 6, 2017. PDN CQ-16-01	5/26/16

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