

GENERAL DESCRIPTION

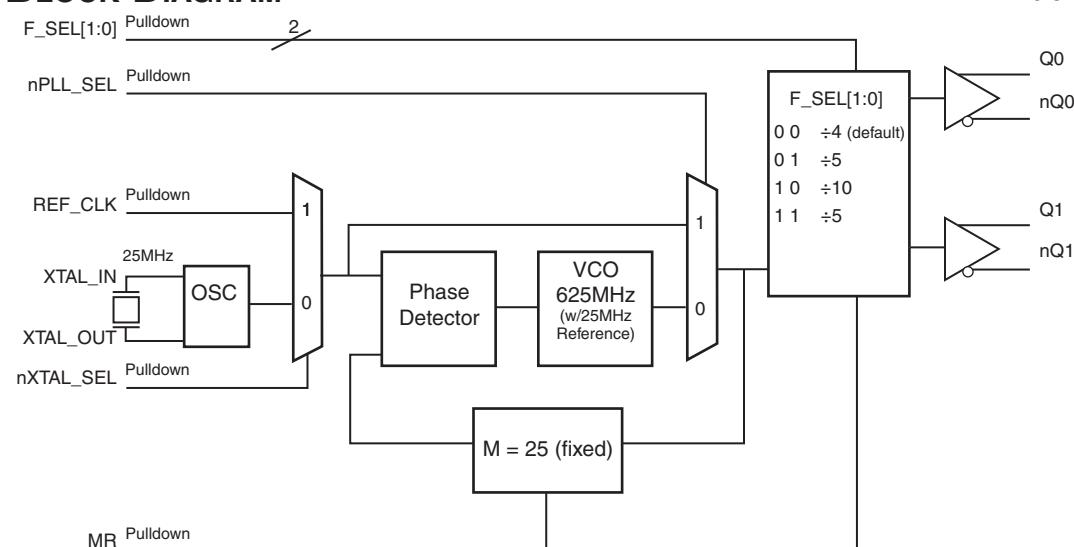
The 843002I-01 is a 2 output LVPECL synthesizer optimized to generate Ethernet reference clock frequencies. Using a 25MHz 18pF parallel resonant crystal, the following frequencies can be generated based on the 2 frequency select pins (F_SEL[1:0]): 156.25MHz, 125MHz, and 62.5MHz. The 843002I-01 uses IDT's FemtoClock® low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Ethernet jitter requirements. The 843002I-01 is packaged in a small 20-pin TSSOP package.

FEATURES

- Two 3.3V or 2.5V LVPECL outputs
- Selectable crystal oscillator interface or LVCMS/LVTTL single-ended input
- Supports the following output frequencies: 156.25MHz, 125MHz and 62.5MHz
- VCO range: 560MHz - 680MHz
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (1.875MHz-20MHz): 0.55ps (typical)
- Output skew: 30ps (maximum)
- Supply Voltage Modes
 - Core/Outputs
 - 3.3/3.3
 - 2.5/2.5
- -40°C to 85°C ambient operating temperature
- Available in lead-free RoHS-compliant package

FREQUENCY SELECT FUNCTION TABLE

| Inputs | | | | Output Frequency (25MHz Ref.) |
|--------|--------|-----------------|-----------------|----------------------------------|
| F_SEL1 | F_SEL0 | M Divider Value | N Divider Value | |
| 0 | 0 | 25 | 4 | 156.25 (default) |
| 0 | 1 | 25 | 5 | 125 |
| 1 | 0 | 25 | 10 | 62.5 |
| 1 | 1 | 25 | 5 | 125 |

BLOCK DIAGRAM**PIN ASSIGNMENT**

| | | | |
|----------|----|----|-----------|
| nc | 1 | 20 | Vcc0 |
| Vcc0 | 2 | 19 | Q1 |
| Q0 | 3 | 18 | nQ1 |
| nQ0 | 4 | 17 | VEE |
| MR | 5 | 16 | Vcc |
| nPLL_SEL | 6 | 15 | nXTAL_SEL |
| nc | 7 | 14 | REF_CLK |
| VccA | 8 | 13 | XTAL_IN |
| F_SEL0 | 9 | 12 | XTAL_OUT |
| Vcc | 10 | 11 | F_SEL1 |

843002I-01
20-Lead TSSOP
6.5mm x 4.4mm x 0.92mm
package body
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | Description | |
|--------|-----------------------|--------|--|---|
| 1, 7 | nc | Unused | No connect. | |
| 2, 20 | V_{CCO} | Power | Output supply pins. | |
| 3, 4 | Q_0, nQ_0 | Output | Differential output pair. LVPECL interface levels. | |
| 5 | MR | Input | Pulldown | Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Q_x to go low and the inverted outputs nQ_x to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels. |
| 6 | $nPLL_SEL$ | Input | Pulldown | Determines whether synthesizer is in PLL or bypass mode. LVCMOS/LVTTL interface levels. |
| 8 | V_{CCA} | Power | | Analog supply pin. |
| 9, 11 | F_SEL0, F_SEL1 | Input | Pulldown | Frequency select pins. LVCMOS/LVTTL interface levels. |
| 10, 16 | V_{CC} | Power | | Core supply pin. |
| 12, 13 | $XTAL_OUT, XTAL_IN$ | Input | | Parallel resonant crystal interface. $XTAL_OUT$ is the output, $XTAL_IN$ is the input. |
| 14 | REF_CLK | Input | Pulldown | LVCMOS/LVTTL reference clock input. |
| 15 | $nXTAL_SEL$ | Input | Pulldown | Selects between crystal or REF_CLK inputs as the the PLL Reference source. Selects XTAL inputs when LOW. Selects REF_CLK when HIGH. LVCMOS/LVTTL interface levels. |
| 17 | V_{EE} | Power | | Negative supply pins. |
| 18, 19 | nQ_1, Q_1 | Output | | Differential output pair. LVPECL interface levels. |

NOTE: refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------|-------------------------|-----------------|---------|---------|---------|------------|
| C_{IN} | Input Capacitance | | | 4 | | pF |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | k Ω |

ABSOLUTE MAXIMUM RATINGS

| | |
|--|--------------------------|
| Supply Voltage, V_{CC} | 4.6V |
| Inputs, V_I | -0.5V to $V_{CC} + 0.5V$ |
| Outputs, I_O | |
| Continuous Current | 50mA |
| Surge Current | 100mA |
| Package Thermal Impedance, θ_{JA} | 73.2°C/W (0 lfpm) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 10\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|---------|---------|---------|-------|
| V_{CC} | Core Supply Voltage | | 2.97 | 3.3 | 3.63 | V |
| V_{CCA} | Analog Supply Voltage | | 2.97 | 3.3 | 3.63 | V |
| V_{CCO} | Output Supply Voltage | | 2.97 | 3.3 | 3.63 | V |
| I_{EE} | Power Supply Current | | | | 130 | mA |
| I_{CCA} | Analog Supply Current | | | | 13 | mA |

TABLE 3B. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|---------|---------|---------|-------|
| V_{CC} | Core Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| V_{CCA} | Analog Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| V_{CCO} | Output Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| I_{EE} | Power Supply Current | | | | 115 | mA |
| I_{CCA} | Analog Supply Current | | | | 12 | mA |

TABLE 3C. LVC MOS / LV TTL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 10\%$ OR $2.5V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|--------------------|----------------------------------|---------------------------------------|---------|----------------|---------|
| V_{IH} | Input High Voltage | $V_{CC} = 3.3V$ | 2 | | $V_{CC} + 0.3$ | V |
| | | $V_{CC} = 2.5V$ | 1.7 | | $V_{CC} + 0.3$ | V |
| V_{IL} | Input Low Voltage | $V_{CC} = 3.3V$ | -0.3 | | 0.8 | V |
| | | $V_{CC} = 2.5V$ | -0.3 | | 0.7 | V |
| I_{IH} | Input High Current | REF_CLK, MR, nPLL_SEL, nXTAL_SEL | $V_{CC} = V_{IN} = 3.63V$ or $2.625V$ | | 150 | μA |
| I_{IL} | Input Low Current | REF_CLK, MR, nPLL_SEL, nXTAL_SEL | $V_{CC} = V_{IN} = 3.63V$ or $2.625V$ | -5 | | μA |

TABLE 3D. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 10\%$ OR $2.5V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|-----------------------------------|-----------------|-----------------|---------|-----------------|-------|
| V_{OH} | Output High Voltage; NOTE 1 | | $V_{CCO} - 1.4$ | | $V_{CCO} - 0.9$ | V |
| V_{OL} | Output Low Voltage; NOTE 1 | | $V_{CCO} - 2.0$ | | $V_{CCO} - 1.7$ | V |
| V_{SWING} | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{CCO} - 2V$.

TABLE 4. CRYSTAL CHARACTERISTICS

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|------------------------------------|-----------------|---------|---------|---------|----------|
| Mode of Oscillation | Fundamental | | | | |
| Frequency | | 22.4 | 25 | 27.2 | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |
| Drive Level | | | | 1 | mW |

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 5A. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 10\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------------------|-----------------------------|-------------------------------|---------|---------|---------|-------|
| f_{OUT} | Output Frequency | $F_{SEL}[1:0] = 00$ | 140 | | 170 | MHz |
| | | $F_{SEL}[1:0] = 01$ | 112 | | 136 | MHz |
| | | $F_{SEL}[1:0] = 10$ | 56 | | 68 | MHz |
| $tsk(o)$ | Output Skew; NOTE 1, 2 | | | | 30 | ps |
| $t_{jitter}(\emptyset)$ | RMS Phase Jitter; NOTE 2, 3 | 156.25MHz, (1.875MHz - 20MHz) | | 0.55 | | ps |
| | | 125MHz, (1.875MHz - 20MHz) | | 0.60 | | ps |
| | | 62.5MHz, (1.875MHz - 20MHz) | | 0.70 | | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 350 | | 650 | ps |
| odc | Output Duty Cycle | | 48 | | 52 | % |

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions.

Measured at the output differential cross points.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

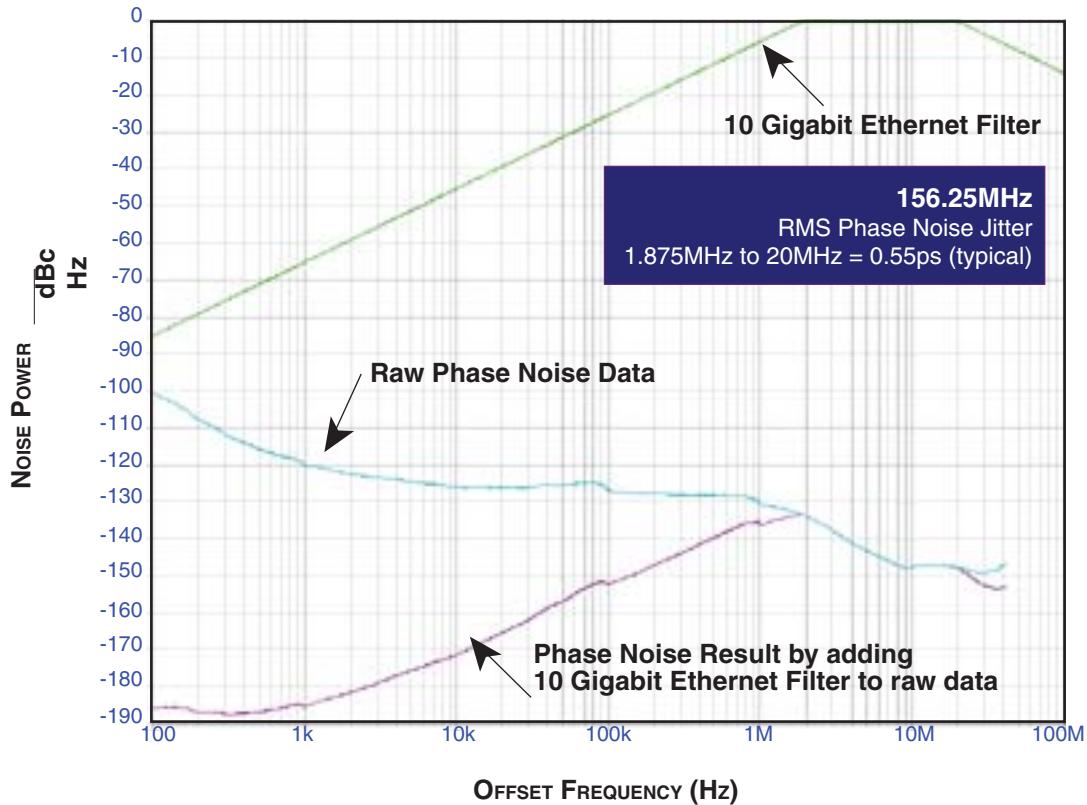
NOTE 3: Measured using crystal input.

TABLE 5B. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

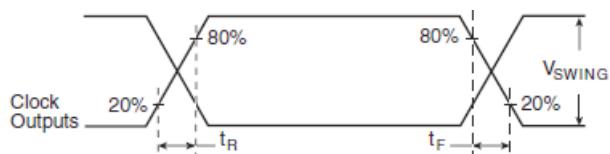
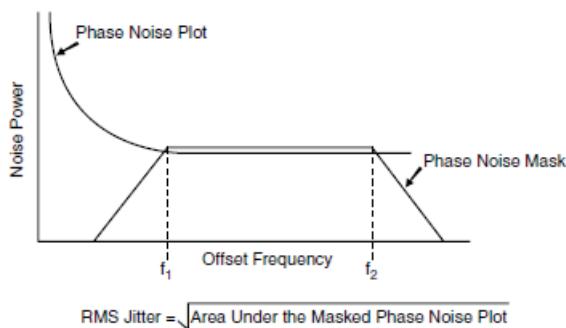
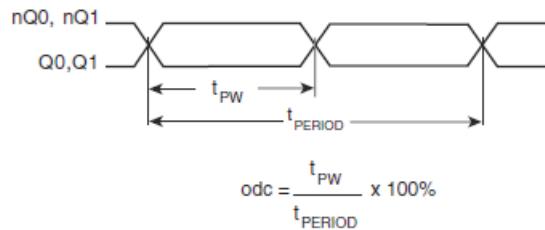
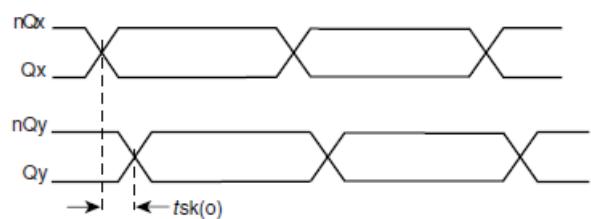
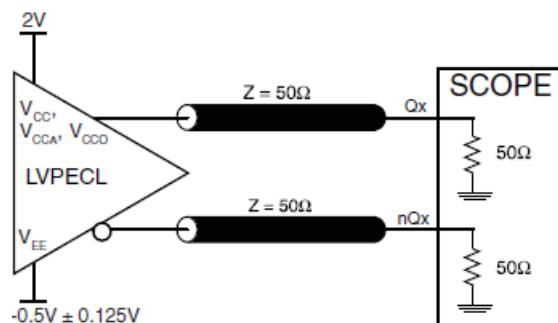
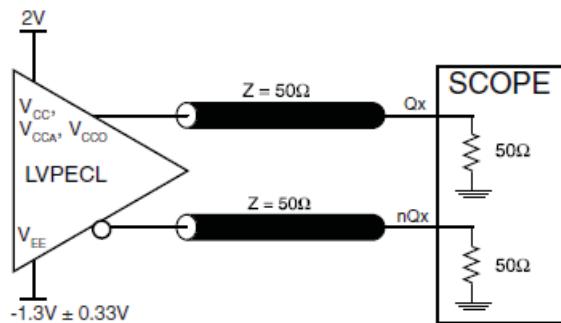
| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------------------|-----------------------------|-------------------------------|---------|---------|---------|-------|
| f_{OUT} | Output Frequency | $F_{SEL}[1:0] = 00$ | 140 | | 170 | MHz |
| | | $F_{SEL}[1:0] = 01$ | 112 | | 136 | MHz |
| | | $F_{SEL}[1:0] = 10$ | 56 | | 68 | MHz |
| $tsk(o)$ | Output Skew; NOTE 1, 2 | | | | 30 | ps |
| $t_{jitter}(\emptyset)$ | RMS Phase Jitter; NOTE 2, 3 | 156.25MHz, (1.875MHz - 20MHz) | | 0.55 | | ps |
| | | 125MHz, (1.875MHz - 20MHz) | | 0.60 | | ps |
| | | 62.5MHz, (1.875MHz - 20MHz) | | 0.74 | | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 350 | | 650 | ps |
| odc | Output Duty Cycle | | 48 | | 52 | % |

For Notes, see Table 5A above.

TYPICAL PHASE NOISE AT 156.25MHz @ 3.3V



PARAMETER MEASUREMENT INFORMATION



APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 843002I-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC} , V_{CCA1} , and V_{CCA0} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a $10\mu F$ and a $.01\mu F$ bypass capacitor should be connected to each V_{CCA} .

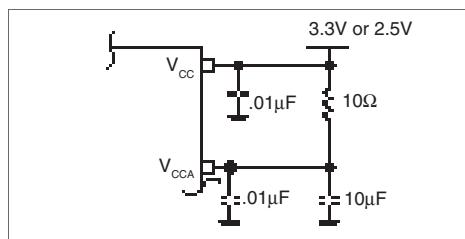


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The 843002I-01 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz 18pF

parallel resonant crystal and were chosen to minimize the ppm error.

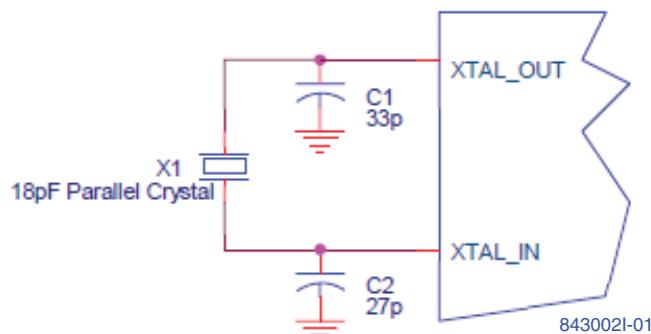


FIGURE 2. CRYSTAL INPUT INTERFACE

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUT:

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a $1\text{k}\Omega$ resistor can be tied from XTAL_IN to ground.

REF_CLK INPUT:

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a $1\text{k}\Omega$ resistor can be tied from the REF_CLK to ground.

LVCMOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A $1\text{k}\Omega$ resistor can be used.

OUTPUTS:

LVPECL OUTPUT

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to

drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figures 3A and 3B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

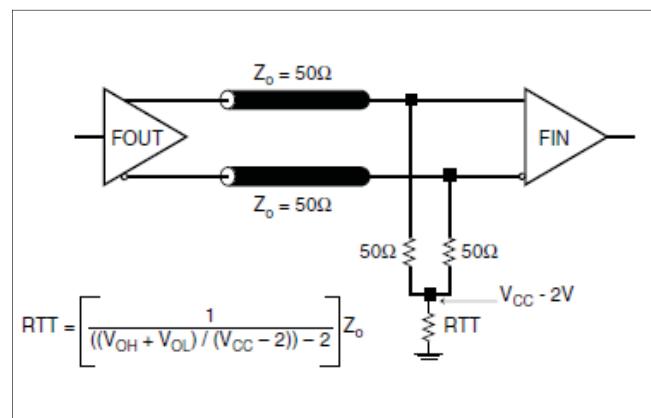


FIGURE 3A. LVPECL OUTPUT TERMINATION

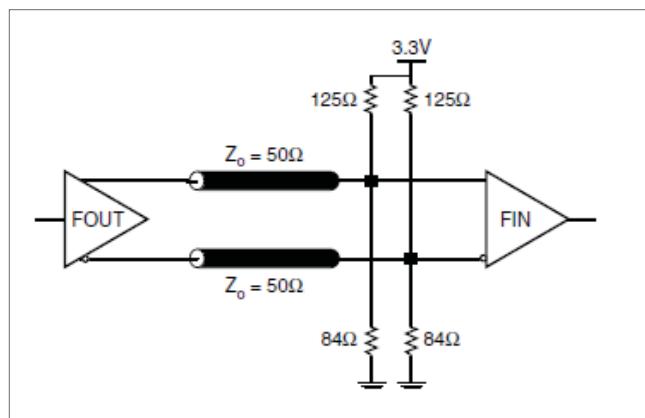


FIGURE 3B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 4A and Figure 4B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{CC} - 2V$. For $V_{CCO} = 2.5V$, the $V_{CCO} - 2V$ is very close to

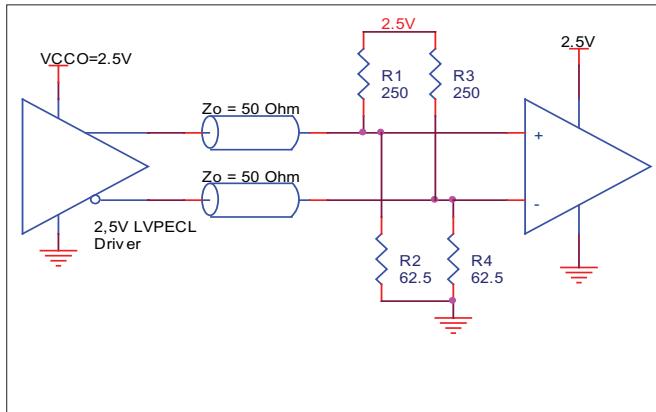


FIGURE 4A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

ground level. The R3 in Figure 4B can be eliminated and the termination is shown in Figure 4C.

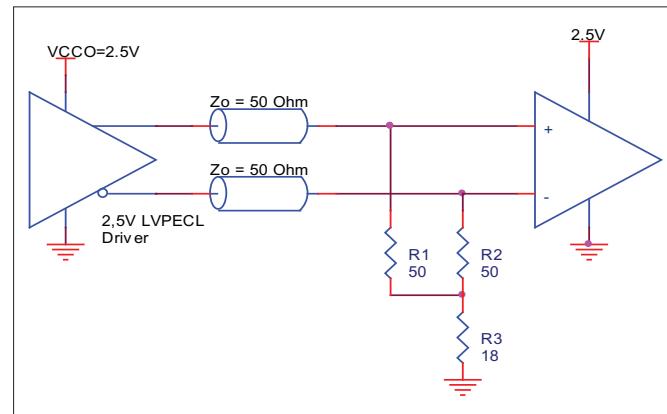


FIGURE 4B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

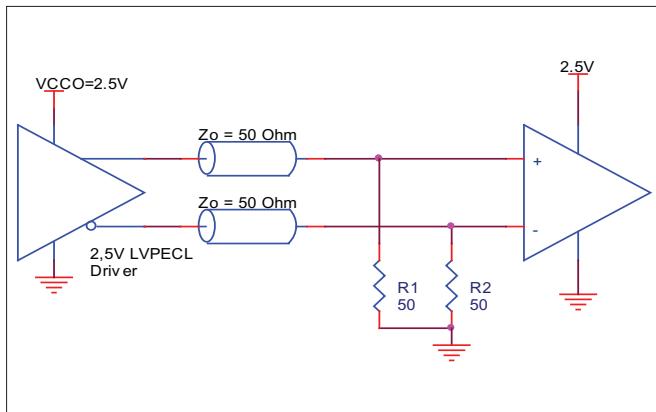


FIGURE 4C. 2.5V LVPECL TERMINATION EXAMPLE

LAYOUT GUIDELINE

Figure 5A shows a schematic example of the 843002I-01. An example of LVEPCL termination is shown in this schematic. Additional LVPECL termination approaches are shown in the LVPECL Termination Application Note. In this example, an 18 pF

parallel resonant 26.5625MHz crystal is used. The C1=27pF and C2=33pF are recommended for frequency accuracy. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy.

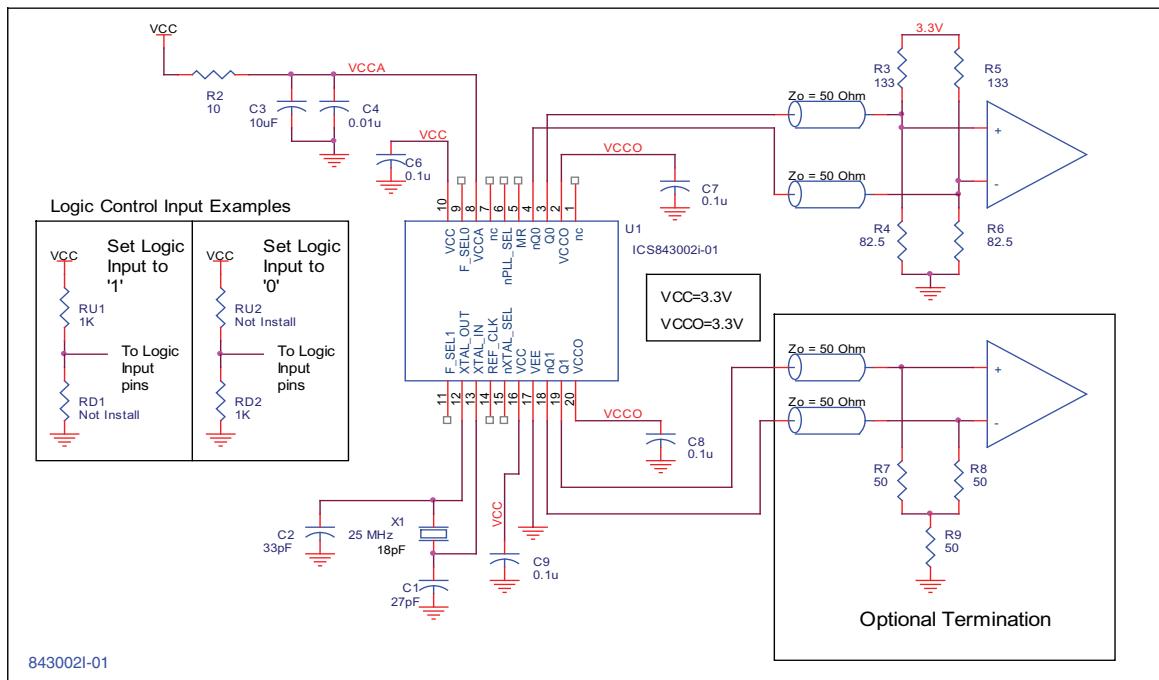


FIGURE 5A. 843002I-01 SCHEMATIC EXAMPLE

PC BOARD LAYOUT EXAMPLE

Figure 5B shows an example of 843002I-01 P.C. board layout. The crystal X1 footprint shown in this example allows installation of either surface mount HC49S or through-hole HC49 package. The footprints of other components in this example are listed in

the Table 6. There should be at least one decoupling capacitor per power pin. The decoupling capacitors should be located as close as possible to the power pins. The layout assumes that the board has clean analog power ground plane.

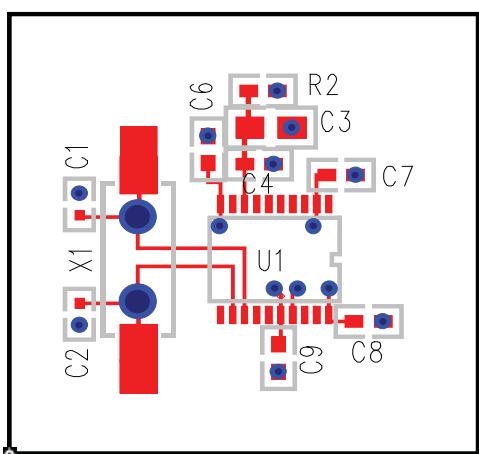


FIGURE 5B. 843002I-01 PC BOARD LAYOUT EXAMPLE

TABLE 6. FOOTPRINT TABLE

| Reference | Size |
|--------------------|------|
| C1, C2 | 0402 |
| C3 | |
| C4, C5, C6, C7, C8 | |
| R2 | |

NOTE: Table 6, lists component sizes shown in this layout example.

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 843002I-01. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 843002I-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.3V + 10\% = 3.63V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.63V * 130mA = 471.9mW$
- Power (outputs)_{MAX} = **30mW/Loaded Output pair**
If all outputs are loaded, the total power is $2 * 30mW = 60mW$

Total Power_{MAX} (3.63V, with all outputs switching) = $471.9mW + 60mW = 531.9mW$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for the devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * P_{d_total} + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

P_{d_total} = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 7 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$85^\circ C + 0.532W * 66.6^\circ C/W = 120.4^\circ C$. This is below the limit of 125°C.

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 20-PIN TSSOP, FORCED CONVECTION

| θ_{JA} by Velocity (Linear Feet per Minute) | | | |
|---|-----------|------------|------------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 114.5°C/W | 98.0°C/W | 88.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 73.2°C/W | 66.6°C/W | 63.5°C/W |
| NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs. | | | |

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6*.

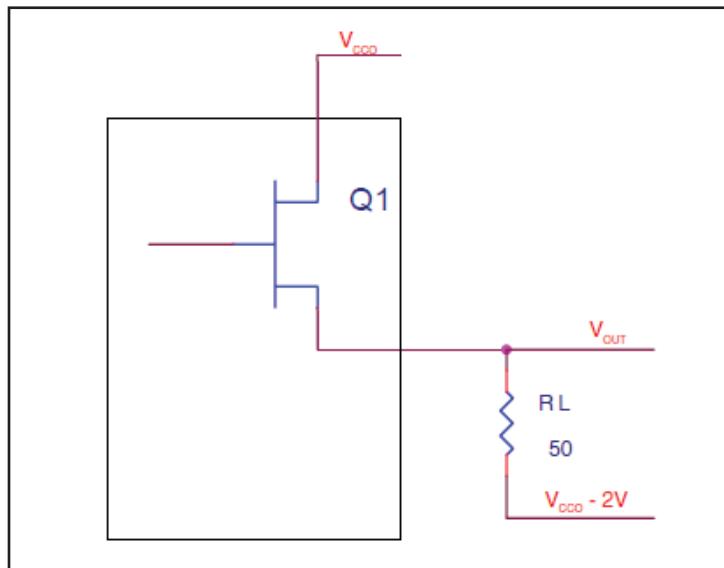


FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{cc0} - 2V$.

- For logic high, $V_{out} = V_{OH_MAX} = V_{cc0_MAX} - 0.9V$

$$(V_{cc0_MAX} - V_{OH_MAX}) = 0.9V$$

- For logic low, $V_{out} = V_{OL_MAX} = V_{cc0_MAX} - 1.7V$

$$(V_{cc0_MAX} - V_{OL_MAX}) = 1.7V$$

Pd_H is power dissipation when the output drives high.
 Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{cc0_MAX} - 2V))/R_L] * (V_{cc0_MAX} - V_{OH_MAX}) = [(2V - (V_{cc0_MAX} - V_{OH_MAX}))/R_L] * (V_{cc0_MAX} - V_{OH_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd_L = [(V_{OL_MAX} - (V_{cc0_MAX} - 2V))/R_L] * (V_{cc0_MAX} - V_{OL_MAX}) = [(2V - (V_{cc0_MAX} - V_{OL_MAX}))/R_L] * (V_{cc0_MAX} - V_{OL_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = 30mW$$

RELIABILITY INFORMATION

TABLE 8. θ_{JA} vs. AIR FLOW TABLE FOR 20 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)

| | 0 | 200 | 500 |
|--|-----------|----------|----------|
| Single-Layer PCB, JEDEC Standard Test Boards | 114.5°C/W | 98.0°C/W | 88.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 73.2°C/W | 66.6°C/W | 63.5°C/W |

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for 843002I-01 is: 2955

PACKAGE OUTLINE - G SUFFIX FOR 20 LEAD TSSOP

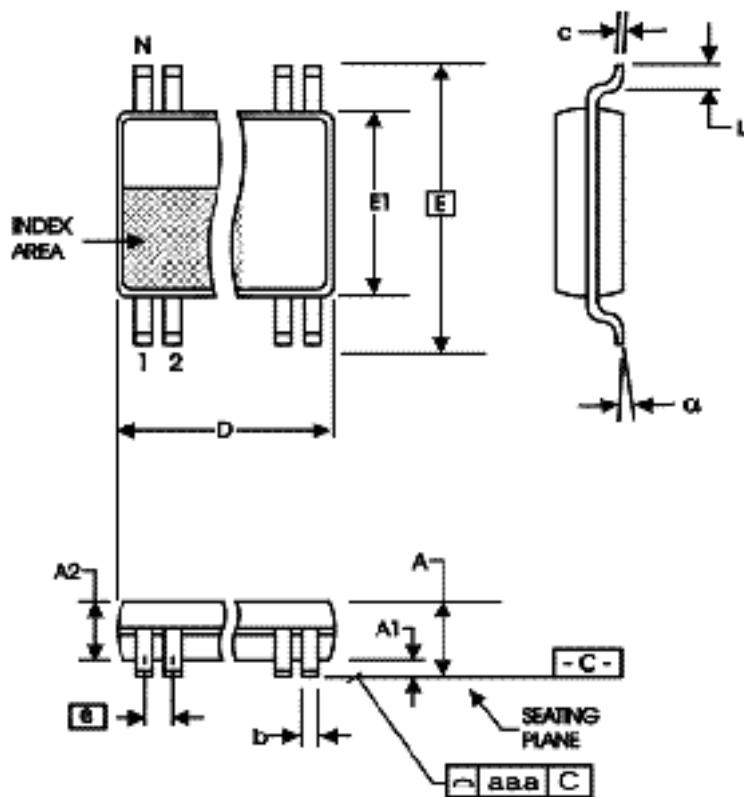


TABLE 9. PACKAGE DIMENSIONS

| SYMBOL | Millimeters | |
|----------|-------------|------|
| | MIN | MAX |
| N | 20 | |
| A | -- | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 6.40 | 6.60 |
| E | 6.40 BASIC | |
| E1 | 4.30 | 4.50 |
| e | 0.65 BASIC | |
| L | 0.45 | 0.75 |
| α | 0° | 8° |
| aaa | -- | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

TABLE 10. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|--------------|---------------------------|--------------------|---------------|
| 843002AGI-01LF | ICS3002AI01L | 20 Lead "Lead-Free" TSSOP | tube | -40°C to 85°C |
| 843002AGI-01LFT | ICS3002AI01L | 20 Lead "Lead-Free" TSSOP | tape & reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET

| Rev | Table | Page | Description of Change | Date |
|-----|-------|----------|--|----------|
| A | T10 | 15 17 | Updated datasheet's header/footer with IDT from ICS. Removed ICS prefix from Part/Order Number column. Added Contact Page. | 12/14/10 |
| A | T10 | 15 | Ordering Information - removed leaded devices, PDN CQ-13-02 Updated data sheet format | 2/20/15 |
| | | | | |

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