General Description

The 8422002I-07 is a 2 output LVHSTL Synthesizer optimized to generate Fibre Channel reference clock frequencies and is a member of the family of high performance clock solutions from IDT. Using a 26.5625MHz 18pF parallel resonant crystal, the following frequencies can be generated based on the 2 frequency select pins (F_SEL[1:0]): 212.5MHz, 187.5MHz, 159.375MHz, 106.25MHz and 53.125MHz. The 8422002I-07 uses IDT's 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Fibre Channel jitter requirements. The 8422002I-07 is packaged in a 20-pin TSSOP, EPad package.

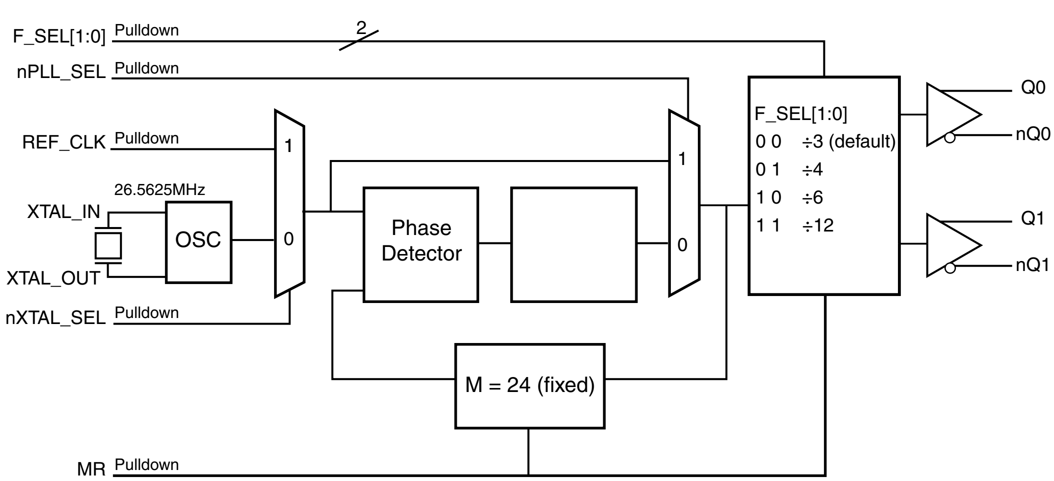
Features

- Two LVHSTL outputs (V_{OH_max} = 1.2V)
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- Supports the following output frequencies: 212.5MHz, 187.5MHz, 159.375MHz, 106.25MHz, 53.125MHz
- VCO range: 560MHz - 680MHz
- RMS phase jitter @ 212.5MHz, using a 25MHz crystal (637kHz - 10MHz): 0.59ps (typical) design target
- Power supply modes:
  Core/Output
  3.3V/1.8V
  2.5V/1.8V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

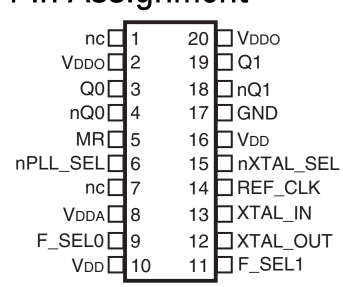
Frequency Select Function Table

Inputs				N Div. Value	M/N Div. Value	Output Frequency (MHz)
Input Frequency (MHz)	F_SEL1	F_SEL0	M Div. Value			
26.5625	0 (default)	0 (default)	24	3	8	212.5
26.5625	0	1	24	4	6	159.375
26.5625	1	0	24	6	4	106.25
26.5625	1	1	24	12	2	53.125
23.4375	0 (default)	0 (default)	24	3	8	187.5

Block Diagram



Pin Assignment



422002I-07
20-Lead TSSOP, EPad
4.4mm x 6.5mm x 0.90mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 7	nc	Unused		No connect.
2, 20	V_{DDO}	Power		Output supply pins.
3, 4	Q0, nQ0	Output		Differential output pair. LVHSTL interface levels.
5	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
6	nPLL_SEL	Input	Pulldown	PLL select control. When LOW, the selected reference clock is frequency-multiplied by the PLL. When HIGH, the PLL is bypassed and the selected reference clock is routed directly to the output dividers. LVCMOS/LVTTL interface levels.
8	V_{DDA}	Power		Analog supply pin.
9, 11	F_SEL0, F_SEL1	Input	Pulldown	Frequency select pins. LVCMOS/LVTTL interface levels.
10, 16	V_{DD}	Power		Core supply pins.
12, 13	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
14	REF_CLK	Input	Pulldown	Single-ended reference clock input. LVCMOS/LVTTL interface levels.
15	nXTAL_SEL	Input	Pulldown	Selects between crystal or REF_CLK inputs as the PLL Reference source. Selects XTAL inputs when LOW. Selects REF_CLK when HIGH. LVCMOS/LVTTL interface levels.
17	GND	Power		Power supply ground.
18, 19	nQ1, Q1	Output		Differential output pair. LVHSTL interface levels.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	33.1°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ±0.2V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.10	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Core Supply Current				112	mA
I_{DDA}	Analog Supply Current				10	mA
I_{DDO}	Output Supply Current	No Load			1	mA

Table 3B. Power Supply DC Characteristics, V_{DD} = 2.5V ± 5%, V_{DDO} = 1.8V ±0.2V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.10	2.5	V_{DD}	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Core Supply Current				106	mA
I_{DDA}	Analog Supply Current				10	mA
I_{DDO}	Output Supply Current	No Load			1	mA

Table 3C. LVCMOS/LVTTL DC Characteristics, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	REF_CLK, MR, F_SEL[0:1], nPLL_SEL, nXTAL_SEL	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	REF_CLK, MR, F_SEL[0:1], nPLL_SEL, nXTAL_SEL	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA

Table 3D. LVHSTL DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ±0.2V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		0.9		1.2	V
V_{OL}	Output Low Voltage; NOTE 1		0		0.4	V
V_{OX}	Output Crossover Voltage; NOTE 2		0.45		0.80	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.2	V

NOTE 1: Outputs termination with 50Ω to ground.
NOTE 2: Defined with respect to output voltage swing at a given condition.

Table 3E. LVHSTL DC Characteristics, V_{DD} = 2.5V ± 5%, V_{DDO} = 1.8V ±0.2V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		0.9		1.2	V
V_{OL}	Output Low Voltage; NOTE 1		0		0.4	V
V_{OX}	Output Crossover Voltage; NOTE 2		0.50		0.90	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.2	V

NOTE 1: Outputs termination with 50Ω to ground.
NOTE 2: Defined with respect to output voltage swing at a given condition.

Table 4. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		23.33	26.5625	28.33	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

AC Electrical Characteristics

Table 5A. AC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ±0.2V, T_A = -40°C to 85°C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL[1:0] = 00	186.67		226.66	MHz
		F_SEL[1:0] = 01	140		170	MHz
		F_SEL[1:0] = 10	93.33		113.33	MHz
		F_SEL[1:0] = 11	46.67		56.66	MHz
*t*sk(o)	Output Skew; NOTE 1, 2				35	ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 3	212.5MHz, (637kHz – 10MHz)		0.59		ps
		187.5MHz, (637kHz – 10MHz)		0.53		ps
		159.375MHz, (637kHz – 10MHz)		0.56		ps
		106.25MHz, (1.875MHz – 20MHz)		0.56		ps
		53.125MHz, (637kHz – 10MHz)		0.66		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	275		875	ps
odc	Output Duty Cycle	N ≠ 3	48		52	%
		N = 3	40		60	%

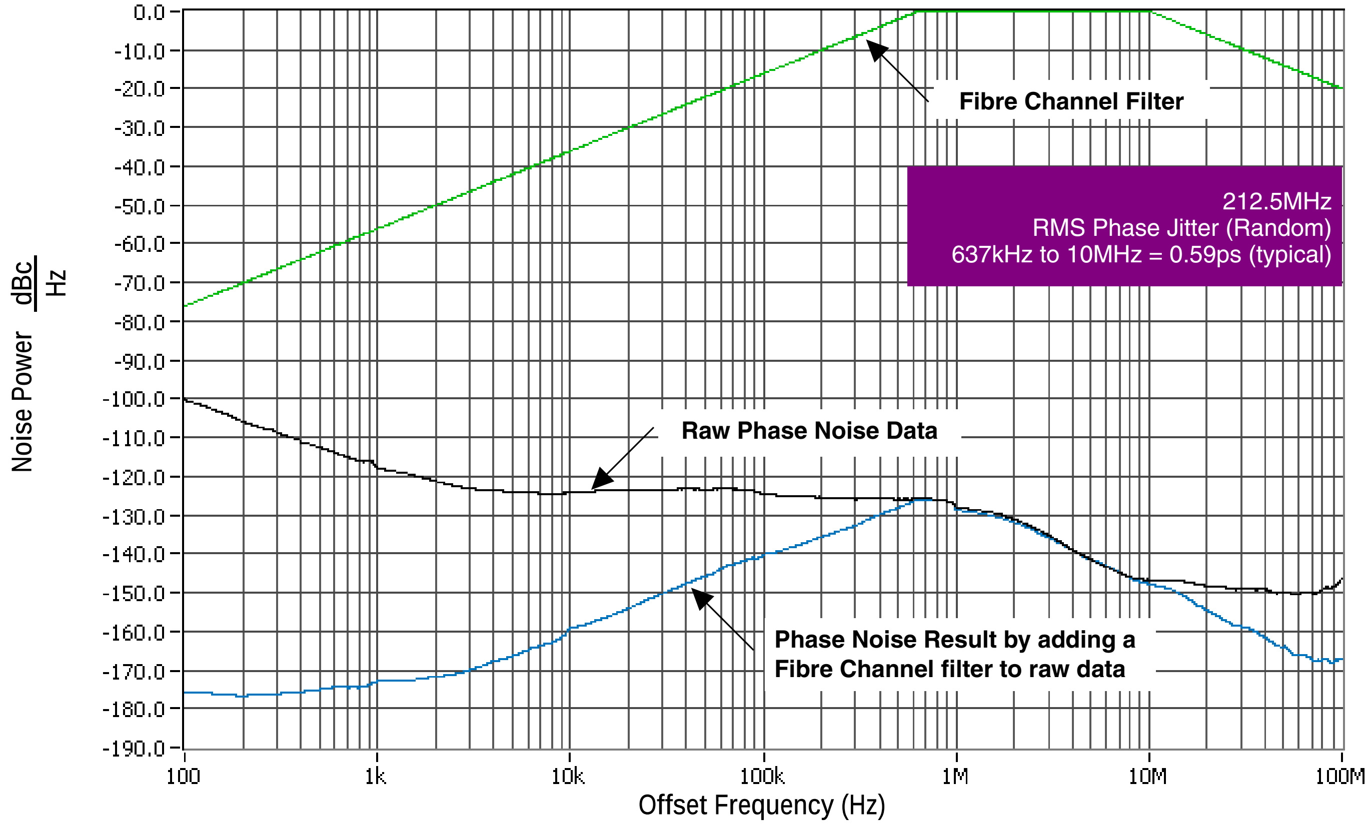
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at V_{DDO}/2.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Please refer to the Phase Noise Plot.

Table 5B. AC Characteristics, V_{DD} = 2.5V ± 5%, V_{DDO} = 1.8V ±0.2V, T_A = -40°C to 85°C

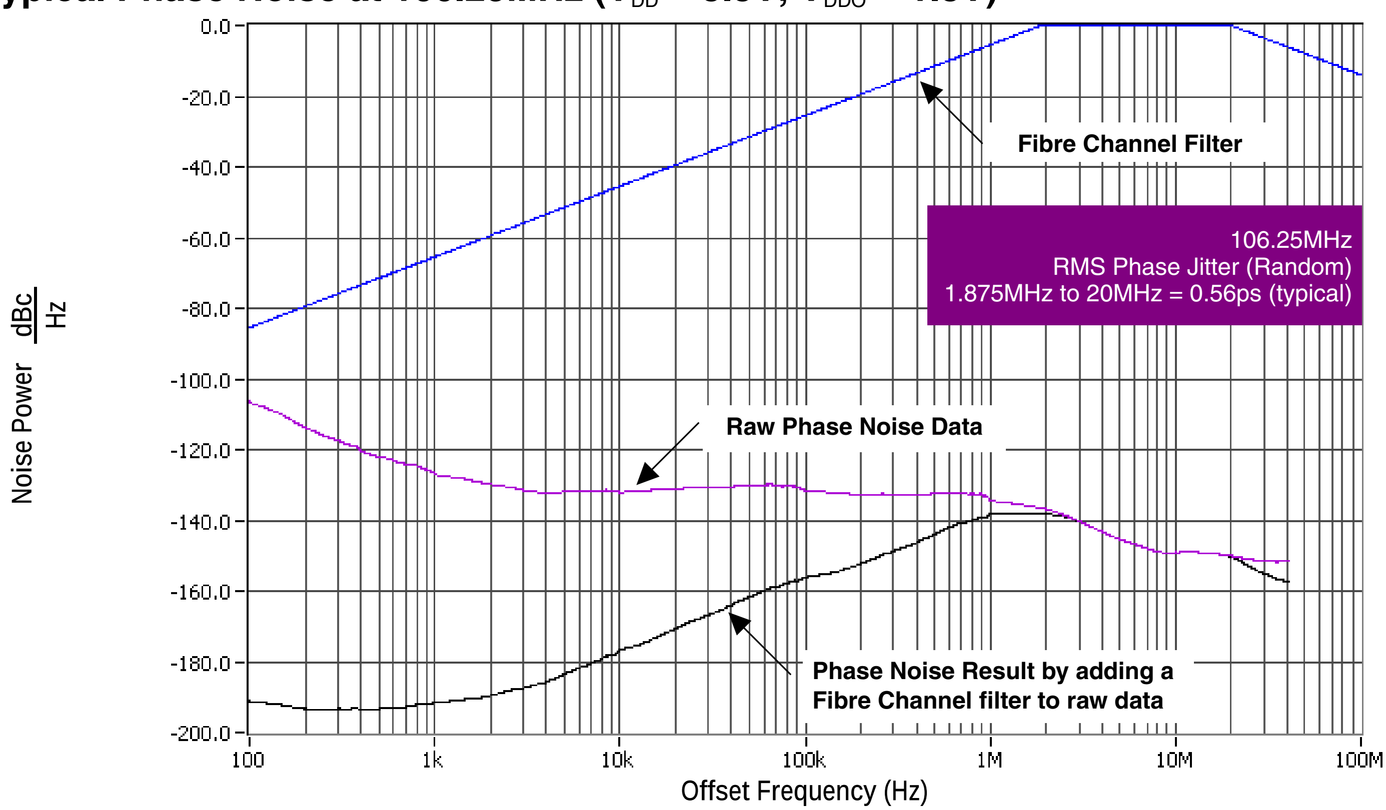
Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL[1:0] = 00	186.67		226.66	MHz
		F_SEL[1:0] = 01	140		170	MHz
		F_SEL[1:0] = 10	93.33		113.33	MHz
		F_SEL[1:0] = 11	46.67		56.66	MHz
*t*sk(o)	Output Skew; NOTE 1, 2				35	ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 3	212.5MHz, (637kHz – 10MHz)		0.60		ps
		187.5MHz, (637kHz – 10MHz)		0.72		ps
		159.375MHz, (637kHz – 10MHz)		0.64		ps
		106.25MHz, (1.875MHz – 20MHz)		0.55		ps
		53.125MHz, (637kHz – 10MHz)		0.68		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		650	ps
odc	Output Duty Cycle	N ≠ 3	48		52	%
		N = 3	40		60	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at V_{DDO}/2.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Please refer to the Phase Noise Plot.

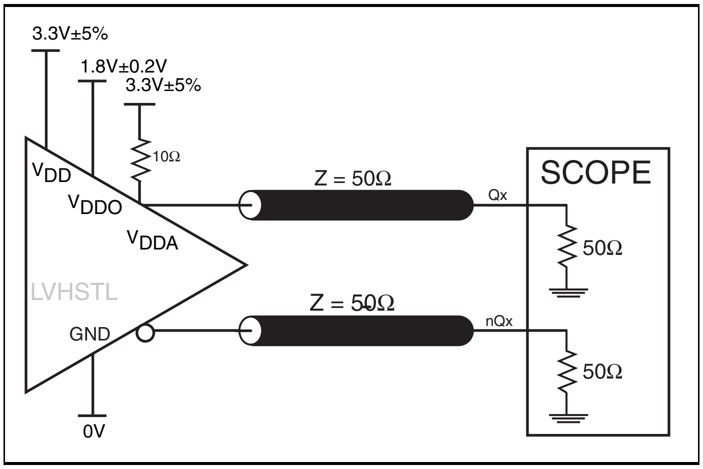
Typical Phase Noise at 212.5MHz (V_{DD} = 3.3V, V_{DDO} = 1.8V)



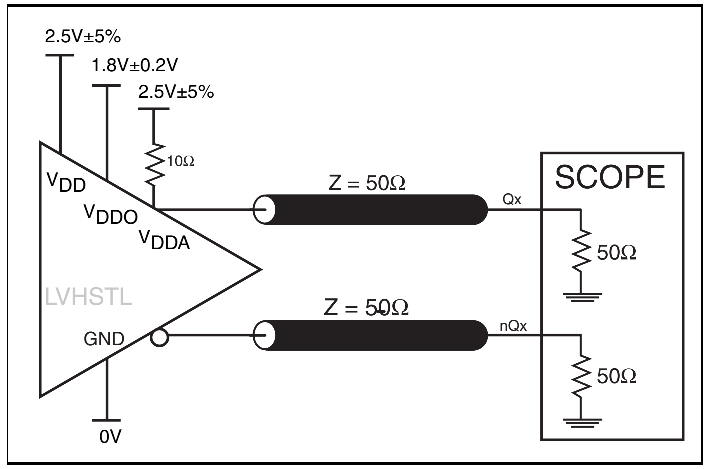
Typical Phase Noise at 106.25MHz (V_{DD} = 3.3V, V_{DDO} = 1.8V)



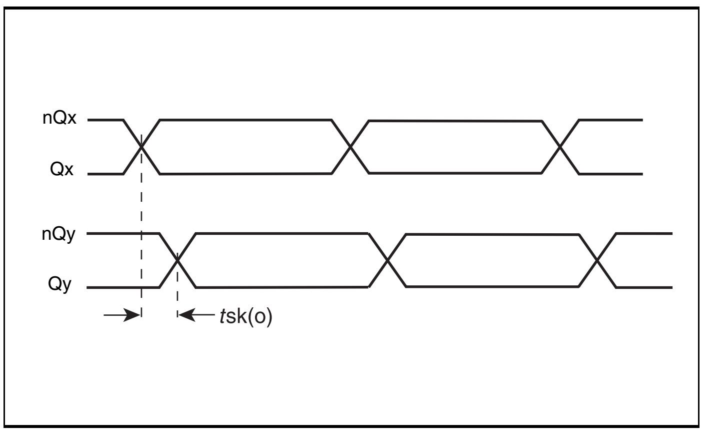
Parameter Measurement Information



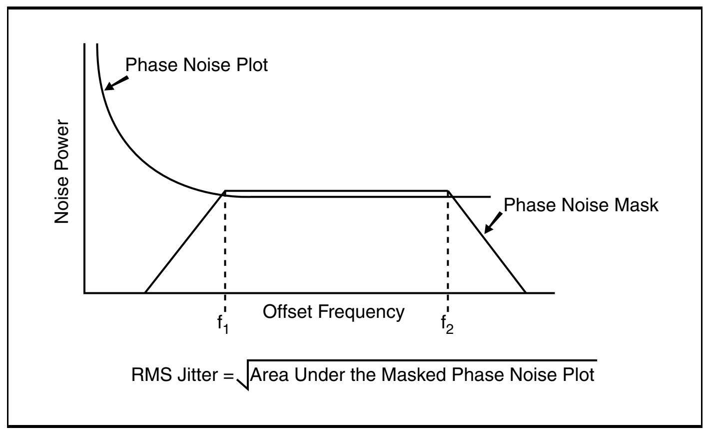
3.3V/1.8V Output Load AC Test Circuit



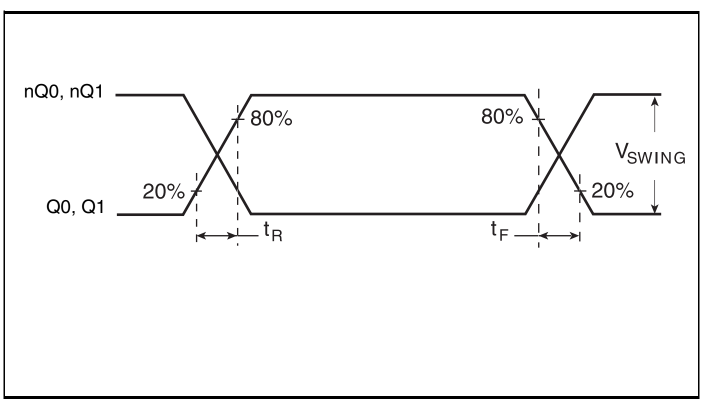
2.5V/1.8V Output Load AC Test Circuit



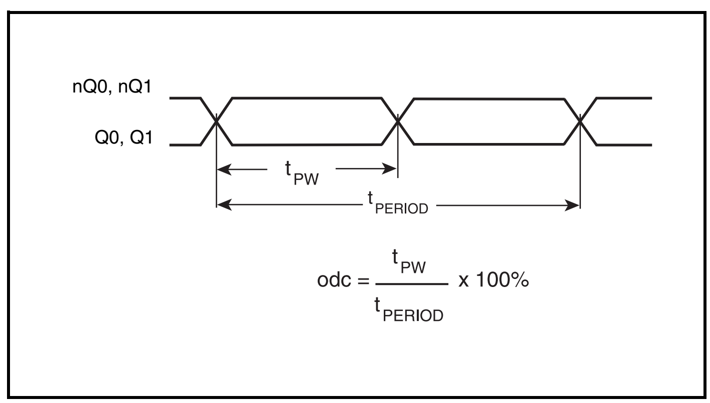
Output Skew



RMS Phase Jitter



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 8422002I-07 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. $V_{DD,}$ V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

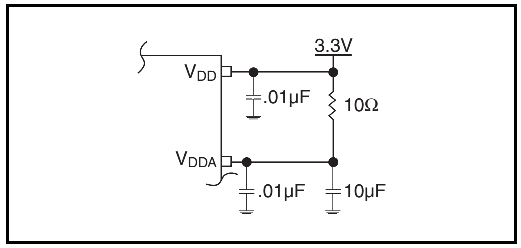


Figure 1. Power Supply Filtering

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_CLK Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

Outputs:

LVHSTL Outputs

All unused LVHSTL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Crystal Input Interface

The 8422002I-07 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz 18pF parallel resonant crystal and were chosen to minimize the ppm error.

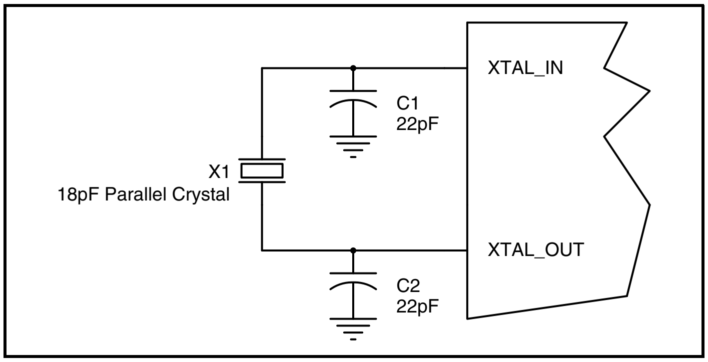


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

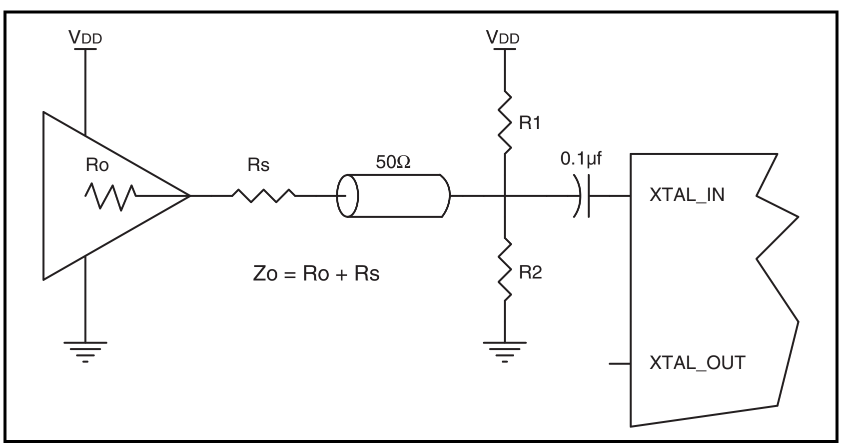


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

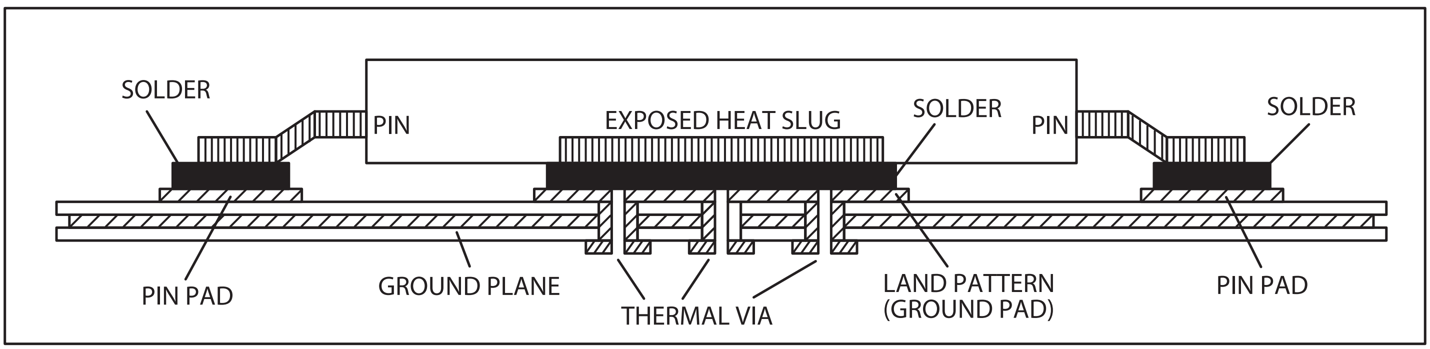


Figure 4. Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)

Schematic Example

Figure 5 shows an example of the 8422002I-07 application schematic. In this example, the device is operated at V_{DD} = 3.3V and V_{DDO} = 1.8V. Both input options are shown. The device can either be driven using a quartz crystal or a 3.3V LVCMOS signal. The C1= 22pF and C2 = 22pF are recommended for frequency accuracy. For different board layouts, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. The LVHSTL output driver termination examples are shown in this schematic. The decoupling capacitors should be located as close as possible to the power pin.

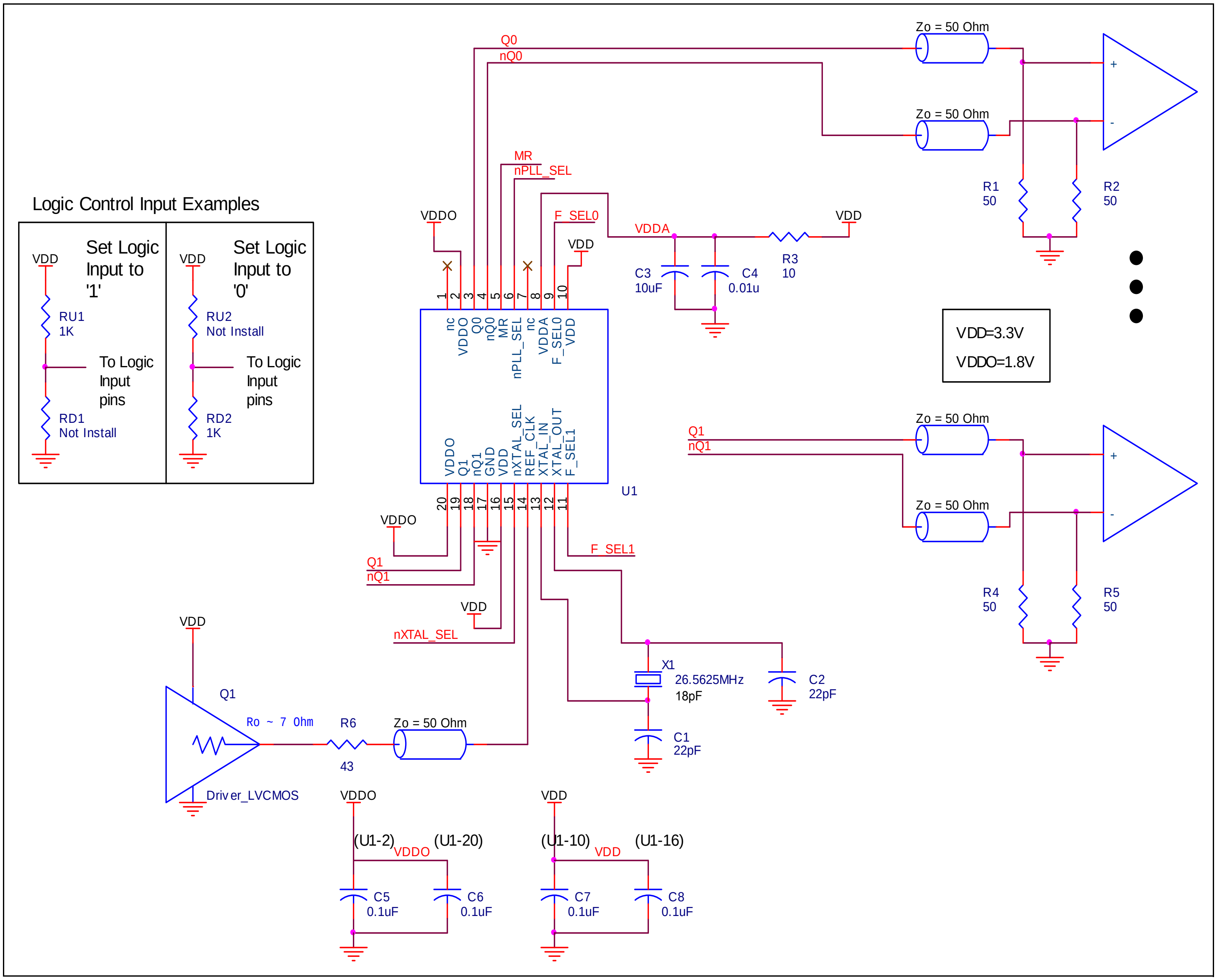


Figure 5. 8422002I-07 LVHSTL Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 8422002I-07.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8422002I-07 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX})$ = 3.465V * (112mA + 10mA) = **422.73mW**
- Power $(outputs)_{MAX}$ = **32mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 x 32mW = **64mW**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 422.73mW + 64mW = **486.73mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 33.1°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.487W * 33.1°C/W = 101.1°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 20 Lead TSSOP, EPad Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	33.1°C/W	26.6°C/W	25.1°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVHSTL output driver circuit and termination are shown in *Figure 6.*

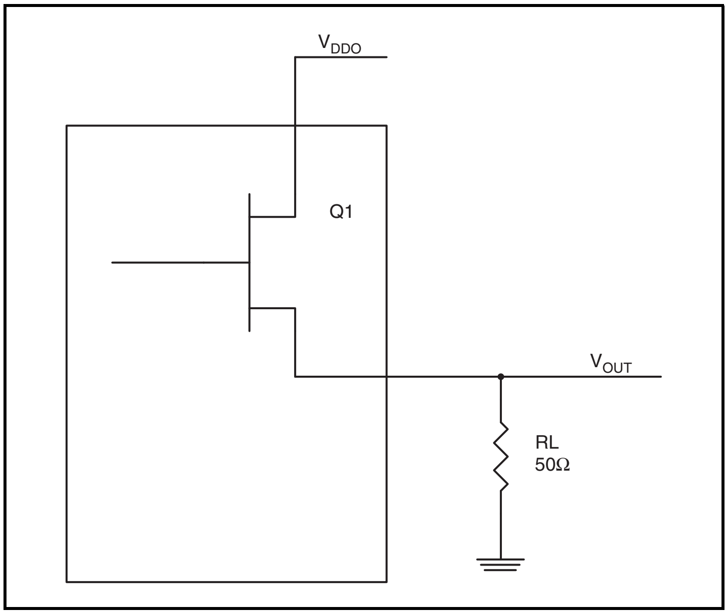


Figure 6. LVHSTL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = (V_{OH\_MAX} / R_L) * (V_{DDO\_MAX} - V_{OH\_MAX})$

$Pd\_L = (V_{OL\_MAX} / R_L) * (V_{DDO\_MAX} - V_{OL\_MAX})$

Pd_H = (1.2V/50Ω) * (2V – 1.2V) = **19.2mW**

Pd_L = (0.4V/50Ω) * (2V – 0.4V) = **12.8mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **32mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 20 Lead TSSOP, EPad

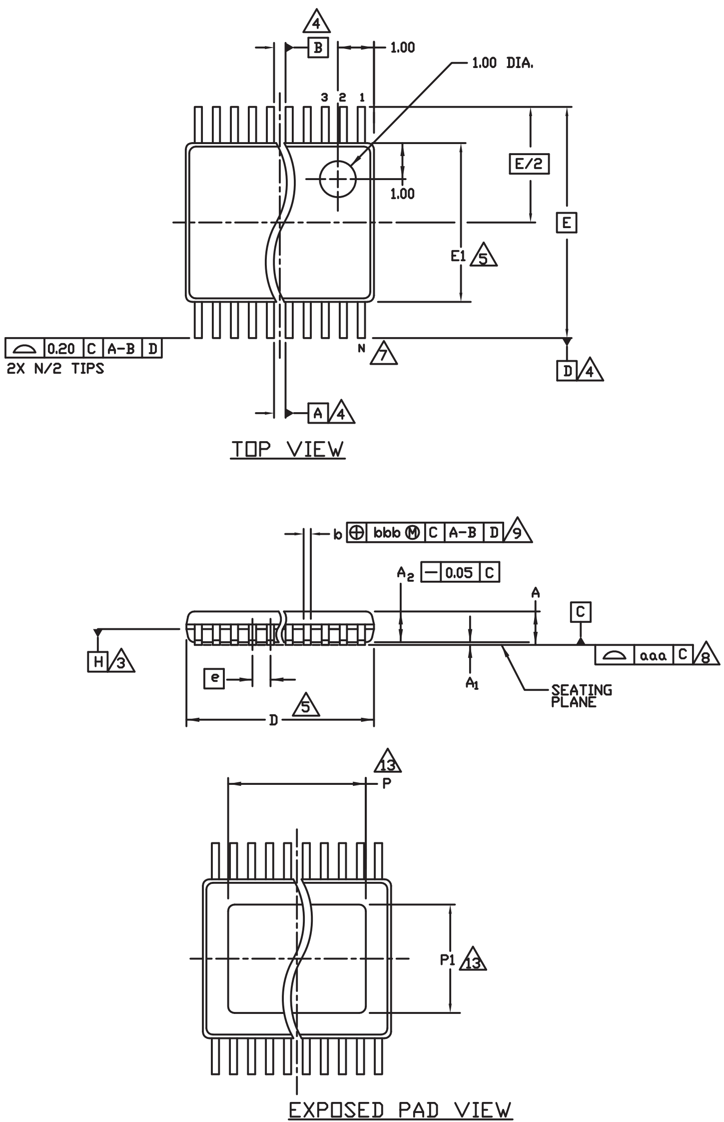
θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	33.1°C/W	26.6°C/W	25.1°C/W

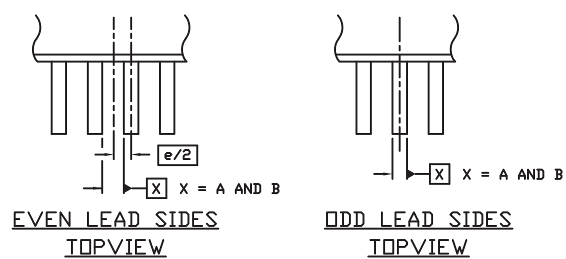
Transistor Count

The transistor count for 8422002I-07 is: 2951

Package Outline and Package Dimensions

Package Outline - G Suffix for 20 Lead TSSOP, EPad





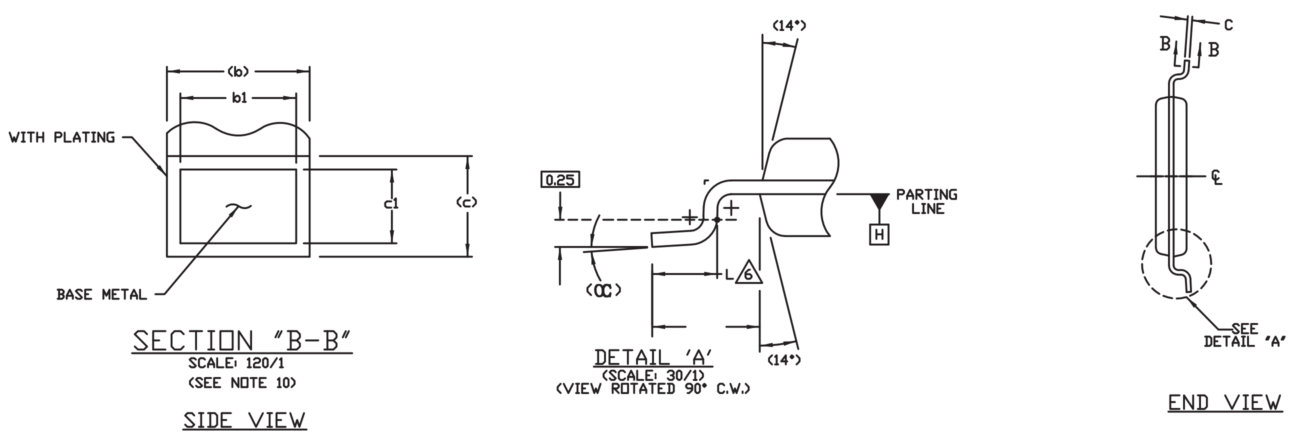


Table 8. Package Dimensions for 20 Lead TSSOP, EPad

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	20	
A		1.10
A1	0.05	0.15
A2	0.85	0.95
b	0.19	0.30
b1	0.19	0.25
c	0.09	0.20
c1	0.09	0.16
D	6.40	6.60
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.50	0.70
P		4.2
P1		3.0
α	0°	8°
aaa		0.076
bbb	0.10	

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8422002AGI-07LF	ICS2002AI07L	“Lead-Free” 20 Lead TSSOP, E-Pad	Tube	-40°C to 85°C
8422002AGI-07LFT	ICS2002AI07L	“Lead-Free” 20 Lead TSSO, E-Pad	Tape & Reel	-40°C to 85°C

Revision History

Revision Date	Description of Change
January 28,2016	▪ Removed ICS from the part numbers where needed. ▪ General Description - removed the ICS chip and HiPerClockS. ▪ Features section - remove reference to leaded package. ▪ Ordering Information - removed quantity from tape and reel. Deleted LF note below table. ▪ Updated header and footer.

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