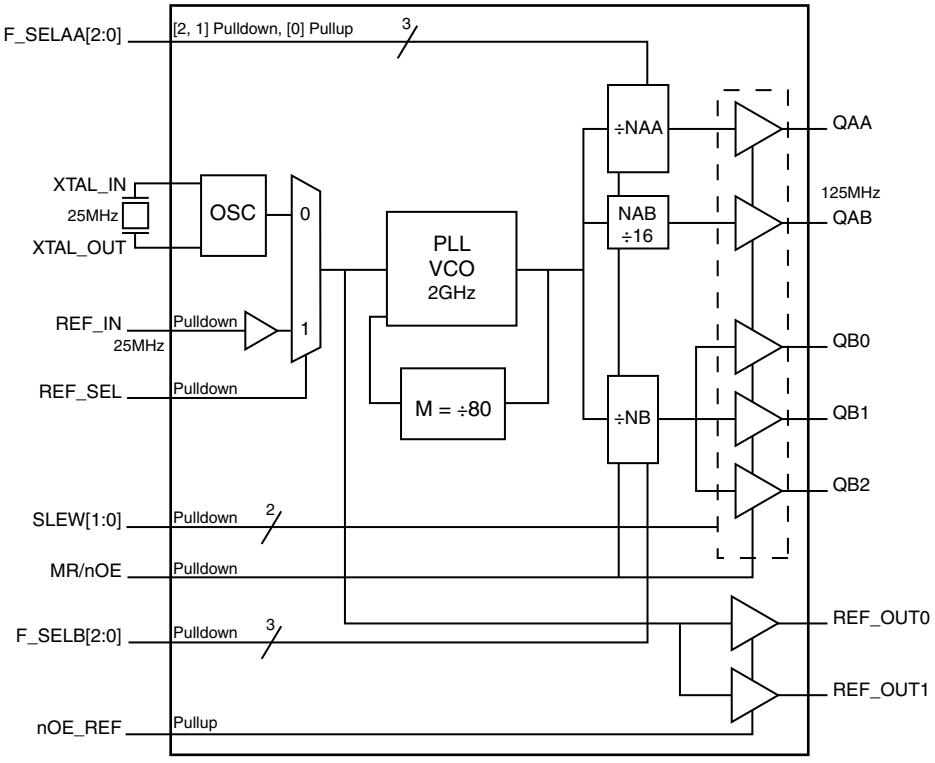
General Description

The 840S07I is a seven output LVCMOS/LVTTL Frequency Synthesizer accepting crystal or single-ended reference clock inputs. The 840S07I uses a 25MHz parallel resonant crystal to generate 33.33MHz – 166.67MHz clock signals, replacing solutions requiring multiple oscillator and fanout buffer solutions. The device supports output slew rate control with two slew select pins (SLEW[1:0]). The VCO operates at a frequency of 2GHz. The device has 3 output banks, output QAA with one 33.33MHz – 166.67MHz LVCMOS/LVTTL output, output QAB with one 125MHz LVCMOS/LVTTL output and Bank B with three 33.33MHz – 166.67MHz LVCMOS/LVTTL outputs.

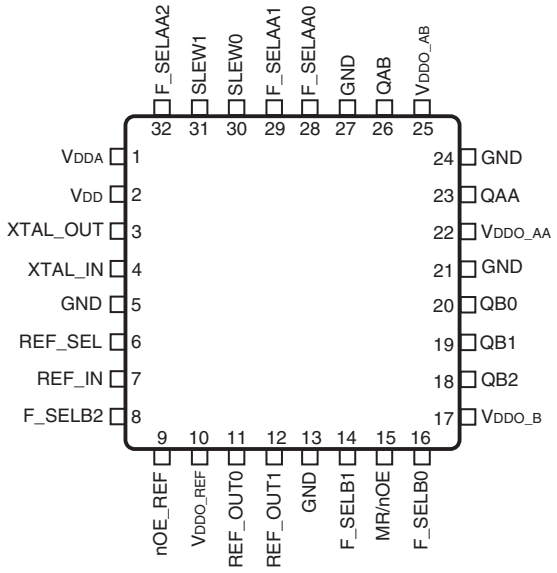
Output QAA and Bank B have their own dedicated frequency select pins and can be independently set for the frequencies mentioned above. Designed for networking and industrial applications, the 840S07I can also drive the high-speed clock inputs of communication processors, DSPs, switches and bridges.

Features

- Five single-ended LVCMOS/LVTTL outputs
- Two REF_OUT LVCMOS/LVTTL clock outputs
- Selectable crystal oscillator interface, 25MHz, 18pF parallel resonant crystal or LVCMOS/LVTTL single-ended reference input
- Supports the following output frequencies:
  Output QAA/Bank B: 33.33MHz, 50MHz, 66.67MHz, 83.33MHz, 100MHz, 125MHz, 133.33MHz and 166.67MHz
  Output QAB: 125MHz
- VCO frequency: 2GHz
- Slew rate control
- Voltage supply modes:
  Core/Output
  3.3V/3.3V
  3.3V/2.5V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package



Pin Assignment



840S07I

32-Lead TQFP, E-Pad
7mm x 7mm x1mm package body
Y Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{DDA}	Power		Analog supply pin.
2	V_{DD}	Power		Core supply pin.
3, 4	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
5, 13, 21, 24, 27	GND	Power		Power supply ground.
6	REF_SEL	Input	Pulldown	Reference select pin. When HIGH selects REF_IN. When LOW, selects crystal. See Table 3D. LVCMOS/LVTTL interface levels.
7	REF_IN	Input	Pulldown	Single-ended reference clock input. Table 3B. LVCMOS/LVTTL interface levels.
8, 14, 16	F_SELB2, F_SELB1, F_SELB0	Input	Pulldown	Frequency select pins for Bank B outputs. See Table 3C. LVCMOS/LVTTL interface levels.
9	nOE_REF	Input	Pullup	Active low REF_OUT enable/disable pin. See Table 3F. LVCMOS/LVTTL interface levels.
10	V_{DDO_REF}	Power		Output supply pin for REF_OUTx clock outputs.
11, 12	REF_OUT0, REF_OUT1	Output		Single-ended reference clock outputs. LVCMOS/LVTTL interface levels.
15	MR/nOE	Input	Pulldown	Active HIGH Master Reset. Active LOW output enable. When logic HIGH, the internal dividers are reset and the outputs are in high impedance (HI-Z). When logic LOW, the internal dividers and the outputs are enabled. See Table 3E. LVCMOS/LVTTL interface levels.
17	V_{DDO_B}	Power		Output supply pin for QBx outputs.
18, 19, 20	QB2, QB1, QB0	Output		Single-ended Bank QBx clock outputs. LVCMOS/ LVTTL interface levels.
22	V_{DDO_AA}	Power		Output supply pin for QAA output.
23	QAA	Output		Single-ended QAA clock output. LVCMOS/LVTTL interface levels.
25	V_{DDO_AB}	Power		Output supply pin for QAB output.
26	QAB	Output		Single-ended QAB clock output. LVCMOS/LVTTL interface levels.
28	F_SELAA0	Input	Pullup	Frequency select pin for QAA output. See Table 3A. LVCMOS/LVTTL interface levels.
29, 32	F_SELAA1, F_SELAA2	Input	Pulldown	Frequency select pins for QAA output. See Table 3A. LVCMOS/LVTTL interface levels.
30, 31	SLEW0, SLEW1	Input	Pulldown	Slew rate select pins for LVCMOS/LVTTL clock output. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				2		pF
C_{PD}	Power Dissipation Capacitance		SLEW[1:0] = 00 V_{DD}, V_{DDO_REF}, V_{DDO_AA}, V_{DDO_AB}, V_{DDO_B} = 3.465V		4		pF
			SLEW[1:0] = 11 V_{DD}, V_{DDO_REF}, V_{DDO_AA}, V_{DDO_AB}, V_{DDO_B} = 3.465V		10		pF
			SLEW[1:0] = 00, V_{DD} = 3.465V, V_{DDO_REF}, V_{DDO_AA}, V_{DDO_AB}, V_{DDO_B} = 2.625V		2.65		pF
			SLEW[1:0] = 11, V_{DD} = 3.465V, V_{DDO_REF}, V_{DDO_AA}, V_{DDO_AB}, V_{DDO_B} = 2.625V		3		pF
R_{PULLUP}	Input Pullup Resistor				51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{OUT}	Output Impedance	QAA, QAB, QBx	V_{DDO_AA}, V_{DDO_AB}, V_{DDO_B} = 3.3V		26		Ω
			V_{DDO_AA}, V_{DDO_AB}, V_{DDO_B} = 2.5V		28		Ω
		REF_OUTx	V_{DDO_REF} = 3.3V		35		Ω
			V_{DDO_REF} = 2.5V		34		Ω

Function Tables

Table 3A. Output QAA Frequency Select Function Table

Inputs				Output Frequencies
F_SELAA2	F_SELAA1	F_SELAA0	NAA Divider Value	QAA (MHz)
L	L	L	60	33.33
L	L	H	40	50 (default)
L	H	L	30	66.67
L	H	H	24	83.33
H	L	L	20	100
H	L	H	16	125
H	H	L	15	133.33
H	H	H	12	166.67

NOTE: Using 25MHz reference.

Table 3B. Output QAB Frequency Select Function Table

Inputs			Output Frequency
XTAL_IN, REF_IN (MHz)	M Divider Value	NAB Divider Value	QAB (MHz)
25	80	16	125

Table 3C. Bank QB Frequency Select Function Table

Inputs				Output Frequencies
F_SELB2	**F_SELB1**	**F_SELB0**	**NB Divider Value**	**QB[0:2] (MHz)**
L	L	L	60	33.33 (default)
L	L	H	40	50
L	H	L	30	66.67
L	H	H	24	83.33
H	L	L	20	100
H	L	H	16	125
H	H	L	15	133.33
H	H	H	12	166.67

NOTE: Using 25MHz reference.

Table 3D. REF_SEL Function Table

Input	
REF_SEL	**Input Reference**
0 (default)	XTAL_IN
1	REF_IN

Table 3E. MR/nOE Function Table

Input	
MR/nOE	**Function**
0 (default)	Output Enabled
1	Device reset, outputs disabled (LOW)

NOTE: The device requires a reset signal after power-up to function properly.

Table 3F. nOE_REF Function Table

Input	
nOE_REF	**Function**
0	REF_OUT [1:0] enabled
1 (default)	REF_OUT [1:0] disabled (LOW)

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to V_{DD} -0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	36.2°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO\_REF} = V_{DDO\_AA} = V_{DDO\_AB} = V_{DDO\_B} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.23	3.3	V_{DD}	V
V_{DDO_X}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current	SLEW[1:0] = 11, QAA = QB[0:2] = 166.67MHz, QAB = 125MHz, REF_OUT[0:1] = 25MHz, Outputs Not Loaded			180	mA
I_{DDA}	Analog Supply Current				23	mA
I_{DDO_X}	Output Supply Current				71	mA

NOTE: V_{DDO_X} denotes V_{DDO_AA}, V_{DDO_AB}, V_{DDO_B}, V_{DDO_REF}.
NOTE: I_{DDO_X} denotes $I_{DDO\_AA} + I_{DDO\_AB} + I_{DDO\_B} + I_{DDO\_REF}$.

Table 4B. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO\_REF} = V_{DDO\_AA} = V_{DDO\_AB} = V_{DDO\_B} = 2.5V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.23	3.3	V_{DD}	V
V_{DDO_X}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current	SLEW[1:0] = 11, QAA = QB[0:2] = 166.67MHz, QAB = 125MHz, REF_OUT[0:1] = 25MHz, Outputs Not Loaded			180	mA
I_{DDA}	Analog Supply Current				23	mA
I_{DDO_X}	Output Supply Current				21	mA

NOTE: V_{DDO_X} denotes V_{DDO_AA}, V_{DDO_AB}, V_{DDO_B}, V_{DDO_REF}.
NOTE: I_{DDO_X} denotes $I_{DDO\_AA} + I_{DDO\_AB} + I_{DDO\_B} + I_{DDO\_REF}$.

Table 4C. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.465V	2.2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.465V	-0.3		0.8	V
I_{IH}	Input High Current	nOE_REF, F_SELAA0	V_{DD} = V_{IN} = 3.465V			10	µA
		F_SELB[2:0], F_SELAA[1:2], REF_IN, REF_SEL, SLEW[1:0], MR/nOE	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	nOE_REF, F_SELAA0	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		F_SELB[2:0], F_SELAA[1:2], REF_IN, REF_SEL, SLEW[1:0], MR/nOE	V_{DD} = 3.465V, V_{IN} = 0V	-10			µA
V_{OH}	Output High Voltage; NOTE 1	QAA, QB[0:2] , REF_OUT[0:1]	SLEW[1:0] = 00, QAA, QB[0:2] = 33.33MHz, REF_OUT[0:1] = 25MHz	2.45			V
				1.8			V
V_{OL}	Output Low Voltage; NOTE 1	QAA, QB[0:2] , REF_OUT[0:1]	SLEW[1:0] = 00, QAA, QB[0:2] = 33.33MHz, REF_OUT[0:1] = 25MHz			0.8	V
						0.65	V

NOTE: V_{DDO_X} denotes V_{DDO_AA}, V_{DDO_AB}, V_{DDO_B}, V_{DDO_REF}.
NOTE 1: Outputs terminated with 50Ω to V_{DDO_X}/2. See Parameter Measurement Information Section, *Load Test Circuit diagrams.*

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

NOTE: Characterized using an 18pF parallel resonant crystal.

AC Electrical Characteristics

Table 6A. AC Characteristics, $V_{DD} = V_{DDO\_REF} = V_{DDO\_AA} = V_{DDO\_AB} = V_{DDO\_B} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	QAB			125		MHz
		QAA, QB[0:2]		33.33		166.67	MHz
*t*sk(o)	Output Skew; NOTE 1, 2		f_{OUT} = 125MHz; SLEW[1:0] = 00			485	ps
*t*sk(b)	Bank Skew; NOTE 2, 3	QB[0:2]	f_{OUT} = 125MHz; SLEW[1:0] = 00			110	ps
tjit(per)	Period Jitter, RMS; NOTE 4		f_{OUT} = 125MHz; SLEW[1:0] = 00			7	ps
tjit(cc)	Cycle-to-Cycle Jitter; NOTE 2		f_{OUT} = 125MHz; SLEW[1:0] = 00			90	ps
t_{SLEW}	Slew Rate, Single-ended Output Clock; NOTE 5	QAA	SLEW[1:0] = 00, Rise/Fall Time: 20% to 80%		1.93	3.0	V/ns
		QAB			2.84	4.75	V/ns
		QB[0:2]			2.59	4.25	V/ns
		QAA	SLEW[1:0] = 01, Rise/Fall Time: 20% to 80%		1.76	2.75	V/ns
		QAB			2.45	4.25	V/ns
		QB[0:2]			2.23	3.75	V/ns
		QAA	SLEW[1:0] = 10, Rise/Fall Time: 20% to 80%		1.58	2.50	V/ns
		QAB			1.88	3.0	V/ns
		QB[0:2]			1.80	2.95	V/ns
		QAA	SLEW[1:0] = 11, Rise/Fall Time: 20% to 80%		0.98	1.65	V/ns
		QAB			1.03	1.75	V/ns
		QB[0:2]			1.01	1.75	V/ns
t_{LOCK}	PLL Lock Time		SLEW[1:0] = 00			20	ms
odc	Output Duty Cycle		$f_{OUT} \leq$ 125MHz; SLEW[1:0] = 00	47		53	%
			f_{OUT} > 125MHz; SLEW[1:0] = 00	45		55	%

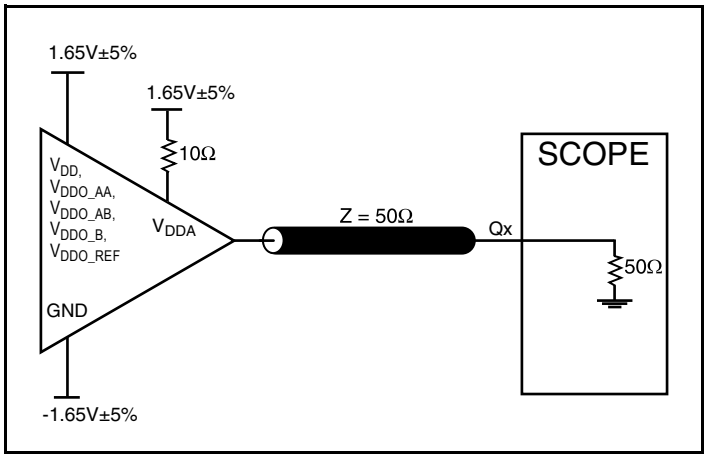
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. Device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO\_X}/2$.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.
NOTE 4: Jitter performance using XTAL inputs.
NOTE 5: A slew rate of 2V/ns or greater should be selected for output frequencies of 100MHz and higher.

Table 6B. AC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO_REF} = V_{DDO_AA} = V_{DDO_AB} = V_{DDO_B} = 2.5V ± 5%, T_A = -40°C to 85°C

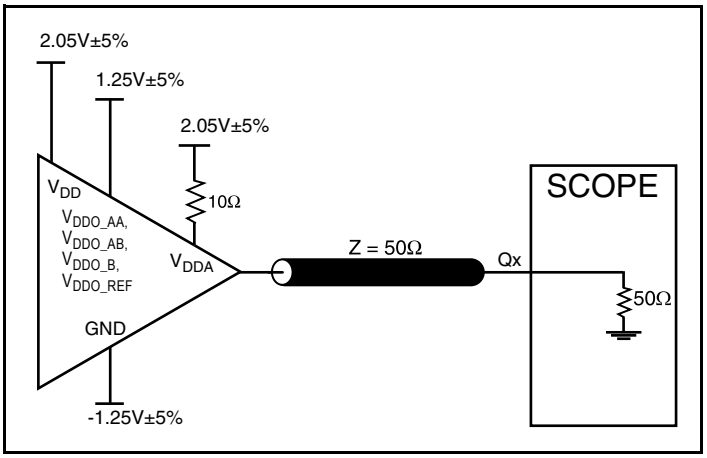
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	QAB			125		MHz
		QAA, QB[0:2]		33.33		166.67	MHz
*t*sk(o)	Output Skew; NOTE 1, 2		f_{OUT} = 125MHz; SLEW[1:0] = 00			435	ps
*t*sk(b)	Bank Skew; NOTE 2, 3	QB[0:2]	f_{OUT} = 125MHz; SLEW[1:0] = 00			115	ps
tjit(per)	Period Jitter, RMS; NOTE 4		f_{OUT} = 125MHz; SLEW[1:0] = 00			12	ps
tjit(cc)	Cycle-to-Cycle Jitter; NOTE 2		f_{OUT} = 125MHz; SLEW[1:0] = 00			96	ps
t_{SLEW}	Slew Rate, Single-ended Output Clocks; NOTE 5	QAA	SLEW[1:0] = 00, Rise/Fall Time: 20% to 80%		1.36	2.15	V/ns
		QAB			1.89	3.25	V/ns
		QB[0:2]			1.81	2.85	V/ns
		QAA	SLEW[1:0] = 01, Rise/Fall Time: 20% to 80%		1.12	1.85	V/ns
		QAB			1.43	2.50	V/ns
		QB[0:2]			1.44	2.50	V/ns
		QAA	SLEW[1:0] = 10, Rise/Fall Time: 20% to 80%		0.88	1.55	V/ns
		QAB			1.06	1.85	V/ns
		QB[0:2]			1.03	1.85	V/ns
		QAA	SLEW[1:0] = 11, Rise/Fall Time: 20% to 80%		0.59	1.15	V/ns
		QAB			0.66	1.15	V/ns
		QB[0:2]			0.61	1.15	V/ns
t_{LOCK}	PLL Lock Time		SLEW[1:0] = 00			25	ms
odc	Output Duty Cycle		$f_{OUT} \leq$ 125MHz; SLEW[1:0] = 00	45		55	%
			f_{OUT} > 125MHz; SLEW[1:0] = 00	43		57	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. Device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO\_X}/2$.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.
NOTE 4: Jitter performance using XTAL inputs.
NOTE 5: A slew rate of 2V/ns or greater should be selected for output frequencies of 100MHz and higher.

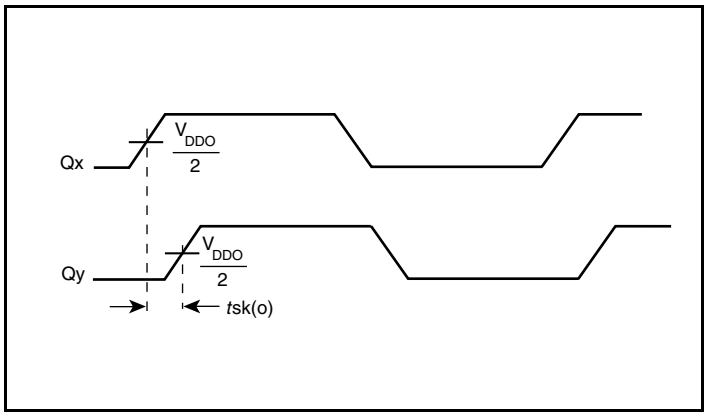
Parameter Measurement Information



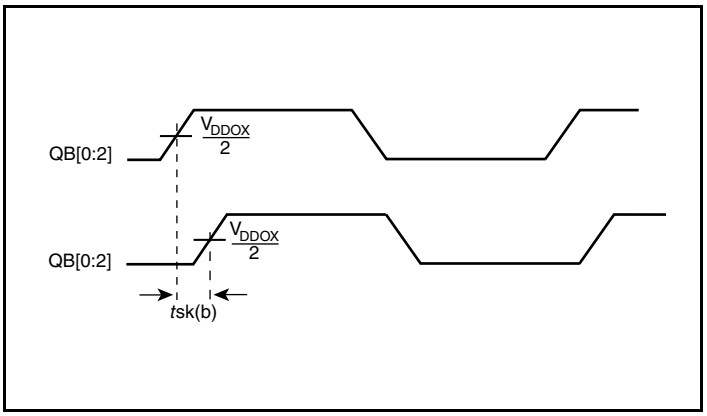
3.3V Core/3.3V LVCMOS Output Load AC Test Circuit



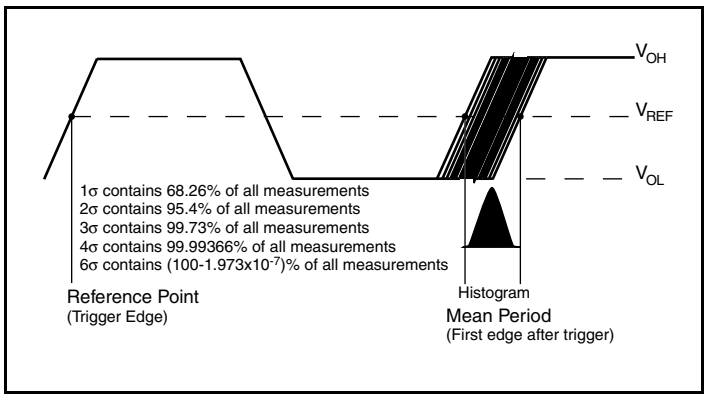
3.3V Core/2.5V LVCMOS Output Load AC Test Circuit



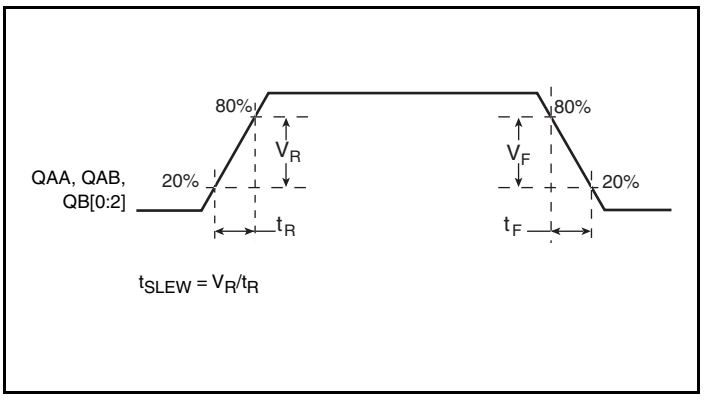
Output Skew



Bank Skew

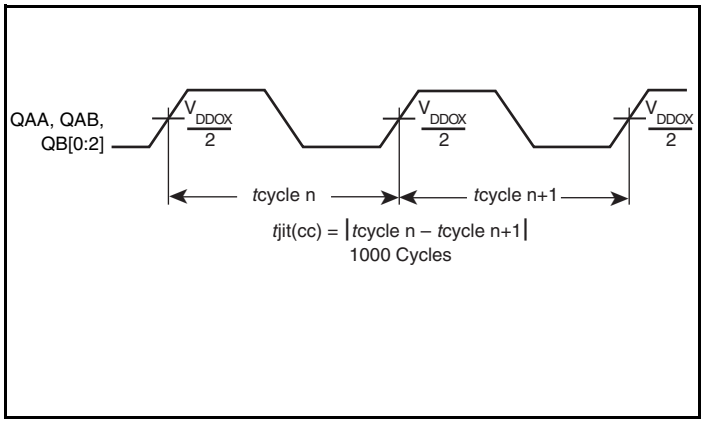


RMS Period Jitter

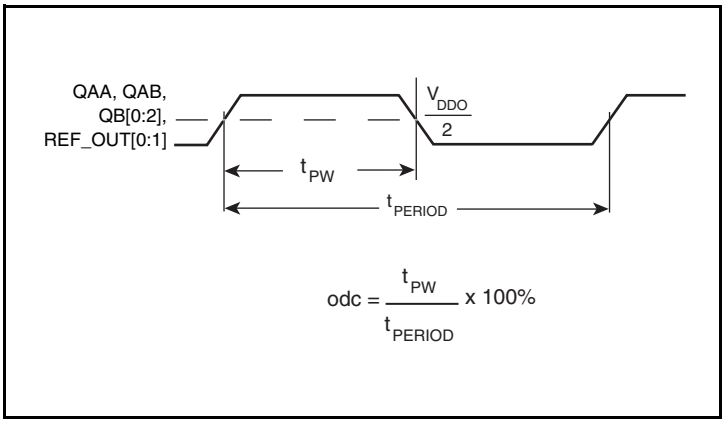


Output Slew Rate

Parameter Measurement Information, continued



Cycle-to-Cycle Jitter



Output Duty Cycle/Pulse Width/Period

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_IN Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_IN to ground.

Outputs:

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 840S07I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA} and V_{DDO_X} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

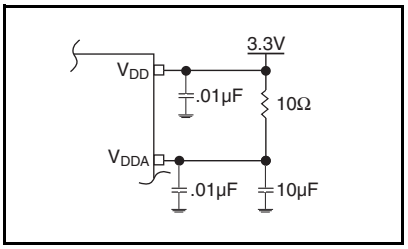


Figure 1. Power Supply Filtering

EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 2.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

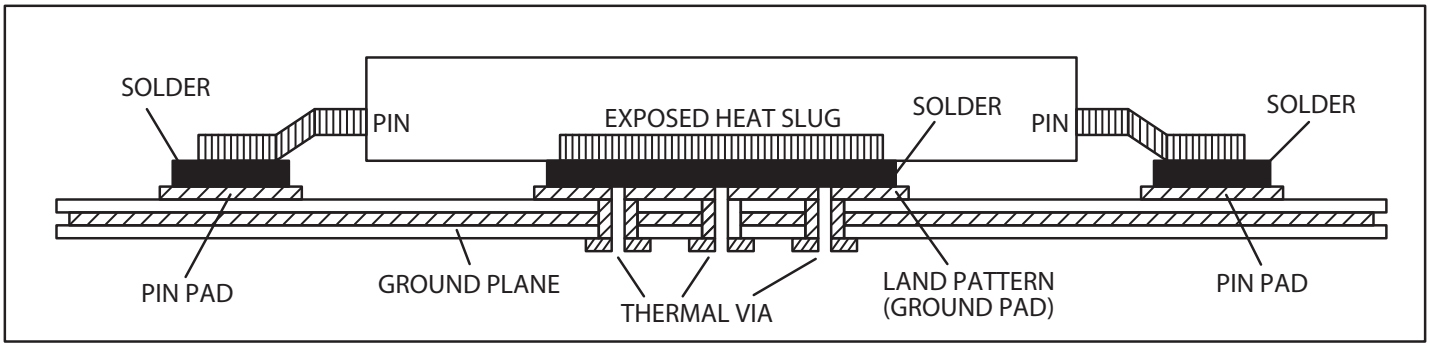


Figure 2. Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)

Crystal Input Interface

The 840S07I has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 3* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

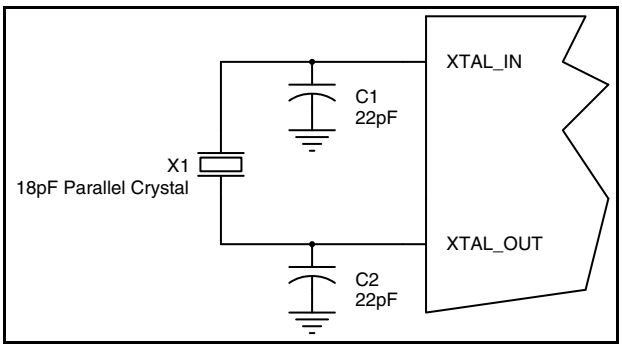


Figure 3. Crystal Input Interface

Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 4A*. The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

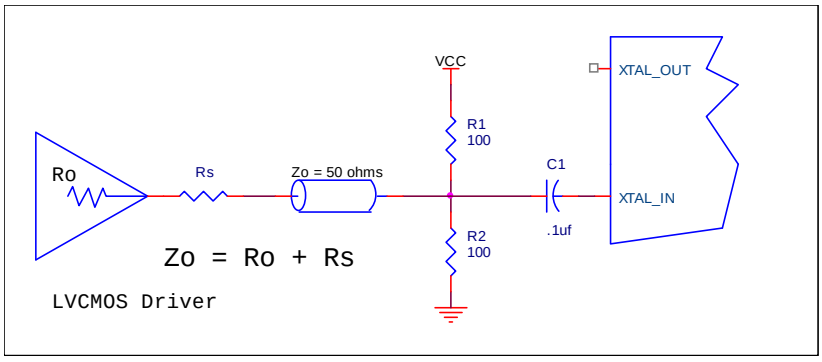


Figure 4A. General Diagram for LVCMOS Driver to XTAL Input Interface

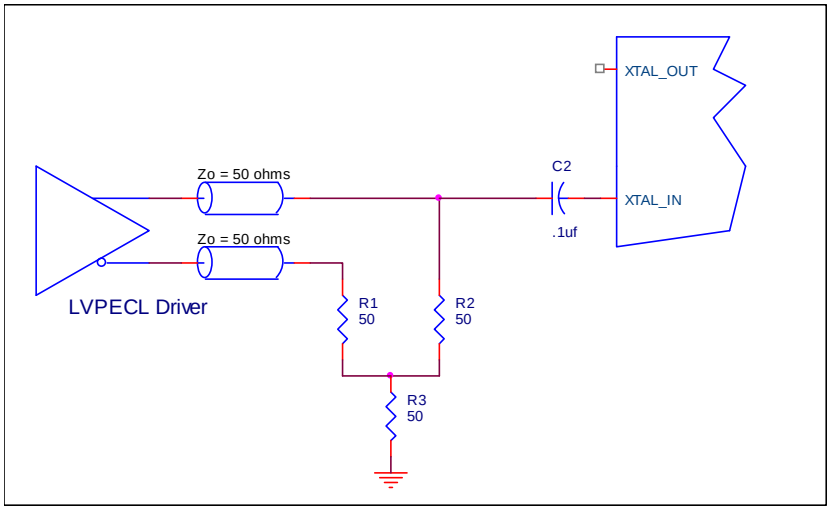


Figure 4B. General Diagram for LVPECL Driver to XTAL Input Interface

Schematic Example

Figure 5 shows an example of the 840S07I application schematic. In this example, the device is operated at V_{DD} = V_{DDO_AA} = V_{CCO_AB} = V_{CCO_B} = = V_{CCO_REF} = 3.3V. The 18pF parallel resonant 25MHz crystal is used. The C1 = 22pF and C2 = 22pF are recommended for frequency accuracy. For different board layouts, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. Two examples of LVCMOS termination are shown in this schematic. The decoupling capacitors should be located as close as possible to the power pin.

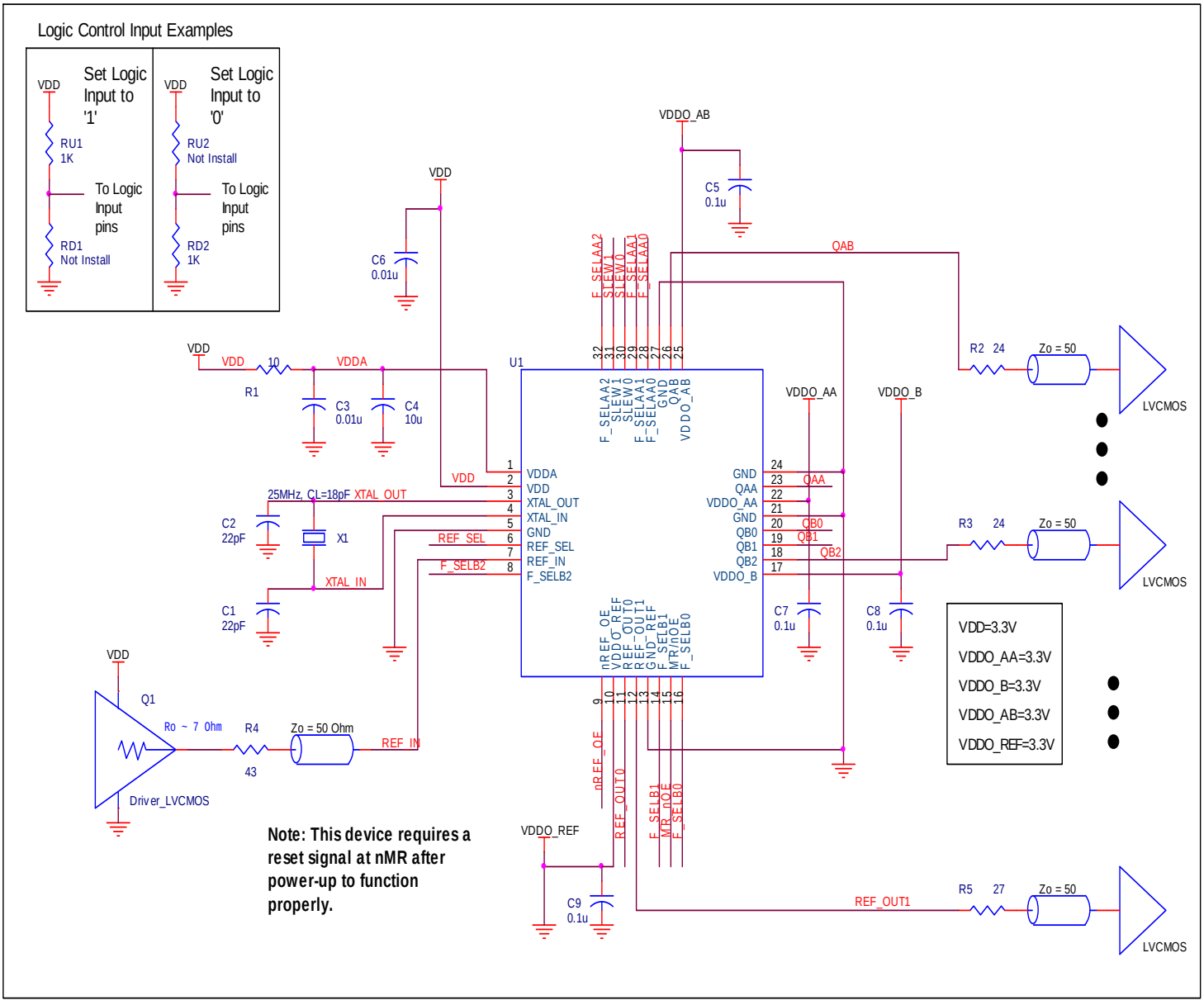


Figure 5. 840S07I Schematic Layout

Power Considerations

This section provides information on power dissipation and junction temperature for the 840S07I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 840S07I is the sum of the core power plus the analog power plus the power dissipation in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

The maximum current at 85°C is as follows:
I_{DD_MAX} = 168.5mA
I_{DDA_MAX} = 20.96mA
I_{DDO_MAX} = 74.11mA

Core Output Power Dissipation

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD} + I_{DDA})$ = 3.465V *(168.5mA + 20.96mA) = **656.51mW**
- Power $(output)_{MAX} = V_{DDO\_MAX} * I_{DDO}$ = 3.465V *74.11mA = **256.80mW**

LVCMOS Output Power Dissipation

- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to $V_{DD}/2$
  Output Current $I_{OUT} = V_{DD\_MAX} / [2 * (50Ω + R_{OUT})]$ = 3.465V / [2 * (50Ω + 35Ω)] = **20.38mA**
- Power Dissipation on the R_{OUT} per LVCMOS output
  Power $(R_{OUT}) = R_{OUT} * (I_{OUT})^2$ = 35Ω * $(20.38mA)^2$ = **14.54mW per output**
- Total Power Dissipation on the R_{OUT}
  Total Power (R_{OUT}) = 14.54mW * 7 = **101.8mW**

- Dynamic Power Dissipation at 25MHz
  Power (25MHz) = C_{PD} * Frequency * $(V_{DDO})^2$ = 10pF * 25MHz * $(3.465V)^2$ = **3mW per output**
  Total Power (25MHz) = 3mW * 2 = **6mW**

- Dynamic Power Dissipation at 166.67MHz
  Power (166.67MHz) = C_{PD} * Frequency * $(V_{DDO})^2$ = 10pF * 166.67MHz * $(3.465V)^2$ = **20mW per output**
  Total Power (166.67MHz) = 20mW * 5 = **100.1mW**

Total Power Dissipation

- **Total Power**
  = Power (core) + Power (output) + Total Power (25MHz + Total Power (166.67MHz)
  = 656.51mW + 256.80mW + 101.8mW + 6.0mW + 100.1mW
  = 1121.15mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 30.6°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.121W *30.6°C/W = 119.3°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 32 Lead TQFP, E-Pad, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	36.2°C/W	30.6°C/W	29.2°C/W

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 32 Lead TQFP, E-Pad

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	36.2°C/W	30.6°C/W	29.2°C/W

Transistor Count

The transistor count for 840S07I is: 2349

Package Outline and Package Dimensions

Package Outline - G Suffix for 32 Lead TQFP, E-Pad

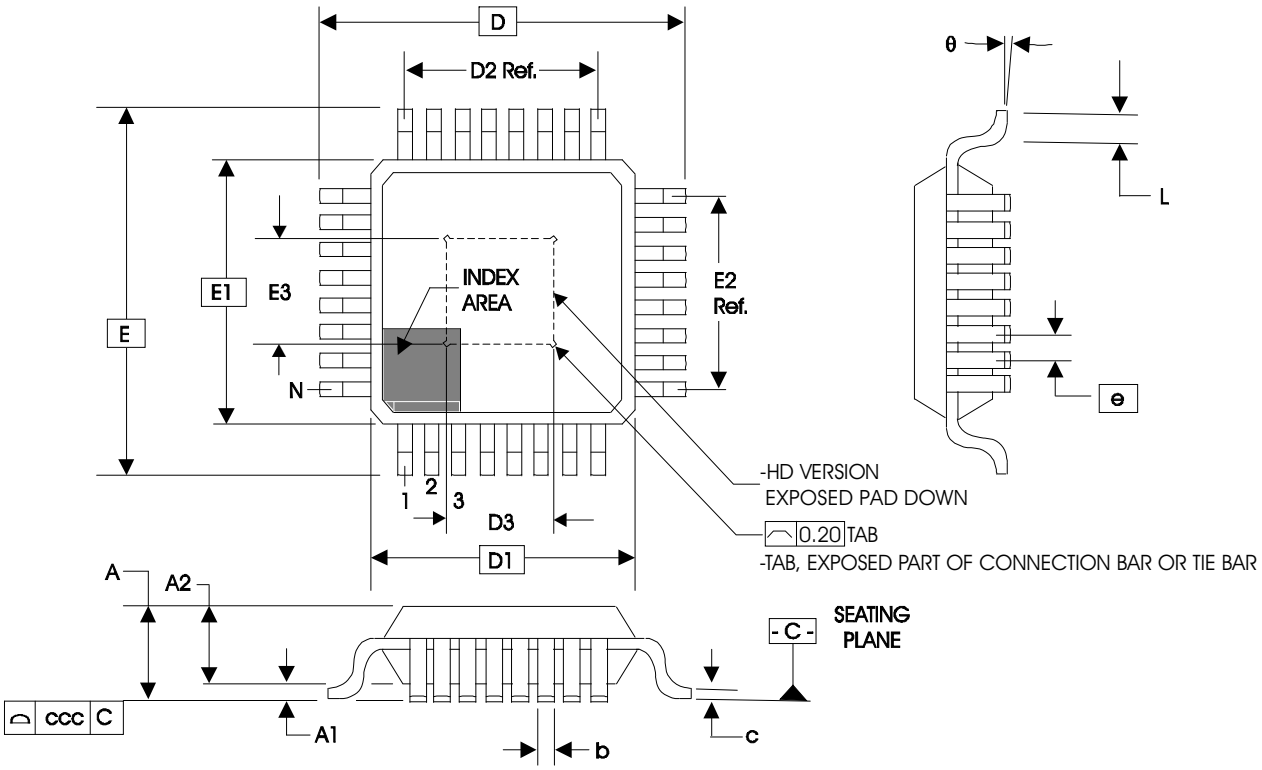


Table 9. Package Dimensions 32 Lead TQFP, E-Pad

JEDEC Variation: ABC - HD All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A			1.20
A1	0.05	0.10	0.15
A2	0.95	1.00	1.05
b	0.30	0.35	0.40
c	0.09		0.20
D & E		9.00 Basic	
D1 & E1		7.00 Basic	
D2 & E2		5.60 Ref.	
D3 & E3	3.0		4.0
e		0.80 Basic	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.10

Reference Document: JEDEC Publication 95, MS-026

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
840S07BYILF	ICS840S07BIL	Lead-Free, 32 Lead TQFP, E-Pad	Tray	-40°C to 85°C
840S07BYILFT	ICS840S07BIL	Lead-Free, 32 Lead TQFP, E-Pad	Tape & Reel	-40°C to 85°C

Revision History

Revision Date	Description of Change
April 14, 2016	▪ Removed ICS from part number where needed. ▪ Ordering Information - removed quantity from tape and reel. Deleted LF note below table. ▪ Updated data sheet header and footer.

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