

NRND – Not Recommend for New Designs - 8/30/2013
For replacement device use ICS840N051BGI

NRND

GENERAL DESCRIPTION

The 840051 is a Gigabit Ethernet Clock Generator and a member of the family of high performance devices from IDT. The 840051 can synthesize 10 Gigabit Ethernet, SONET, or Serial ATA reference clock frequencies with the appropriate choice of crystal and output divider. The 840051 has excellent phase jitter performance and is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

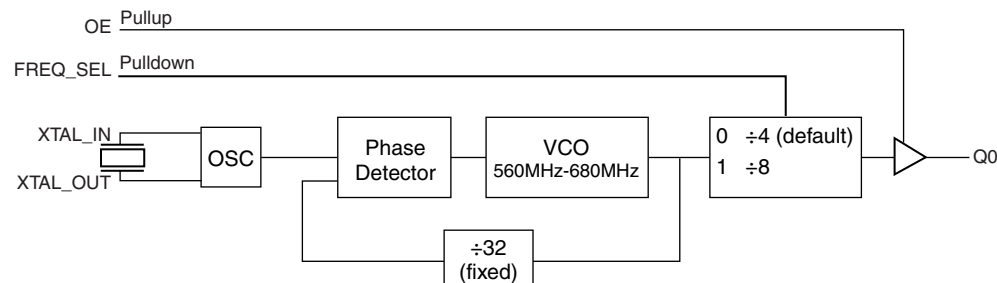
FEATURES

- 1 LVCMOS/LVTTL output, 15Ω output impedance
- Crystal oscillator interface designed for 18pF parallel resonant crystals
- Output frequency range: 70MHz - 170MHz
- VCO range: 560MHz - 680MHz
- RMS phase jitter at 155.52MHz (1.875MHz - 20MHz): 0.48ps (typical)
- RMS phase noise at 155.52MHz
- Offset Noise Power
 - 100Hz-99.7 dBc/Hz
 - 1KHz-120 dBc/Hz
 - 10KHz-128 dBc/Hz
 - 100KHz-127 dBc/Hz
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Lead-Free fully RoHS compliant
- Industrial temperature information available upon request
- **Not Recommended For New Designs**
- **For New Designs use ICS840N051BGI**

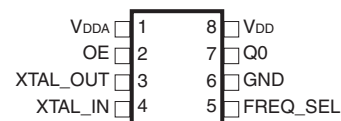
FREQUENCY TABLE

Inputs		Output Frequency (MHz)
Crystal Frequency (MHz)	FREQ_SEL	
20.141601	0	161.132812
20.141601	1	80.566406
19.53125	0	156.25
19.53125	1	78.125
19.44	0	155.52
19.44	1	77.76
18.75	0	150
18.75	1	75

BLOCK DIAGRAM



PIN ASSIGNMENT



840051

8-Lead TSSOP

4.40mm x 3.0mm x 0.925mm
 package body
G Package
 Top View

ICS840051

FEMTOCLOCKS™ CRYSTAL-TO-LVCMOS/LVTTL CLOCK GENERATOR

NRND – Not Recommend for New Designs - 8/30/2013

NRND

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type	Description
1	V _{DDA}	Power	Analog supply pin.
2	OE	Input Pullup	Output enable pin. When HIGH, Q0 output is enabled. When LOW, forces Q0 to HiZ state. LVCMOS/LVTTL interface levels. See Table 3A.
3, 4	XTAL_OUT, XTAL_IN	Input	Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
5	FREQ_SEL	Input Pulldown	Frequency select pin. LVCMOS/LVTTL interface levels. See Table 3B.
6	GND	Power	Power supply ground.
7	Q0	Output	Single-ended clock output. LVCMOS/LVTTL interface levels. 15Ω output impedance.
8	V _{DD}	Power	Core supply pin.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
C _{PD}	Power Dissipation Capacitance	V _{DD} , V _{DDA} = 3.465V		7		pF
R _{PULLUP}	Input Pullup Resistor			51		KΩ
R _{PULLDOWN}	Input Pulldown Resistor			51		KΩ
R _{OUT}	Output Impedance			15		Ω

TABLE 3A. CONTROL FUNCTION TABLE

Control Input	Output
OE	Q0
0	Hi-Z
1	Active

TABLE 3B. FREQ_SEL FUNCTION TABLE

Control Input	N Divider
FRE_SEL	
0	÷4 (default)
1	÷8

ICS840051

FEMTOCLOCKS™ CRYSTAL-TO-LVCMOS/LVTTL CLOCK GENERATOR

NRND – Not Recommend for New Designs - 8/30/2013

NRND

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to $V_{DD} + 0.5V$
Outputs, V_O	-0.5V to $V_{DD} + 0.5V$
Package Thermal Impedance, θ_{JA}	101.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				60	mA
I_{DDA}	Analog Supply Current				10	mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	OE $V_{DD} = V_{IN} = 3.465V$			5	μA
		FREQ_SEL $V_{DD} = V_{IN} = 3.465V$			150	μA
I_{IL}	Input Low Current	OE $V_{DD} = 3.465V, V_{IN} = 0V$	-150			μA
		FREQ_SEL $V_{DD} = 3.465V, V_{IN} = 0V$	-5			μA
V_{OH}	Output High Voltage; NOTE 1		2.6			V
V_{OL}	Output Low Voltage; NOTE 1				0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DD}/2$. See Parameter Measurement Information Section, "3.3V Output Load Test Circuit".

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		17.5		21.25	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

ICS840051

FEMTOCLOCKS™ CRYSTAL-TO-LVCMOS/LVTTL CLOCK GENERATOR

NRND – Not Recommend for New Designs - 8/30/2013

NRND

TABLE 6. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		70		170	MHz
$t_{jit}(\emptyset)$	RMS Phase Jitter (Random); NOTE 1	155.52MHz, Integration Range: 1.875MHz - 20MHz		0.48		ps
		77.76MHz, Integration Range: 1.875MHz - 20MHz		0.45		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		500	ps
odc	Output Duty Cycle		48		52	%

NOTE 1: Please refer to the Phase Noise Plots.

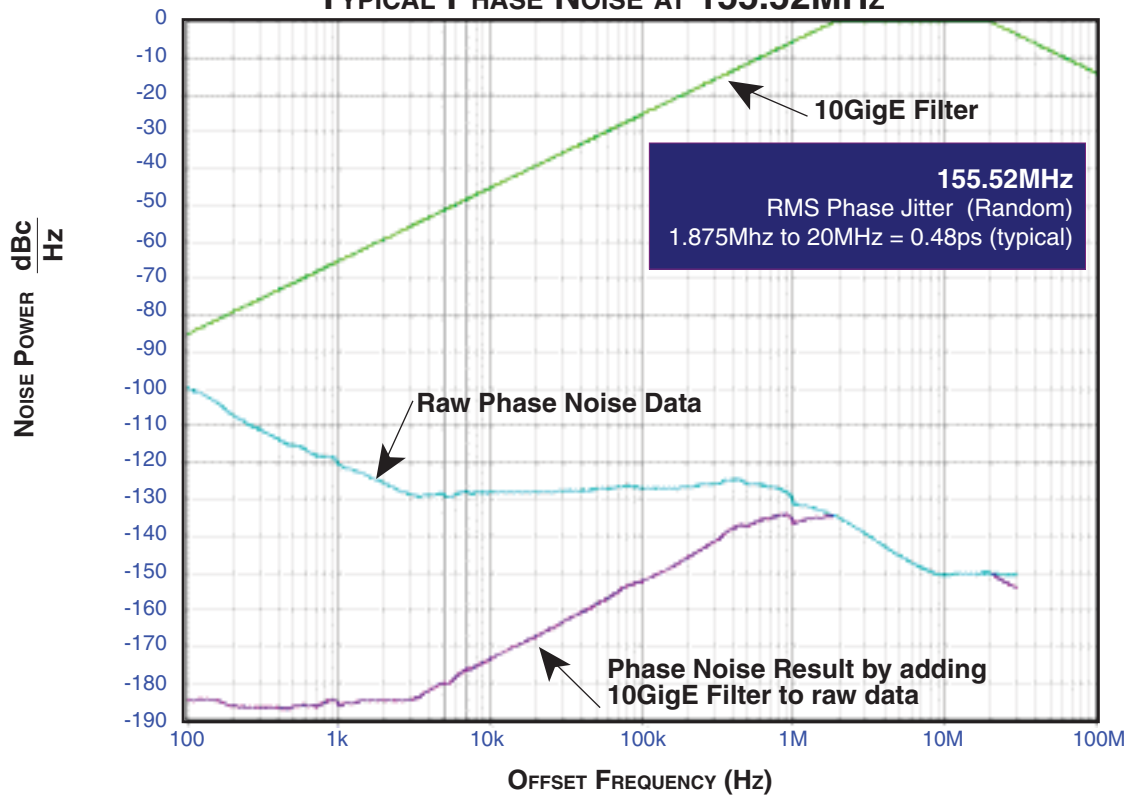
ICS840051

FEMTOCLOCKS™ CRYSTAL-TO-LVCMOS/LVTTL CLOCK GENERATOR

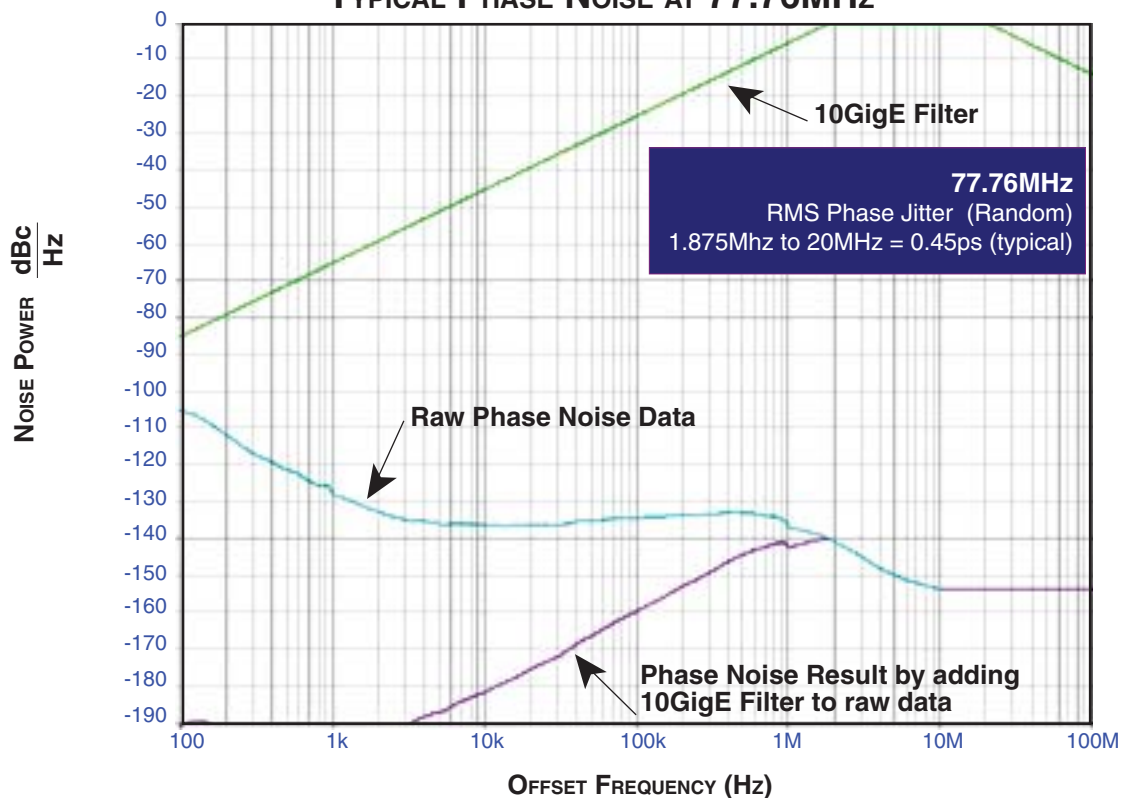
NRND – Not Recommend for New Designs - 8/30/2013

NRND

TYPICAL PHASE NOISE AT 155.52MHz



TYPICAL PHASE NOISE AT 77.76MHz



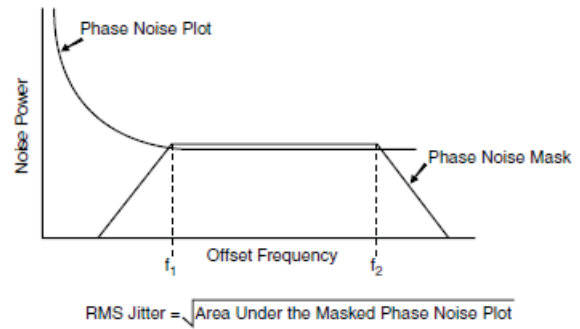
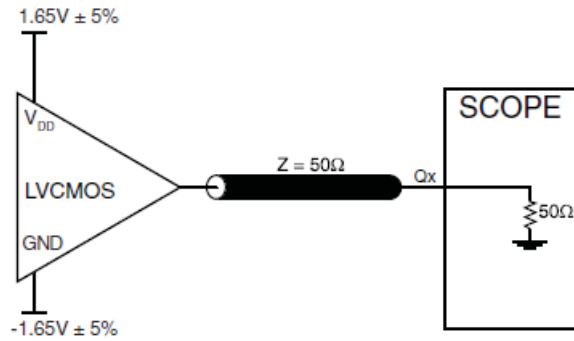
ICS840051

FEMTOCLOCKS™ CRYSTAL-TO-LVCMOS/LVTTL CLOCK GENERATOR

NRND – Not Recommend for New Designs - 8/30/2013

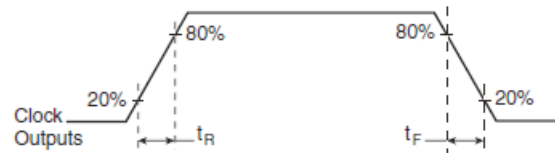
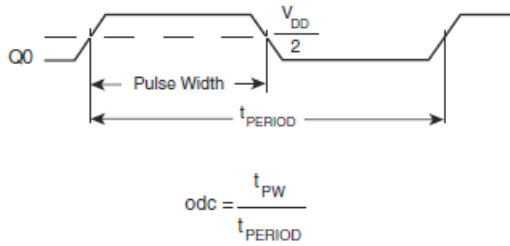
NRND

PARAMETER MEASUREMENT INFORMATION



3.3V OUTPUT LOAD AC TEST CIRCUIT

RMS PHASE JITTER



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 840051 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a $10\mu F$ and a $.01\mu F$ bypass capacitor should be connected to each V_{DDA} pin.

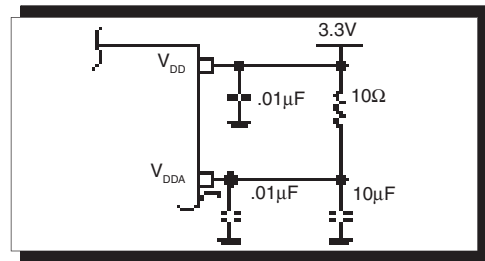


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The 840051 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using an 18pF parallel

resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

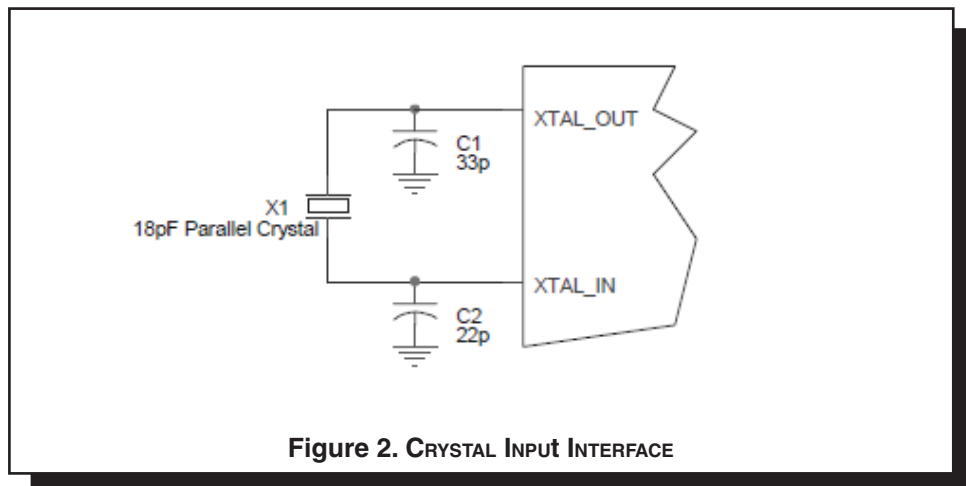


Figure 2. CRYSTAL INPUT INTERFACE

NRND – Not Recommend for New Designs - 8/30/2013

NRND

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

TRANSISTOR COUNT

The transistor count for 840051 is: 1927

ICS840051

FEMTOCLOCKS™ CRYSTAL-TO-LVCMOS/LVTTL CLOCK GENERATOR

NRND – Not Recommend for New Designs - 8/30/2013

NRND

PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP

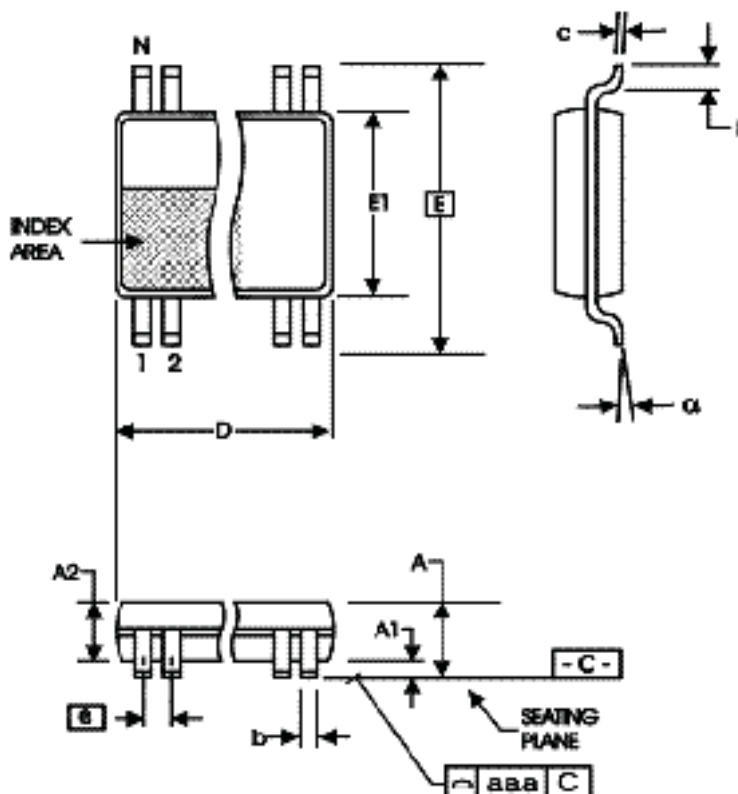


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

ICS840051
FEMTOCLOCKS™ CRYSTAL-TO-
LVCMOS/LVTTL CLOCK GENERATOR

NRND – Not Recommend for New Designs - 8/30/2013

NRND

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
840051AGLF	051AL	8 Lead "Lead-Free" TSSOP	tube	0°C to 70°C
840051AGLFT	051AL	8 Lead "Lead-Free" TSSOP	tape & reel	0°C to 70°C

ICS840051

FEMTOCLOCKS™ CRYSTAL-TO-
LVCMOS/LVTTL CLOCK GENERATOR

NRND – Not Recommend for New Designs - 8/30/2013

NRND

REVISION HISTORY SHEET

Rev	Table	Page	Description of Change	Date
A	T9	10	Ordering Information Table - Removed leaded devices.	9/1/15

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.