

General Description

The 840004I-01 is a 4 output LVCMOS/LVTTL Synthesizer optimized to generate Ethernet reference clock frequencies. Using a 25MHz, 18pF parallel resonant crystal, the following frequencies can be generated based on the 2 frequency select pins (F_SEL1:0): 156.25MHz, 125MHz, and 62.5MHz. The 840004I-01 uses IDT's 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical random rms phase jitter, easily meeting Ethernet jitter requirements. The 840004I-01 is packaged in a small 20-pin TSSOP package.

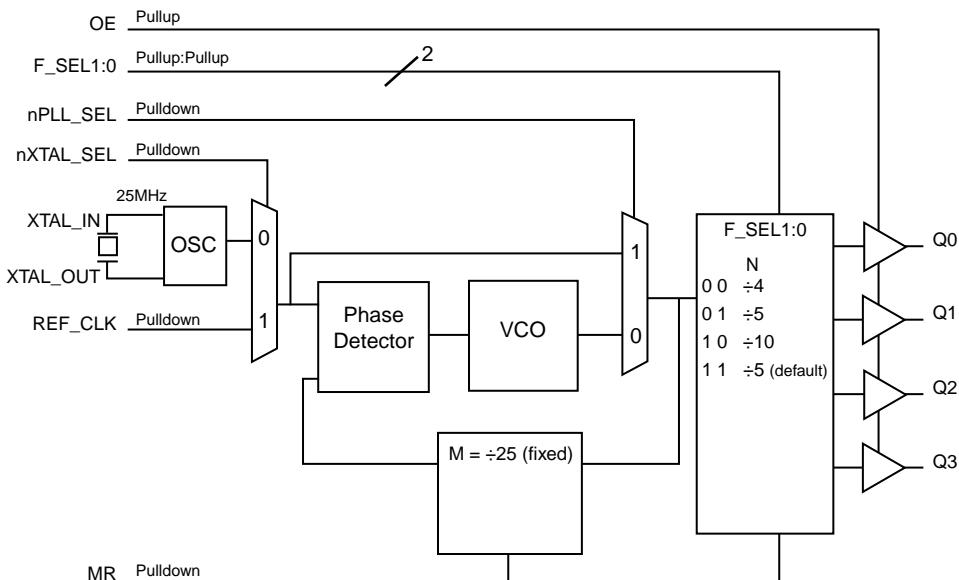
Features

- Four single-ended LVCMOS/LVTTL outputs 17Ω typical output impedance
- Selectable crystal oscillator interface or single-ended input, Supports the following output frequencies: 156.25MHz, 125MHz and 62.5MHz
- VCO range: 560MHz - 700MHz
- RMS phase jitter at 156.25MHz (1.875MHz – 20MHz): 0.52ps (typical)
- Output supply modes:
Core/Output
3.3V/3.3V
3.3V/2.5V
2.5V/2.5V
- 40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package
- For functional replacement part use 8T49N241

Frequency Select Function Table for Ethernet Frequencies

Inputs					Output Frequency (MHz), (25MHz Reference)
F_SEL1	F_SEL0	M Div. Value	N Div. Value	M/N Ratio Value	
0	0	25	4	6.25	156.25
0	1	25	5	5	125
1	0	25	10	2.5	62.5
1	1	25	5	5	125 (default)

Block Diagram



Pin Assignment

F_SEL0	1	F_SEL1	20
nc	2	nc	19
nXTAL_SEL	3	Q0	18
REF_CLK	4	Q1	17
OE	5	VDDO	16
MR	6	Q2	15
nPLL_SEL	7	Q3	14
VDDA	8	GND	13
nc	9	XTAL_IN	12
VDD	10	XTAL_OUT	11

840004I-01
20-Lead TSSOP
6.5mm x 4.4mm x 0.925mm
package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 20	F_SEL0, F_SEL1	Input	Pullup	Frequency select pins. LVCMOS/LVTTL interface levels.
2, 9	nc	Unused		No connect.
3	nXTAL_SEL	Input	Pulldown	Selects between the crystal or REF_CLK inputs as the PLL reference source. When HIGH, selects REF_CLK. When LOW, selects XTAL inputs. LVCMOS/LVTTL interface levels.
4	REF_CLK	Input	Pulldown	Single-ended reference clock input. LVCMOS/LVTTL interface levels.
5	OE	Input	Pullup	Output enable pin. When HIGH, the outputs are active. When LOW, the outputs are in a high impedance state. LVCMOS/LVTTL interface levels.
6	MR	Input	Pulldown	Active HIGH master reset. When logic HIGH, the internal dividers are reset causing the outputs to go low. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
7	nPLL_SEL	Input	Pulldown	PLL bypass. When LOW, the output is driven from the VCO output. When HIGH, the PLL is bypassed and the output frequency = reference clock frequency/N output divider. LVCMOS/LVTTL interface levels.
8	VDDA	Power		Analog supply pin.
10	VDD	Power		Core supply pin.
11, 12	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
13, 19	GND	Power		Power supply ground.
14, 15, 17, 18	Q3, Q2, Q1, Q0	Output		Single-ended clock outputs. 17Ω typical output impedance. LVCMOS/ LVTTL interface levels.
16	VDDO	Power		Output supply pin.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
C _{PD}	Power Dissipation Capacitance			8		pF
R _{PULLUP}	Input Pullup Resistor			51		kΩ
R _{PULLDOWN}	Input Pulldown Resistor			51		kΩ
R _{OUT}	Output Impedance	V _{DDO} = 3.3V±5%		17		Ω
		V _{DDO} = 2.5V±5%		21		Ω

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to $V_{DD} + 0.5V$
Outputs, V_O	-0.5V to $V_{DD} + 0.5V$
Package Thermal Impedance, θ_{JA}	73.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{DD}	Power Supply Current				100	mA
I_{DDA}	Analog Supply Current				12	mA
I_{DDO}	Output Supply Current				10	mA

Table 3B. Power Supply DC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				95	mA
I_{DDA}	Analog Supply Current				12	mA
I_{DDO}	Output Supply Current				8	mA

Table 3C. LVC MOS/LVTTL DC Characteristics, $T_A = -40^\circ\text{C}$ to 85°C

Symbol	Parameter	Test Conditions		Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	$V_{DD} = 3.465\text{V}$		2		$V_{DD} + 0.3$	V
		$V_{DD} = 2.625\text{V}$		1.7		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	$V_{DD} = 3.465\text{V}$		-0.3		0.8	V
		$V_{DD} = 2.625\text{V}$		-0.3		0.7	V
I_{IH}	Input High Current	nXTAL_SEL, nPLL_SEL, REF_CLK, MR	$V_{DD} = V_{IN} = 3.465\text{V}$ or 2.625V			150	μA
		OE, F_SEL[0:1]	$V_{DD} = V_{IN} = 3.465\text{V}$ or 2.625V			5	μA
I_{IL}	Input Low Current	nXTAL_SEL, nPLL_SEL, REF_CLK, MR	$V_{DD} = 3.465\text{V}$ or 2.625V , $V_{IN} = 0\text{V}$		-5		μA
		OE, F_SEL[0:1]	$V_{DD} = 3.465\text{V}$ or 2.625V , $V_{IN} = 0\text{V}$		-150		μA
V_{OH}	Output High Voltage; NOTE 1	$V_{DDO} = 3.3\text{V} \pm 5\%$		2.6			V
		$V_{DDO} = 2.5\text{V} \pm 5\%$		1.8			V
V_{OL}	Output Low Voltage; NOTE 1	$V_{DDO} = 3.3\text{V} \pm 5\%$ or $2.5\text{V} \pm 5\%$				0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement Information section. *Load Test Circuit diagrams*.

Table 4. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

AC Electrical Characteristics

Table 5A. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{out}	Output Frequency	$F_{SEL}[1:0] = 00$	140	156.25	175	MHz
		$F_{SEL}[1:0] = 01$ or 11	112	125	140	MHz
		$F_{SEL}[1:0] = 10$	56	62.5	70	MHz
$t_{sk}(o)$	Output Skew: NOTE 1, 2				60	MHz
$t_{jit}(\emptyset)$	RMS Phase Jitter (Random); NOTE 3	156.25MHz, Integration Range: 1.875MHz – 20MHz		0.52		ps
		125MHz, Integration Range: 1.875MHz – 20MHz		0.65		ps
		62.5MHz, Integration Range: 1.875MHz – 20MHz		0.55		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		750	ps
odc	Output Duty Cycle	$F_{SEL}[1:0] = 00, 01$ or 11	42		58	%
		$F_{SEL}[1:0] = 10$	49		51	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Please refer to the Phase Noise Plot.

Table 5B. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{out}	Output Frequency	$F_{SEL}[1:0] = 00$	140	156.25	175	MHz
		$F_{SEL}[1:0] = 01$ or 11	112	125	140	MHz
		$F_{SEL}[1:0] = 10$	56	62.5	70	MHz
$t_{sk}(o)$	Output Skew: NOTE 1, 2				60	MHz
$t_{jit}(\emptyset)$	RMS Phase Jitter (Random); NOTE 3	156.25MHz, Integration Range: 1.875MHz – 20MHz		0.48		ps
		125MHz, Integration Range: 1.875MHz – 20MHz		0.59		ps
		62.5MHz, Integration Range: 1.875MHz – 20MHz		0.53		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		750	ps
odc	Output Duty Cycle	$F_{SEL}[1:0] = 00, 01$ or 11	42		58	%
		$F_{SEL}[1:0] = 10$	49		51	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Please refer to the Phase Noise Plot.

Table 5C. AC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{out}	Output Frequency	$F_{SEL}[1:0] = 00$	140	156.25	175	MHz
		$F_{SEL}[1:0] = 01$ or 11	112	125	140	MHz
		$F_{SEL}[1:0] = 10$	56	62.5	70	MHz
$t_{sk(o)}$	Output Skew: NOTE 1, 2				60	MHz
$t_{jit}(\emptyset)$	RMS Phase Jitter (Random); NOTE 3	156.25MHz, Integration Range: 1.875MHz – 20MHz		0.50		ps
		125MHz, Integration Range: 1.875MHz – 20MHz		0.60		ps
		62.5MHz, Integration Range: 1.875MHz – 20MHz		0.51		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		750	ps
odc	Output Duty Cycle	$F_{SEL}[1:0] = 00, 01$ or 11	42		58	%
		$F_{SEL}[1:0] = 10$	49		51	%

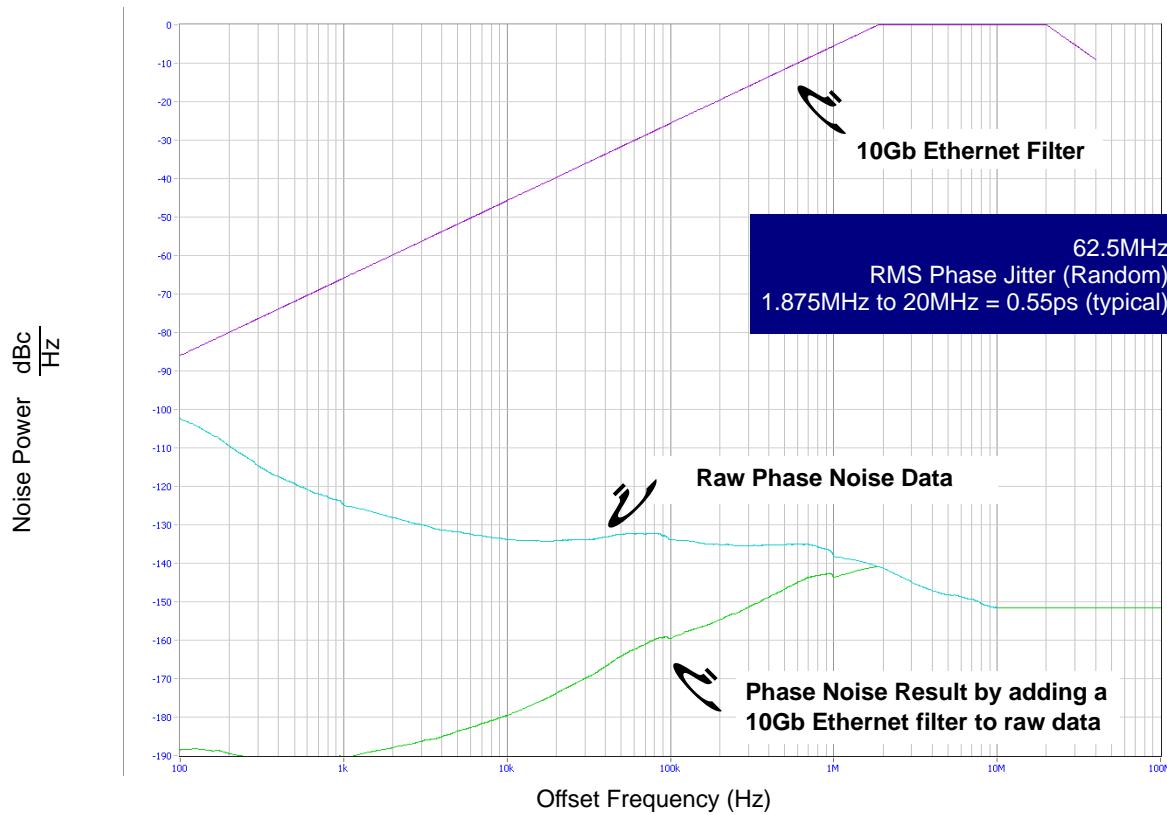
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.

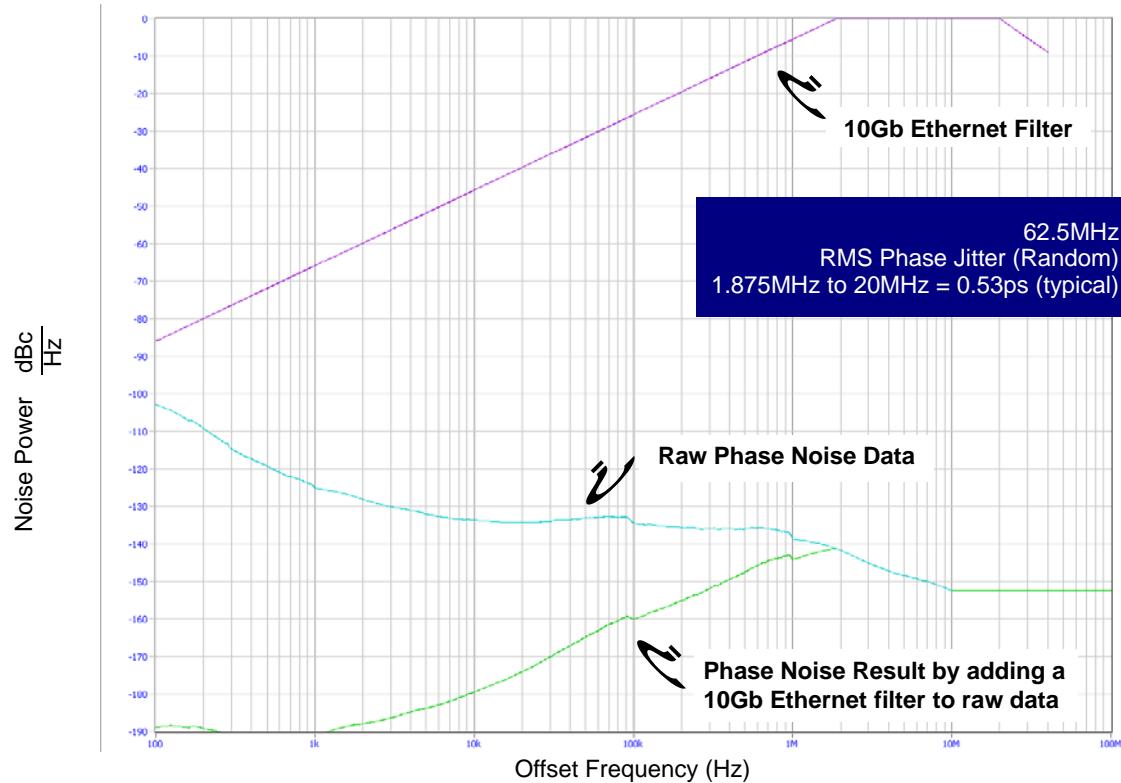
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Please refer to the Phase Noise Plot.

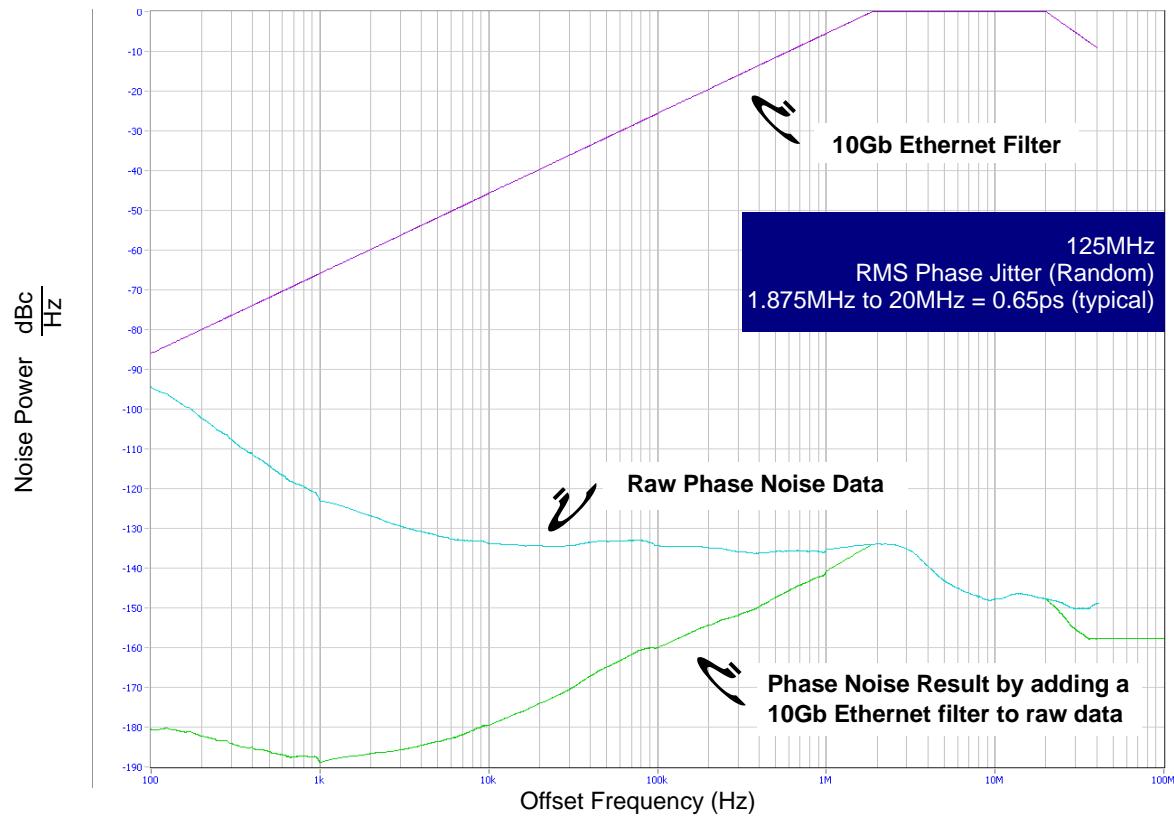
Typical Phase Noise at 62.5MHz (3.3V)



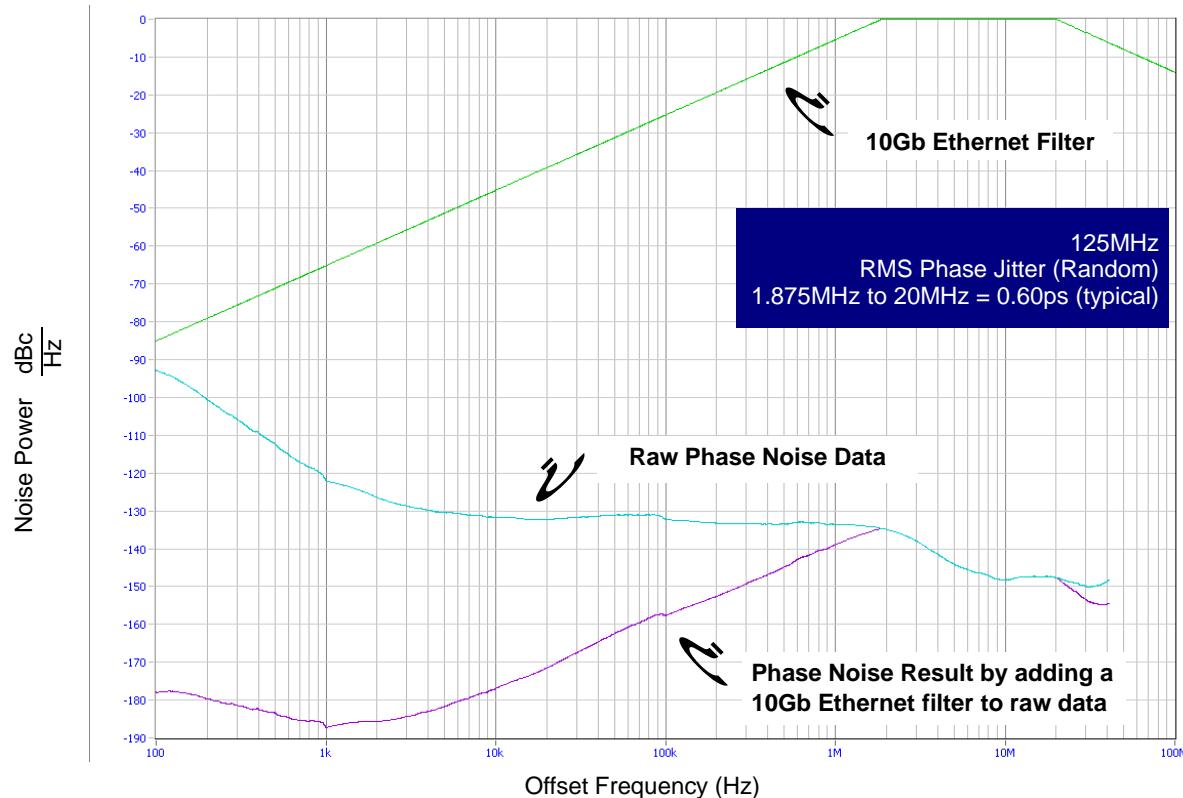
Typical Phase Noise at 62.5MHz (2.5V)



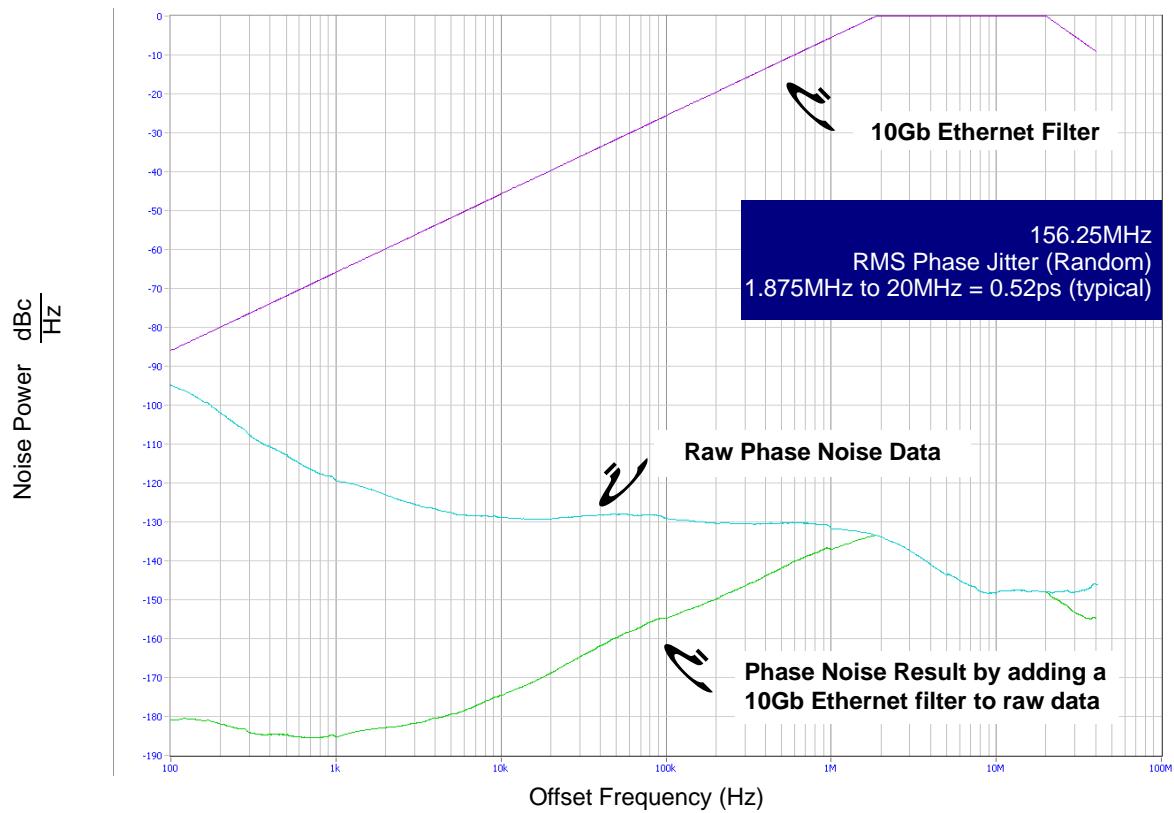
Typical Phase Noise at 125MHz (3.3V)



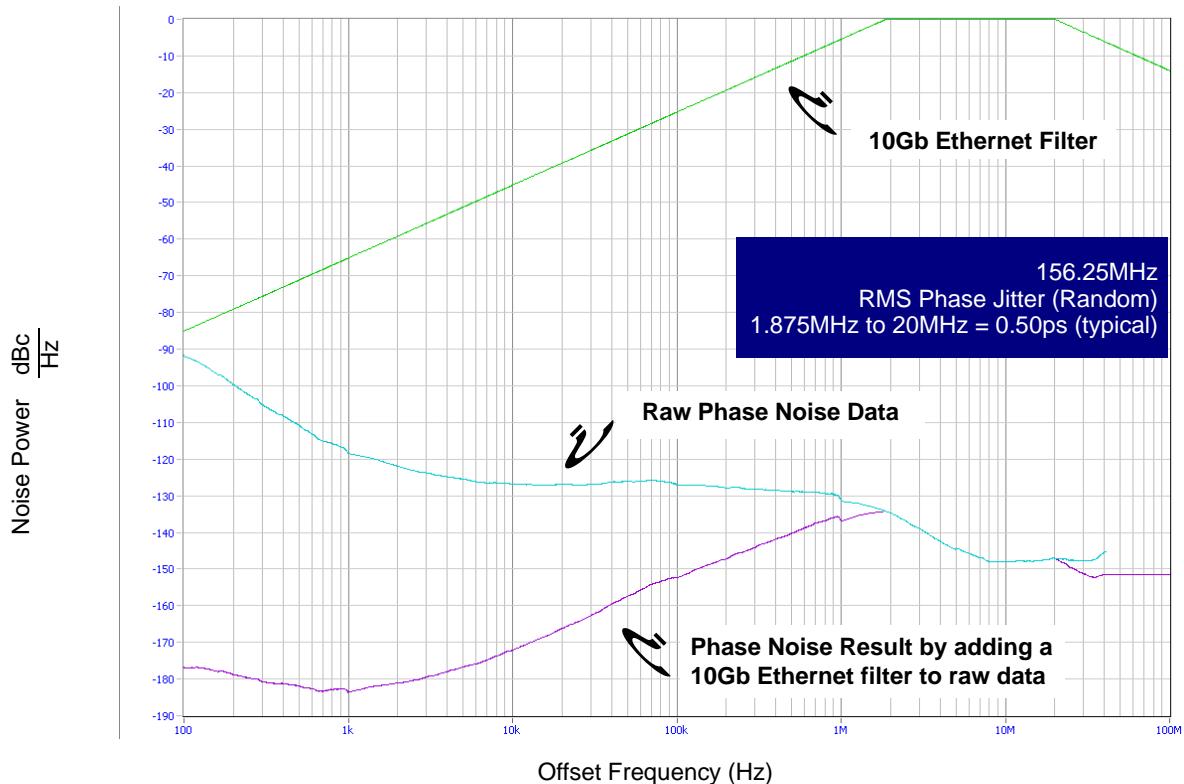
Typical Phase Noise at 125MHz (2.5V)



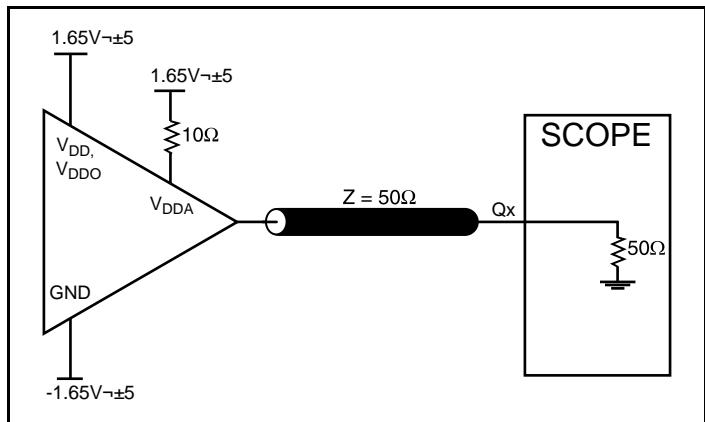
Typical Phase Noise at 156.25MHz (3.3V)



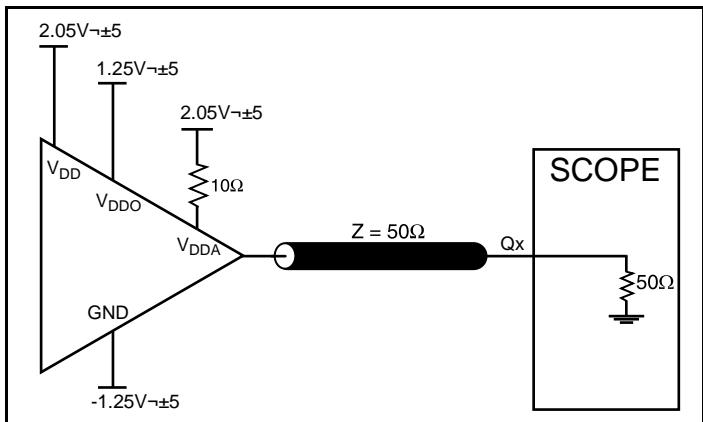
Typical Phase Noise at 156.25MHz (2.5V)



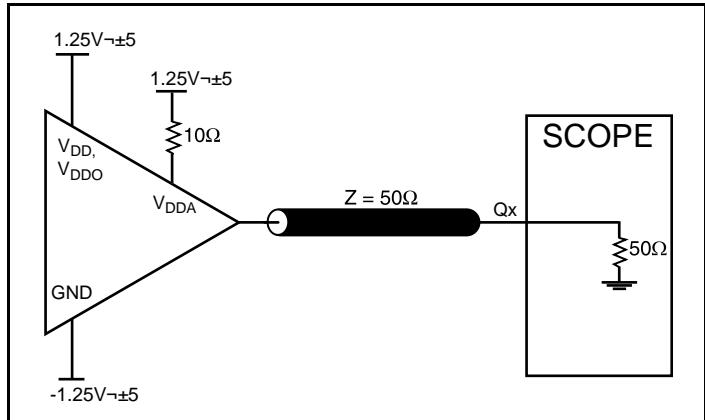
Parameter Measurement Information



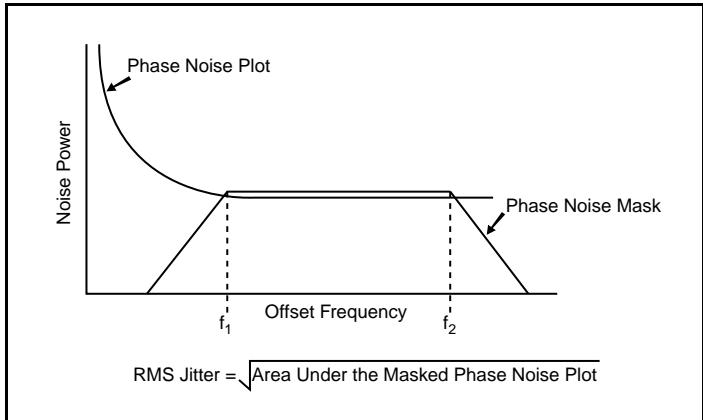
3.3V Core/3.3V LVC MOS Output Load AC Test Circuit



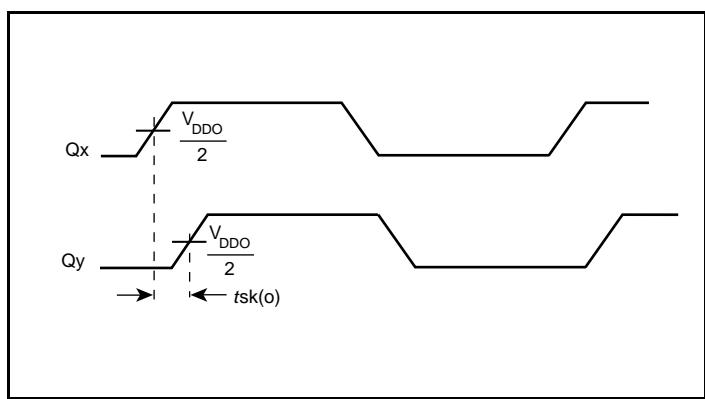
3.3V Core/2.5V LVC MOS Output Load AC Test Circuit



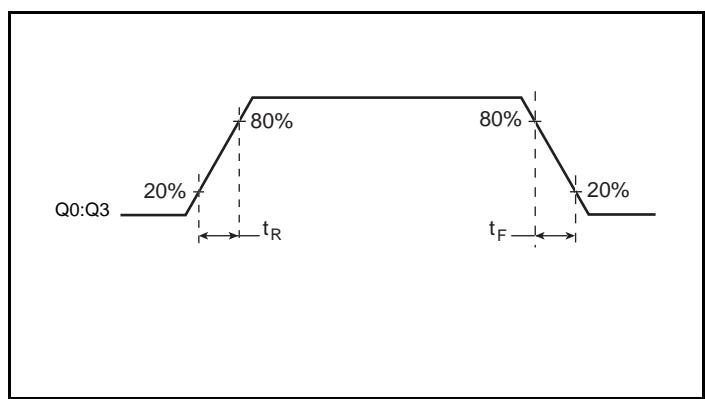
2.5V Core/2.5V LVC MOS Output Load AC Test Circuit



RMS Phase Jitter

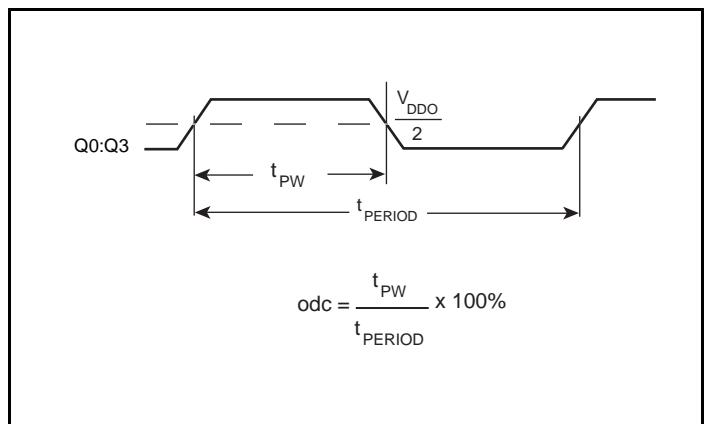


Output Skew



Output Rise/Fall Time

Parameter Measurement Information, continued



Output Duty Cycle Pulse Width/Period

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a $1\text{k}\Omega$ resistor can be tied from XTAL_IN to ground.

REF_CLK Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a $1\text{k}\Omega$ resistor can be tied from the REF_CLK to ground.

LVC MOS Control Pins

All control pins have internal pull-downs; additional resistance is not required but can be added for additional protection. A $1\text{k}\Omega$ resistor can be used.

Outputs:

LVC MOS Outputs

All unused LVC MOS outputs can be left floating. We recommend that there is no trace attached.

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 8400041-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} , V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and $0.01\mu\text{F}$ bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a $10\mu\text{F}$ bypass capacitor be connected to the V_{DDA} pin.

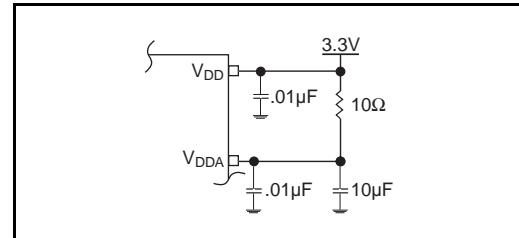


Figure 1. Power Supply Filtering

Crystal Input Interface

The 840004I-01 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

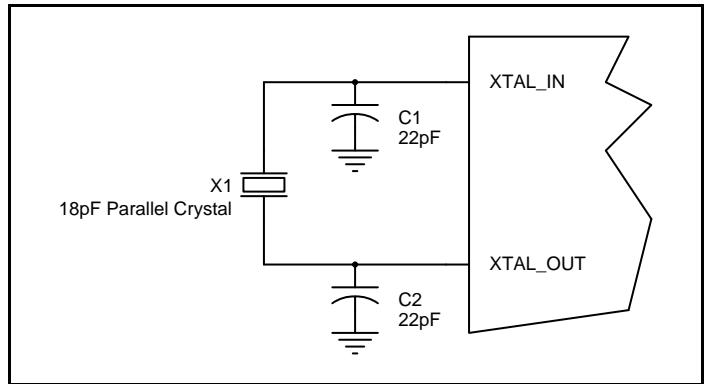


Figure 2. Crystal Input Interface

LVCMS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3*. The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output

impedance of the driver (R_o) plus the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R_1 and R_2 in parallel should equal the transmission line impedance. For most 50Ω applications, R_1 and R_2 can be 100Ω . This can also be accomplished by removing R_1 and making $R_2 50\Omega$.

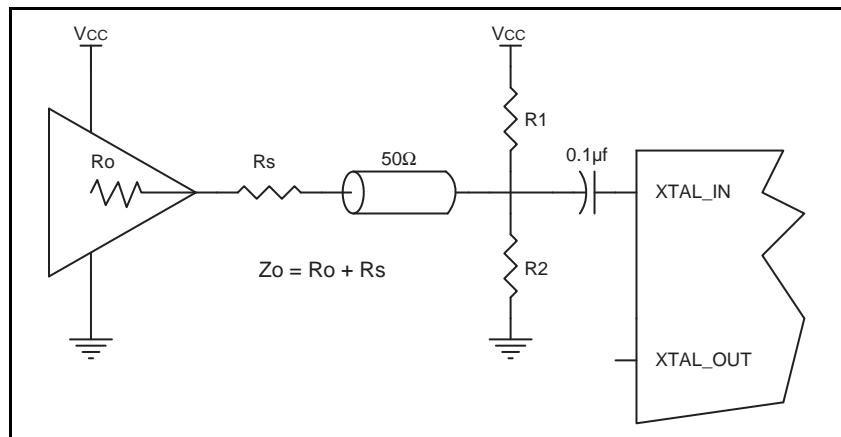


Figure 3. General Diagram for LVCMS Driver to XTAL Input Interface

Schematic Example

Figure 4 shows a schematic example of the 840004I-01. An example of LVCMS termination is shown in this schematic. Additional LVCMS termination approaches are shown in the LVCMS Termination Application Note. In this example, an 18pF parallel resonant 25MHz crystal is used. The $C_1 = 22\text{pF}$ and $C_2 = 22\text{pF}$

are recommended for frequency accuracy. For different board layouts, the C_1 and C_2 may be slightly adjusted for optimizing frequency accuracy. $1\text{k}\Omega$ pullup or pulldown resistors can be used for the logic control input pins.

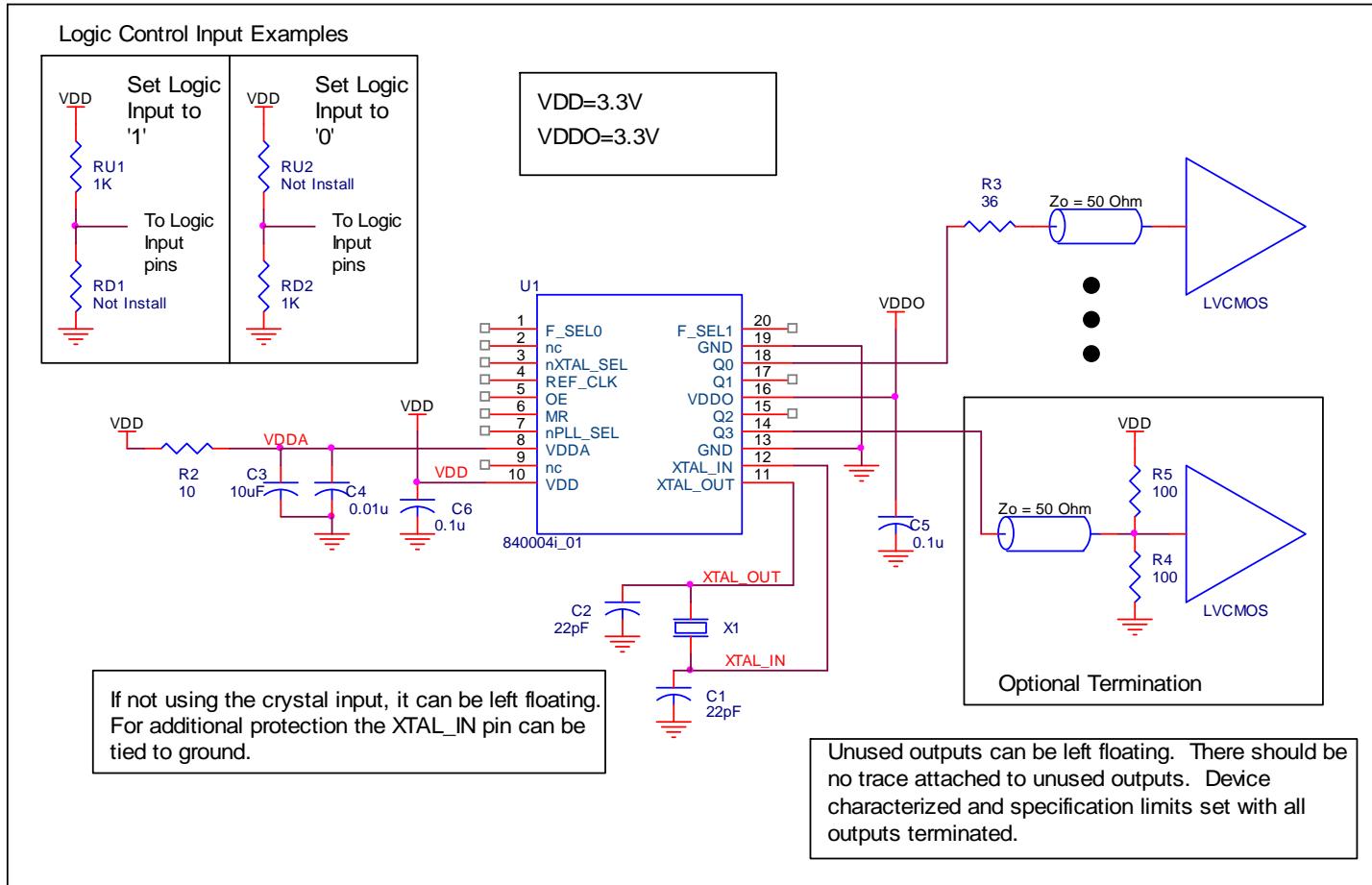


Figure 4. P.C. 840004I-01 Schematic Example

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 20 Lead TSSOP

θ_{JA} by Velocity			
Linear Feet per Minute	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

Transistor Count

The transistor count for 840004I-01: 3796

Package Outline and Package Dimensions

Package Outline - G Suffix for 20 Lead TSSOP

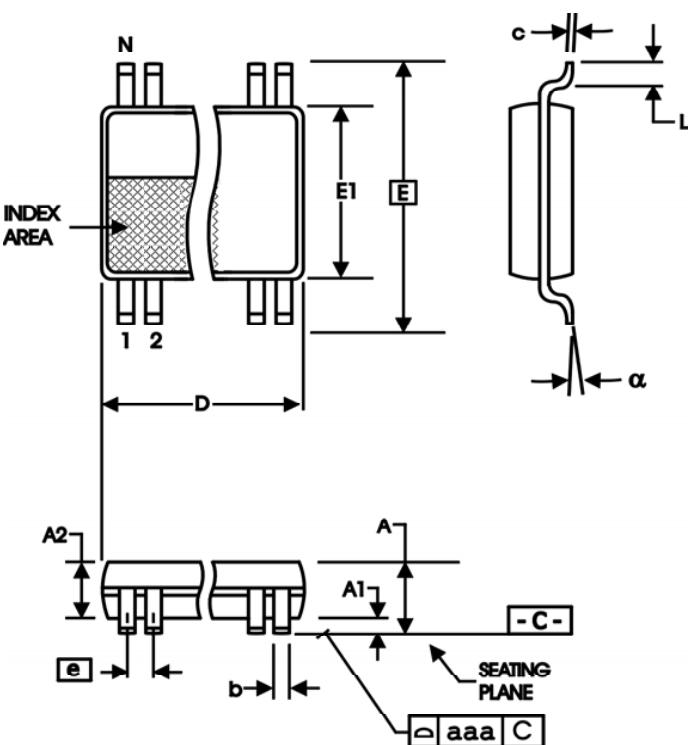


Table 7. Package Dimensions for 20 Lead TSSOP

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	20	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40	Basic
E1	4.30	4.50
e	0.65	Basic
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
840004BGI-01LF	ICS0004BI01L	20 Lead "Lead-Free" TSSOP	Tube	-40°C to 85°C
840004BGI-01LFT	ICS0004BI01L	20 Lead "Lead-Free" TSSOP	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T8	15	Ordering Information Table - corrected standard marking and added lead-free marking.	10/22/07
B	T5A - T5B	4 - 5	AC Characteristics Tables - revised Test Conditions for Output Duty Cycle. Updated format throughout datasheet.	10/30/08
C	T5A - T5B T5C	5 6	Changed from ICS840004AGI-01 to ICS840004BGI-01 throughout. AC Characteristics - Changed Output Rise/Fall Time and Output Duty Cycle. AC Characteristics - Changed Output Rise/Fall Time and Output Duty Cycle.	2/9/09
C	T8	16	Ordering Information - removed leaded devices. Updated data sheet format.	4/2/15
C		1	Product Discontinuation Notice - Last time buy expires November 2, 2016. PDN# CQ-15-05.	11/4/15
D			Obsolete datasheet per PDN# CQ-15-05. Updated datasheet header/footer.	11/7/16

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.