

## GENERAL DESCRIPTION

The 840001I-25 is a General Purpose Clock Generator and a member of the family of high performance devices from IDT. The 840001I-25 can accept frequency from a 22.4MHz to 170MHz and generate a 22.4MHz to 170MHz output. The 840001I-25 has excellent phase jitter performance, from 637kHz – 10MHz integration range. The 840001I-25 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

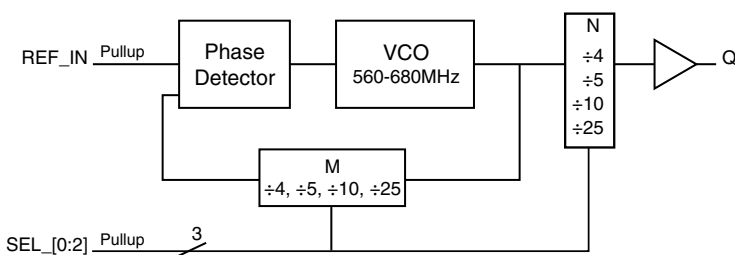
## FEATURES

- One LVCMOS/LVTTL output, 15Ω output impedance
- Output frequency range: 22.4MHz – 170MHz
- VCO range: 560MHz to 680MHz
- RMS phase jitter @ 125MHz (637kHz - 10MHz): 0.36ps (typical)
- Full 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

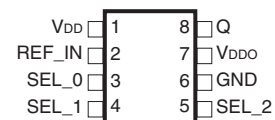
## COMMONLY USED FREQUENCY TABLE

Inputs						Output Frequency (MHz)
SEL2	SEL1	SEL0	M Divider	N Divider	REF_IN (MHz)	Q
0	0	0	25	25	25	25
0	0	1	10	25	62.5	25
0	1	0	4	25	156.25	25
0	1	1	5	25	125	25
1	0	0	10	10	62.5	62.5
1	0	1	5	5	125	125
1	1	0	4	4	156.25	156.25
1	1	1	10	25	62.5	25 (default)

## BLOCK DIAGRAM



## PIN ASSIGNMENT



### 840001I-25

#### 8-Lead TSSOP

4.40mm x 3.0mm x 0.925mm package body

#### G Package

Top View

**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1	$V_{DD}$	Power		Positive supply pin.
2	REF_IN	Input	Pullup	Reference input frequency. LVCMOS/LVTTL interface levels.
3, 4, 5	SEL_0, SEL_1, SEL_2	Input	Pullup	M and N configuration select pins. LVCMOS/LVTTL interface levels.
6	GND	Power		Power supply ground.
7	$V_{DDO}$	Power		Output supply pin.
8	Q	Output		Single-ended clock output. LVCMOS/LVTTL interface levels. 15 $\Omega$ output impedance.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$C_{IN}$	Input Capacitance			4		pF
$C_{PD}$	Power Dissipation Capacitance	$V_{DD}, V_{DDO} = 3.465V$		6		pF
		$V_{DD}, V_{DDO} = 2.625V$		5		pF
$R_{PULLUP}$	Input Pullup Resistor			51		k $\Omega$
$R_{OUT}$	Output Impedance			15		$\Omega$

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	129.5°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 3A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Positive Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$	Power Supply Current				83	mA
$I_{DDO}$	Output Supply Current	No Load			2	mA

**TABLE 3B. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Positive Supply Voltage		2.375	2.5	2.625	V
$V_{DDO}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current				80	mA
$I_{DDO}$	Output Supply Current	No Load			2	mA

**TABLE 3C. LVCMOS/LVTTL DC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$  OR  $2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	$V_{DD} = 3.465V$	2		$V_{DD} + 0.3$	V
		$V_{DD} = 2.625V$	1.7		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	$V_{DD} = 3.465V$	-0.3		0.8	V
		$V_{DD} = 2.625V$	-0.3		0.7	V
$I_{IH}$	Input High Current	REF_IN, SEL_[0:2] $V_{DD} = V_{IN} = 3.465V$ or $2.625V$			5	$\mu\text{A}$
$I_{IL}$	Input Low Current	REF_IN, SEL_[0:2] $V_{DD} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-150			$\mu\text{A}$
$V_{OH}$	Output High Voltage; NOTE 1	$V_{DDO} = 3.465V$	2.6			V
		$V_{DDO} = 2.625V$	1.8			V
$V_{OL}$	Output Low Voltage; NOTE 1	$V_{DDO} = 3.465V$ or $2.625V$			0.6	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DDO}/2$ . See Parameter Measurement Information Section, "Output Load Test Circuit" diagrams.

**TABLE 4A. AC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency		22.4		170	MHz
$t_{jit}(\emptyset)$	RMS Phase Jitter (Random); NOTE 1	125MHz, Integration Range: 637kHz - 10MHz		0.37		ps
		156.25MHz, Integration Range: 637kHz - 10MHz		0.38		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	150		650	ps
odc	Output Duty Cycle		47		53	%

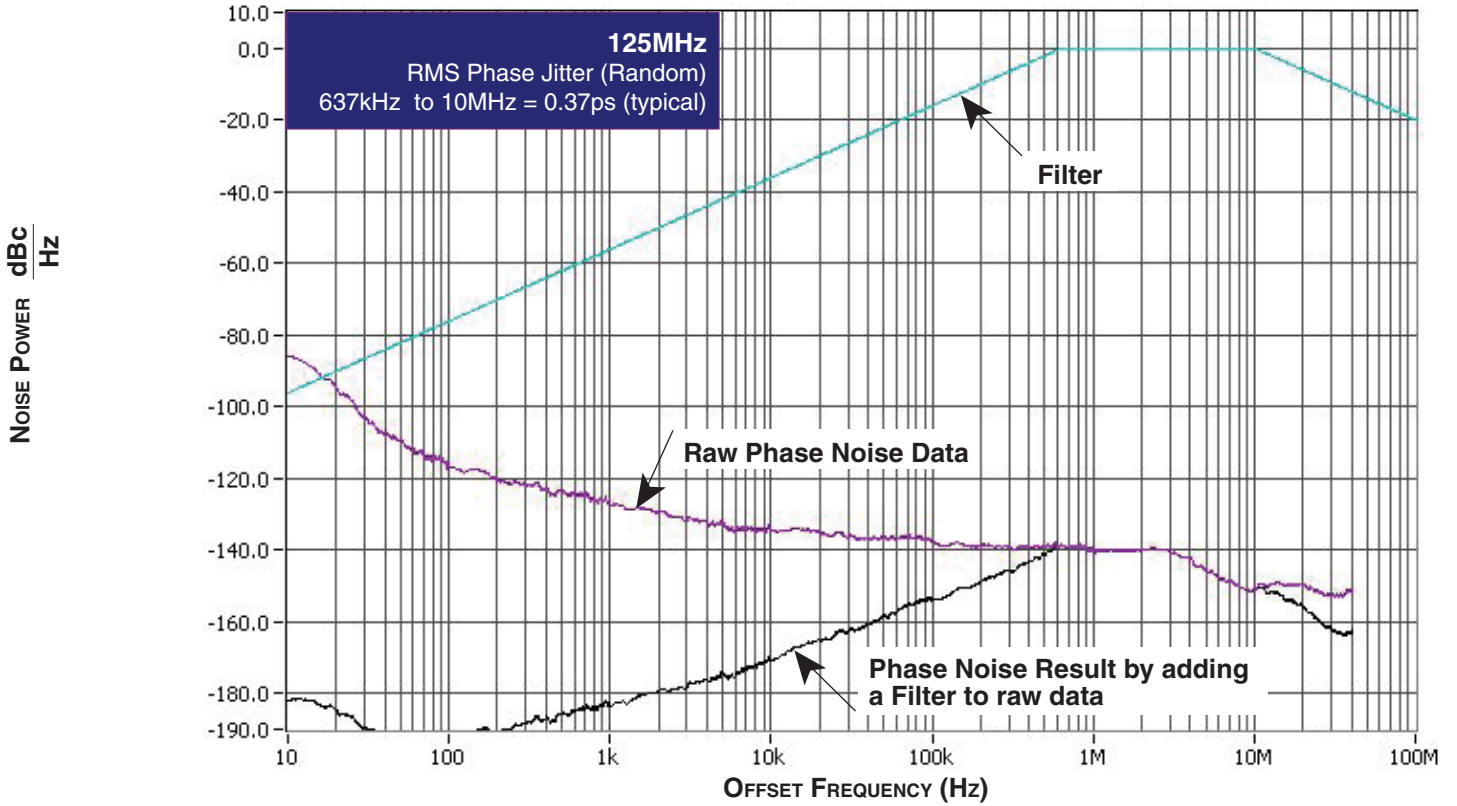
NOTE 1: Please refer to the Phase Noise Plot.

**TABLE 4B. AC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$**

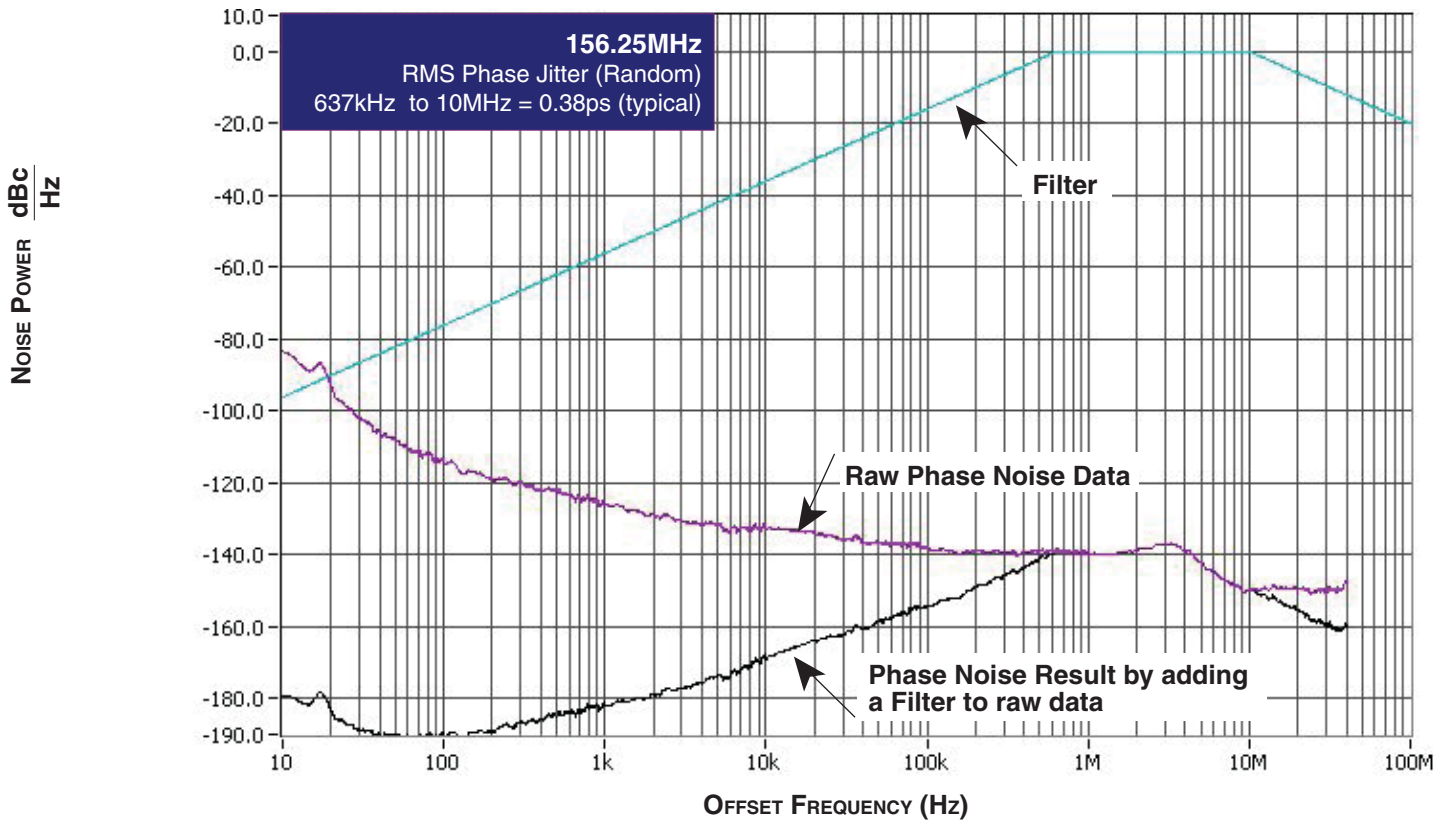
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency		22.4		170	MHz
$t_{jit}(\emptyset)$	RMS Phase Jitter (Random); NOTE 1	125MHz, Integration Range: 637kHz - 10MHz		0.36		ps
		156.25MHz, Integration Range: 637kHz - 10MHz		0.35		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	150		650	ps
odc	Output Duty Cycle		47		53	%

NOTE 1: Please refer to the Phase Noise Plot.

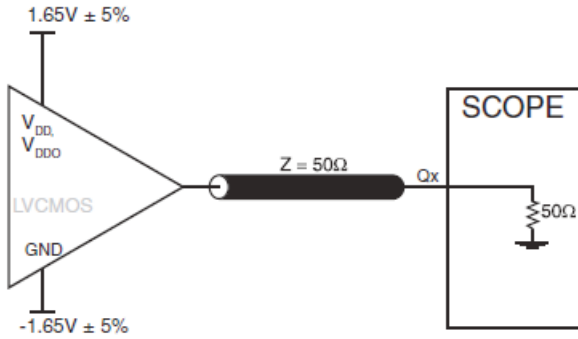
TYPICAL PHASE NOISE AT 125MHz @ 3.3V



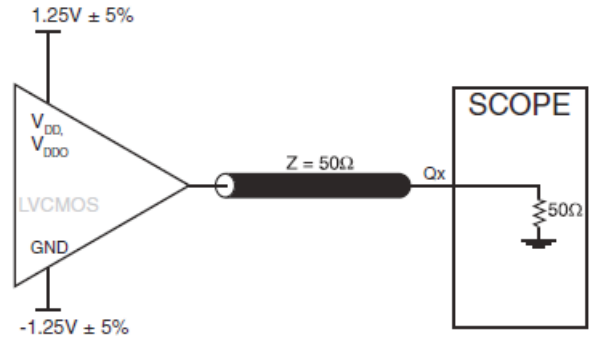
TYPICAL PHASE NOISE AT 156.25MHz @ 3.3V



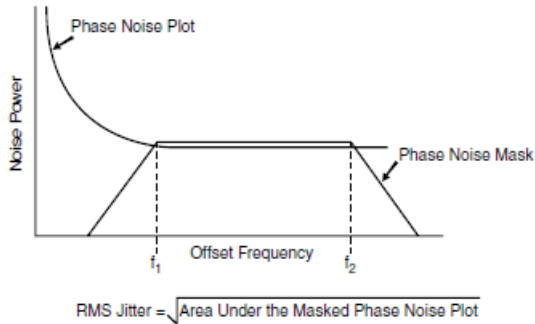
## PARAMETER MEASUREMENT INFORMATION



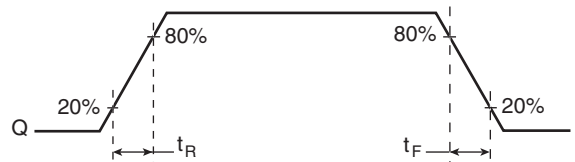
3.3V OUTPUT LOAD AC TEST CIRCUIT



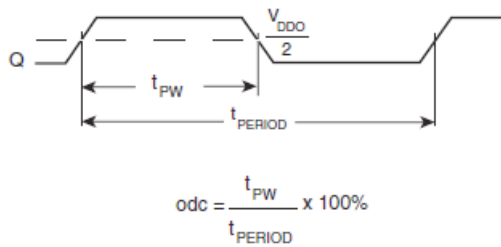
2.5V OUTPUT LOAD AC TEST CIRCUIT



RMS PHASE JITTER



OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

## APPLICATION INFORMATION

### RECOMMENDATIONS FOR UNUSED INPUT PINS

#### INPUTS:

#### LVC MOS CONTROL PINS:

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 840001I-25. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 840001I-25 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

#### Core and Output Power Dissipation

- Power (core, output) =  $V_{DD\_MAX} * (I_{DD} + I_{DDO}) = 3.465V * (83mA + 2mA) = \mathbf{294.5mW}$

#### LVC MOS Output Power Dissipation

- Output Impedance  $R_{OUT}$  Power Dissipation due to Loading  $50\Omega$  to  $V_{DDO}/2$   
Output Current  $I_{OUT} = V_{DDO\_MAX} / [2 * (50\Omega + R_{OUT})] = 3.465V / [2 * (50\Omega + 15\Omega)] = \mathbf{26.6mA}$
- Power Dissipation on the  $R_{OUT}$  per LVC MOS output  
Power ( $R_{OUT}$ ) =  $R_{OUT} * (I_{OUT})^2 = 15\Omega * (26.6mA)^2 = \mathbf{10.6mW}$  per output
- Dynamic Power Dissipation at 156.25MHz  
Power (156.25MHz) =  $C_{PD} * Frequency * (V_{DDO})^2 = 6pF * 156.25MHz * (3.465V)^2 = \mathbf{11.26mW}$  per output

#### Total Power Dissipation

- Total Power**  
= Power (core, output) + Power Dissipation ( $R_{OUT}$ ) + Dynamic Power Dissipation (156.25MHz)  
=  $294.5mW + 10.6mW + 11.26mW$   
=  $\mathbf{316.4mW}$



2. Junction Temperature.

Junction temperature, T<sub>j</sub>, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for T<sub>j</sub> is as follows:  $T_j = \theta_{JA} * Pd_{total} + T_A$

T<sub>j</sub> = Junction Temperature

θ<sub>JA</sub> = Junction-to-Ambient Thermal Resistance

Pd<sub>total</sub> = Total Device Power Dissipation (example calculation is in section 1 above)

T<sub>A</sub> = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ<sub>JA</sub> must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 125.5°C/W per Table 5.

Therefore, T<sub>j</sub> for an ambient temperature of 85°C with all outputs switching is:

$$85^{\circ}\text{C} + 0.316\text{W} * 125.5^{\circ}\text{C}/\text{W} = 124.7^{\circ}\text{C}.$$

This is below the limit of 125°C.

This calculation is only an example. T<sub>j</sub> will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

**TABLE 5. THERMAL RESISTANCE θ<sub>JA</sub> FOR 8-LEAD TSSOP, FORCED CONVECTION**

<b>θ<sub>JA</sub> by Velocity (Meters Per Second)</b>			
	<b>0</b>	<b>1</b>	<b>2.5</b>
Multi-Layer PCB, JEDEC Standard Test Boards	129.5°C/W	125.5°C/W	123.5°C/W

## RELIABILITY INFORMATION

TABLE 6.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 8 LEAD TSSOP

$\theta_{JA}$ by Velocity (Meters Per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	129.5°C/W	125.5°C/W	123.5°C/W

### TRANSISTOR COUNT

The transistor count for 8400011-25 is: 2588

## PACKAGE OUTLINE AND PACKAGE DIMENSIONS

PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP

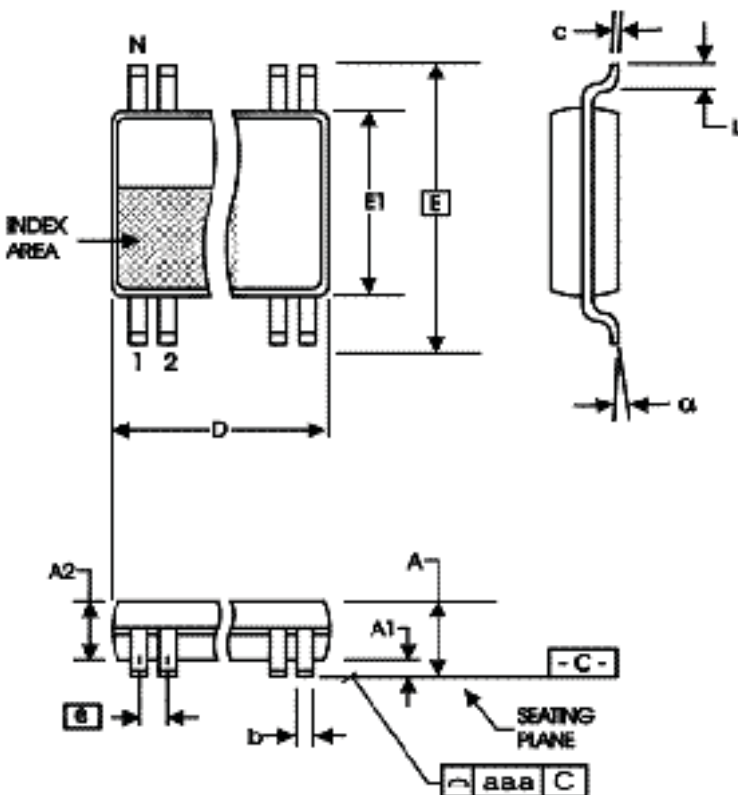


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
$\alpha$	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

**TABLE 8. ORDERING INFORMATION**

<b>Part/Order Number</b>	<b>Marking</b>	<b>Package</b>	<b>Shipping Packaging</b>	<b>Temperature</b>
840001BGI-25LF	BI25L	8 lead "Lead Free" TSSOP	tube	-40°C to 85°C
840001BGI-25LFT	BI25L	8 lead "Lead Free" TSSOP	tape & reel	-40°C to 85°C

**REVISION HISTORY SHEET**

<b>Rev</b>	<b>Table</b>	<b>Page</b>	<b>Description of Change</b>	<b>Date</b>
A	T8	11	Ordering Information - removed leaded devices. Updated data sheet format.	7/29/15
A	T8	1 11	General Description - removed Hipercllocks. Ordering Information - removed Lead Free note below the table. Updated header and footer.	1/15/16



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