

GENERAL DESCRIPTION

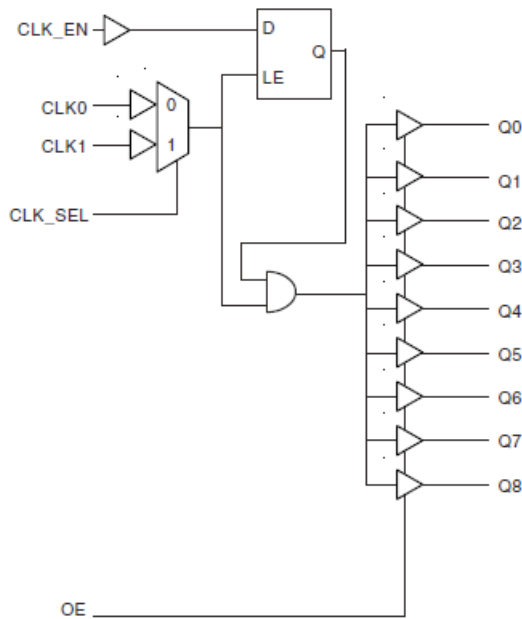
The 83947I is a low skew, 1-to-9 LVCMOS Fanout Buffer. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 9 to 18 byutilizing the ability of the outputs to drive two series terminated lines.

Guaranteed output and part-to-part skew characteristics make the 83947I ideal for high performance, single ended applications that also require a limited output voltage.

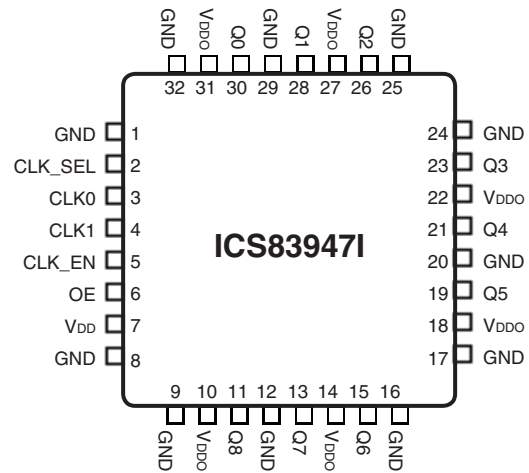
FEATURES

- 9 LVCMOS/LVTTL outputs
- Selectable CLK0 and CLK1 can accept the following input levels: LVCMOS and LVTTL
- Maximum output frequency: 110MHz
- Output skew: 500ps (maximum)
- Part-to-part skew: 2ns (maximum)
- 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Lead-Free package available

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 8, 9, 12, 16, 17, 20, 24, 25, 29, 32	GND	Power		Power supply ground.
2	CLK_SEL	Input	Pullup	Clock select input. When HIGH, selects CLK1. When LOW, selects CLK0. LVCMOS / LVTTTL interface levels.
3, 4	CLK0, CLK1	Input	Pullup	Reference clock inputs. LVCMOS / LVTTTL interface levels.
5	CLK_EN	Input	Pullup	Clock enable. LVCMOS / LVTTTL interface levels.
6	OE	Input	Pullup	Output enable. LVCMOS / LVTTTL interface levels.
7	V _{DD}	Power		Core supply pin.
10, 14, 18, 22, 27, 31	V _{DDO}	Power		Output supply pins.
11, 13, 15, 19, 21, 23, 26, 28, 30	Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	Output		Q0 thru Q8 clock outputs. LVCMOS / LVTTTL interface levels.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
C _{PD}	Power Dissipation Capacitance (per output)			25		pF
R _{PULLUP}	Input Pullup Resistor			51		KΩ
R _{PULLDOWN}	Input Pulldown Resistor			51		KΩ
R _{OUT}	Output Impedance		5	7	12	Ω

TABLE 3. OUTPUT ENABLE AND CLOCK ENABLE FUNCTION TABLE

Control Inputs		Output
OE	CLK_EN	Q0:Q8
0	X	Hi-Z
1	0	LOW
1	1	Follows CLK input

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to $V_{DD} + 0.5V$
Outputs, V_O	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 0.3V$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Coret Supply Voltage		3.0	3.3	3.6	V
V_{DDO}	Output Supply Voltage		3.0	3.3	3.6	V
I_{DD}	Input Supply Current			33	50	mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 0.3V$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		3.6	V
V_{IL}	Input Low Voltage				0.8	V
I_{IN}	Input Current	CLK0, CLK1, CLK_SEL, OE, CLK_EN	-100			μA
V_{OH}	Output High Voltage	$I_{OH} = -20\text{mA}$	2.5			V
V_{OL}	Output Low Voltage	$I_{OL} = 20\text{mA}$			0.4	V

TABLE 5. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 0.3V$, $T_A = -40^{\circ}C$ TO $85^{\circ}C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		110			MHz
t_{PD}	Propagation Delay, NOTE 1	CLK to Q	1.8		4.5	ns
tsk(o)	Output Skew; NOTE 2, 5	Measured on rising edge @ $V_{DDO}/2$			500	ps
tsk(pp)	Part-to-Part Skew; NOTE 3, 5	Measured on rising edge @ $V_{DDO}/2$			2	ns
t_{PW}	Output Pulse Width		tPeriod/2 - 800		tPeriod/2 + 800	ps
t_S	Clock Enable Setup Time; NOTE 6	CLK_EN to CLK	0			ns
t_H	Clock Enable Hold Time; NOTE 6	CLK_EN to CLK	1			ns
t_{ZL}, t_{ZH}	Output Enable Time; NOTE 4				11	ns
t_{LZ}, t_{HZ}	Output Disable Time; NOTE 4				11	ns
t_R	Output Rise Time	0.8V to 2.0V	0.2		1	ns
t_F	Output Fall Time	0.8V to 2.0V	0.2		1	ns

All parameters measured at f_{MAX} unless noted otherwise.

NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at $V_{DDO}/2$.

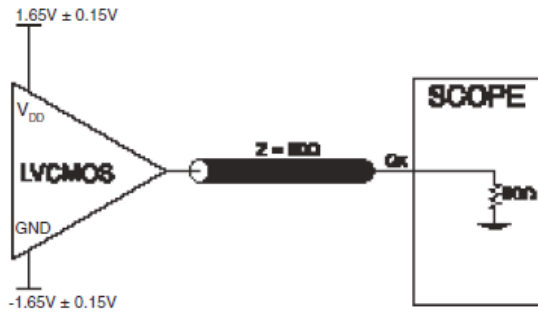
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.

NOTE 4: These parameters are guaranteed by characterization. Not tested in production.

NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 6: Setup and Hold times are relative to the rising edge of the input clock.

PARAMETER MEASUREMENT INFORMATION



3.3V OUTPUT LOAD AC TEST CIRCUIT



OUTPUT SKEW



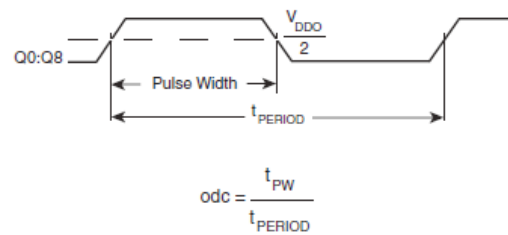
PART-TO-PART SKEW



PROPAGATION DELAY



OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 32 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for 839471 is: 1040

PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD LQFP

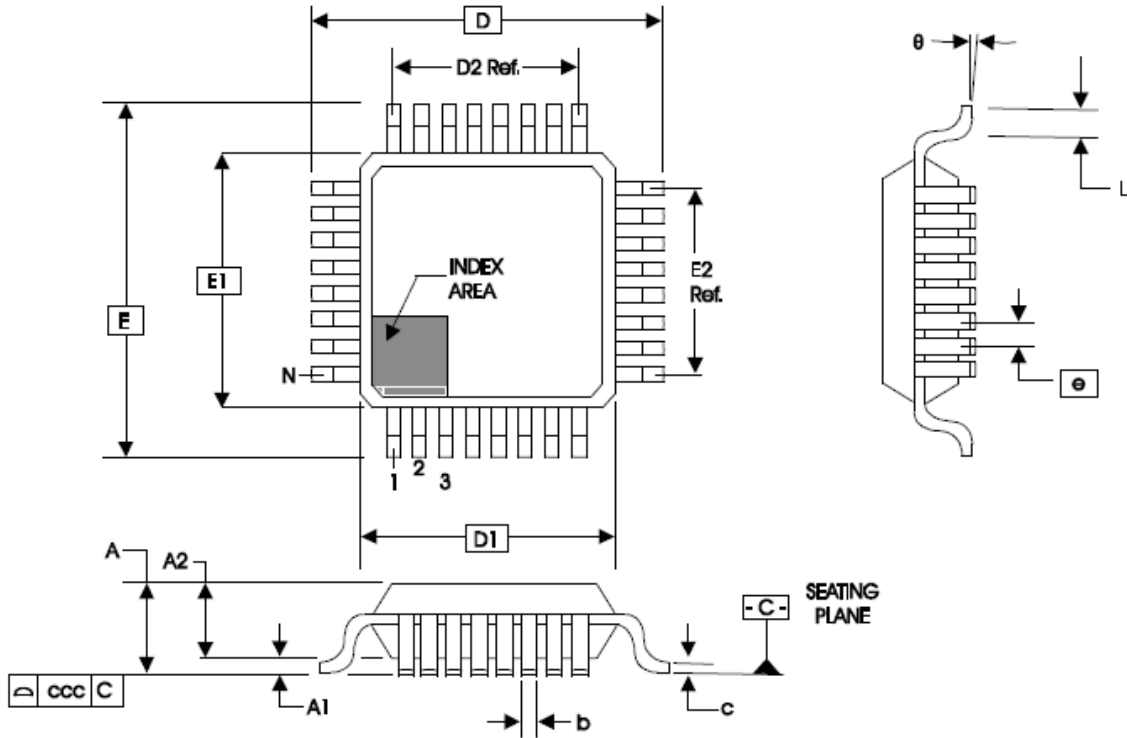


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N	32		
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D	9.00 BASIC		
D1	7.00 BASIC		
D2	5.60 Ref.		
E	9.00 BASIC		
E1	7.00 BASIC		
E2	5.60 Ref.		
e	0.80 BASIC		
L	0.45	0.60	0.75
theta	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
83947AYILN	ICS3947AYIN	32 Lead "Lead-Free/Annealed" LQFP	tray	-40°C to 85°C
83947AYILNT	ICS3947AYIN	32 Lead "Lead-Free/Annealed" LQFP	Tape & Reel	-40°C to 85°C

REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
A	T5	4	AC Characteristics Table, t_s and t_H rows- revised Test Conditions to read CLK_EN to CLK.	6/21/02
B	T2	1	Added Lead Free bullet in Features section.	10/11/04
	T8	2	Pin Characteristics Table - changed C_{IN} from 4pF max. to 4pF min. R_{OUT} added 5 Ω min and 12 Ω max.	
B	T8	8	Ordering Information Table - add Lead-Free part.	8/9/10
		10	Updated format throughout data sheet.	
B	T8	8	Updated datasheet's header/footer with IDT from ICS.	11/10/14
		10	Removed ICS prefix from Part/Order Number column. Added Contact Page.	
B	T8	8	Updated datasheet format Ordering information - removed leaded part numbers - PDN CQ-13-02 expired	3/17/16
B			Removed ICS from part number where needed. Updated header and footer.	

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.