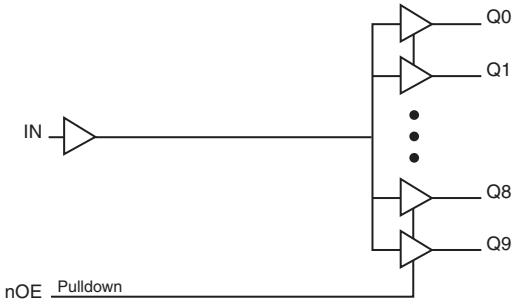
General Description

The 83210 is a low skew, 1-to-10 HSTL Fanout Buffer. The class II HSTL outputs are balanced push-pull in design, capable of delivering 16mA into a 10pF load. This class allows both source series termination and symmetrically double parallel termination.

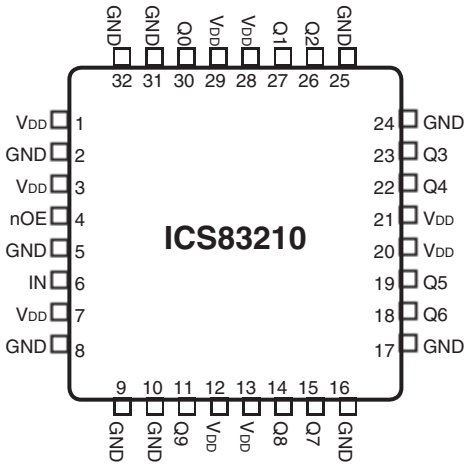
Features

- Ten single-ended HSTL outputs
- One single-ended HSTL clock input
- Maximum input frequency: 150MHz
- Output skew: 110ps (maximum)
- Part-to-part skew: 2ns (maximum)
- 1.5V power supply
- 0°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



32-Lead TQFP
7mm x 7mm x 1.0mm package body
Y package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 3, 7, 12, 13, 20, 21, 28, 29	V_{DD}	Power		Power supply pins.
2, 5, 8, 9, 10, 16, 17, 24, 25, 31, 32	GND	Power		Power supply ground.
4	nOE	Input	Pulldown	Output enable/disable input pin. When LOW, outputs Qx outputs are enabled. When HIGH, Qx outputs are disabled low. LVCMOS/LVTTL interface levels.
5	IN	Input		Single-ended reference clock input. HSTL interface levels.
11, 14, 15, 18, 19, 22, 23, 26, 27, 30	Q9, Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	Output		Single-ended HSTL clock outputs.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{OUT}	Output Pin Capacitance			4.5	6	pF
R_{OUT}	Output Impedance			20		Ω

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	75.5°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 3A. Power Supply DC Characteristics, V_{DD} = 1.5V ± 8%, TA = 0°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		1.38	1.5	1.62	V
I_{DD}	Power Supply Current	Outputs Loaded @ 62.5MHz		215	250	mA
I_{DDQ}	Quiescent Supply Current	V_{IN} = 0V, outputs disabled			1	mA

Table 3B. LVCMOS / LVTTL DC Characteristics, V_{DD} = 1.5V ± 8%, TA = 0°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	nOE		0.7*V_{DD}		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	nOE		-0.3		0.3*V_{DD}	V
I_{IH}	Input High Current	nOE				150	µA
I_{IL}	Input Low Current	nOE		-5			µA

Table 3C. HSTL DC Characteristics, V_{DD} = 1.5V ± 8%, TA = 0°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	IN	V_{REF} = 0.75V	0.85		1.8	V
V_{IL}	Input Low Voltage	IN		-0.3		0.65	V
V_{OH}	Output High Voltage		I_{OH} = -16mA	1.0		V_{DD} + 0.3	V
V_{OL}	Output Low Voltage		I_{OL} = 16mA	-0.3		0.4	V

TABLE 4. AC CHARACTERISTICS, V_{DD} = 1.5V ± 8%, T_A = 0°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency				150	MHz
t_{PLH}	Propagation Delay, Low-to-High; NOTE 1		1.0		5.5	ns
t_{PHL}	Propagation Delay, High-to-Low NOTE 1		1.0		5.5	ns
tsk(o)	Output Skew; NOTE 2, 4				110	ps
tsk(pp)	Part-to-Part Skew; NOTE 3, 4				2	ns
t_{EN}	Output Enable Time				7	ns
t_{DIS}	Output Disable Time				7	ns
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		1.3	ns
odc	Output Duty Cycle	Fout ≤ 100MHz	48		52	%
		Fout > 100MHz	45		55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

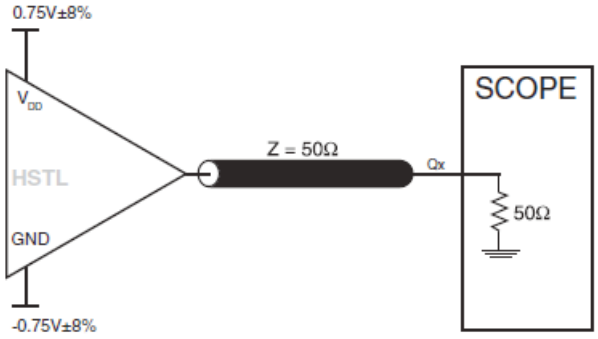
NOTE 1: Measured from the $V_{DD}/2$ of the input to $V_{DD}/2$ of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DD}/2$ of the output.

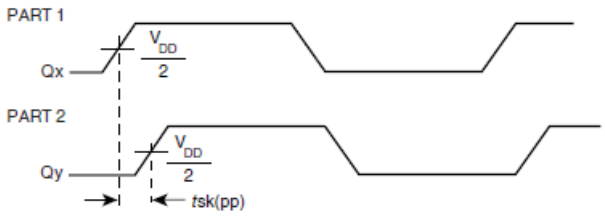
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions at the same temperature. Using the same type of inputs on each device, the outputs are measured at $V_{DD}/2$ of the output.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

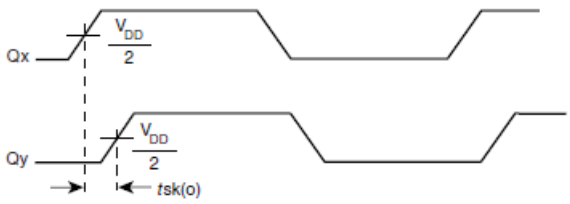
Parameter Measurement Information



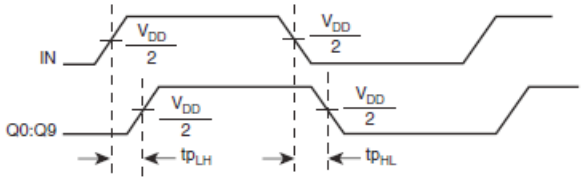
1.5V Output Load AC Test Circuit



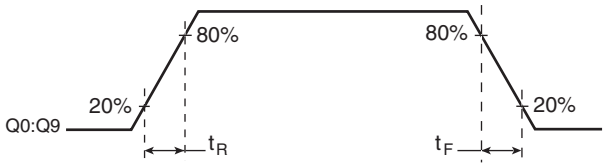
Part-to-Part Skew



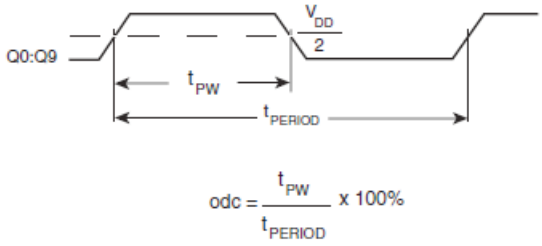
Output Skew



Propagation Delay



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

Applications Information

Recommendations for Unused Output Pins

Outputs:

HSTL Outputs

All unused HSTL outputs can be left floating. We recommend that there is no trace attached.

Reliability Information

Table 5. θ_{JA} vs. Air Flow Table for 32 Lead TQFP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	75.5°C/W	65.8°C/W	62.2°C/W

Transistor Count

The transistor count for 83210 is: 218

Package Outline - Y Suffix for 32 Lead TQFP

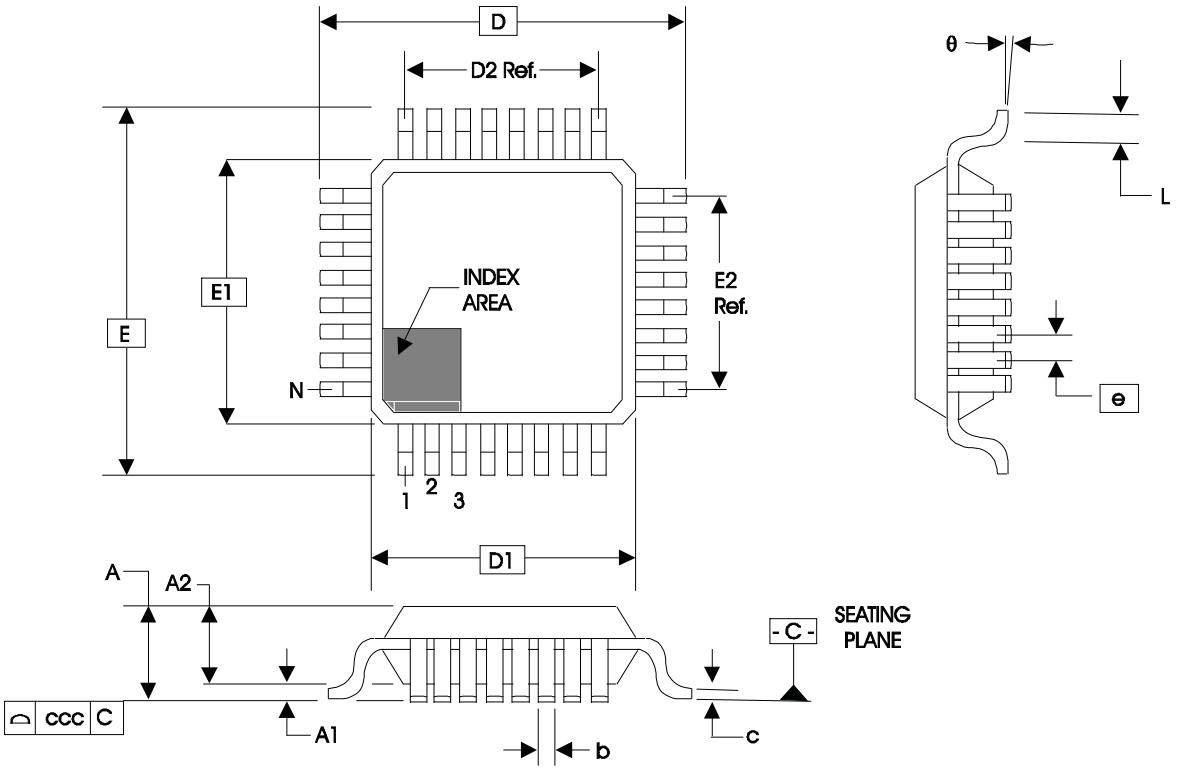


Table 6. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	ABA-HD		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.20
A1	0.05	--	0.15
A2	0.95	1.00	1.05
b	0.30	0.35	0.40
c	0.09	--	0.20
D & E		9.00 BASIC	
D1 & E1		7.00 BASIC	
D2 & E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
83210AYLF	ICS83210AYLF	32 lead “Lead-Free” TQFP	tray	0°C to 85°C
83210AYLFT	ICS83210AYLF	32 lead “Lead-Free” TQFP	tape & reel	0°C to 85°C

REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
A	T3C T4 T7	3 4 7 8	HSTL DC Characteristics Table - deleted NOTE 1, does not apply. AC Characteristics Table - added thermal note. Updated Package Outline. Ordering Information Table - Deleted “ICS” prefix from Part/Order Number column. Changed DT format header/footer.	9/9/10
A	T7	8	Ordering Information - removed leaded devices. Updated data sheet format.	4/28/15
A	T7	8	Removed ICS from the part number where needed. Ordering Information - Deleted LF note below table. Updated Header and footer.	3/10/16

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