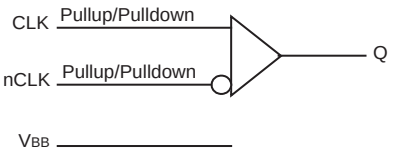
Description

830S21I is a 1-to-1 Differential-to- LVCMOS/ LVTTL translator and a member of the family of High Performance Clock Solutions from IDT. The differential input is highly flexible and can accept the following input types: LVPECL, LVDS, LVHSTL, SSTL and HCSL. The small 8-lead SOIC footprint makes this device ideal for use in applications with limited board space.

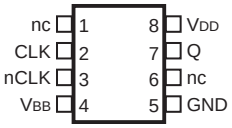
Features

- One LVCMOS/LVTTL output
- Differential CLK, nCLK input pair
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum output frequency: 350MHz
- Part-to-part skew: 525ps (maximum)
- Additive Phase jitter, RMS: 0.11ps (typical)
- Small 8 lead SOIC package saves board space
- Full 3.3V and 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package
- Designed for the fanout of 1PPS signals

Block Diagram



Pin Assignment



830S21I

8-Lead SOIC
3.9 × 4.9 × 1.375 mm package body
M Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 6	nc	Unused		No connect.
2	CLK	Input	Pullup/ Pulldown	Non-inverting differential clock input.
3	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input.
4	V_{BB}	Output		Output reference voltage.
5	GND	Power		Power supply ground.
7	Q	Output		Single-ended clock output. LVCMOS / LVTTL interface levels.
8	V_{DD}	Power		Positive supply pin.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance	V_{DD} = 3.465V		10		pF
		V_{DD} = 2.625V		8		pF
R_{OUT}	Output Impedance	V_{DD} = 3.3V		10		Ω
		V_{DD} = 2.5V		12		Ω

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	93.1°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				12	mA

Table 3B. Power Supply DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				11	mA

Table 3C. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage; NOTE 1	V_{DD} = 3.3V	2.6			V
		V_{DD} = 2.5V	1.8			V
V_{OL}	Output Low Voltage; NOTE 1	V_{DD} = 3.3V or 2.5V			0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DD}/2. See Parameter Measurement Information, *Output Load Test Circuit diagrams.*

Table 3D. Differential DC Characteristics, V_{DD} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
I_{IH}	Input High Current	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1		0.15		1.5	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2		GND + 0.5		V_{DD} – 0.85	V
V_{BB}	Output Voltage Reference		V_{DD} – 1.4	V_{DD} – 1.3	V_{DD} – 1.2	V

NOTE 1:V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

AC Electrical Characteristics

Table 4A. AC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Unit
f_{MAX}	Output Frequency			350		MHz
t_{PD}	Propagation Delay, NOTE 1		0.95		1.95	ns
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3				525	ps
*t*jit	Buffer Additive Phase jitter, RMS; refer to Additive Phase Jitter Section	350MHz, Integration Range (12kHz – 20MHz)		0.11	1	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	85		500	ps
odc	Output Duty Cycle	$f \leq$ 266MHz	47		53	%

NOTE 1: Measured from the differential input crossing point to the output at V_{DD}/2.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DD}/2.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

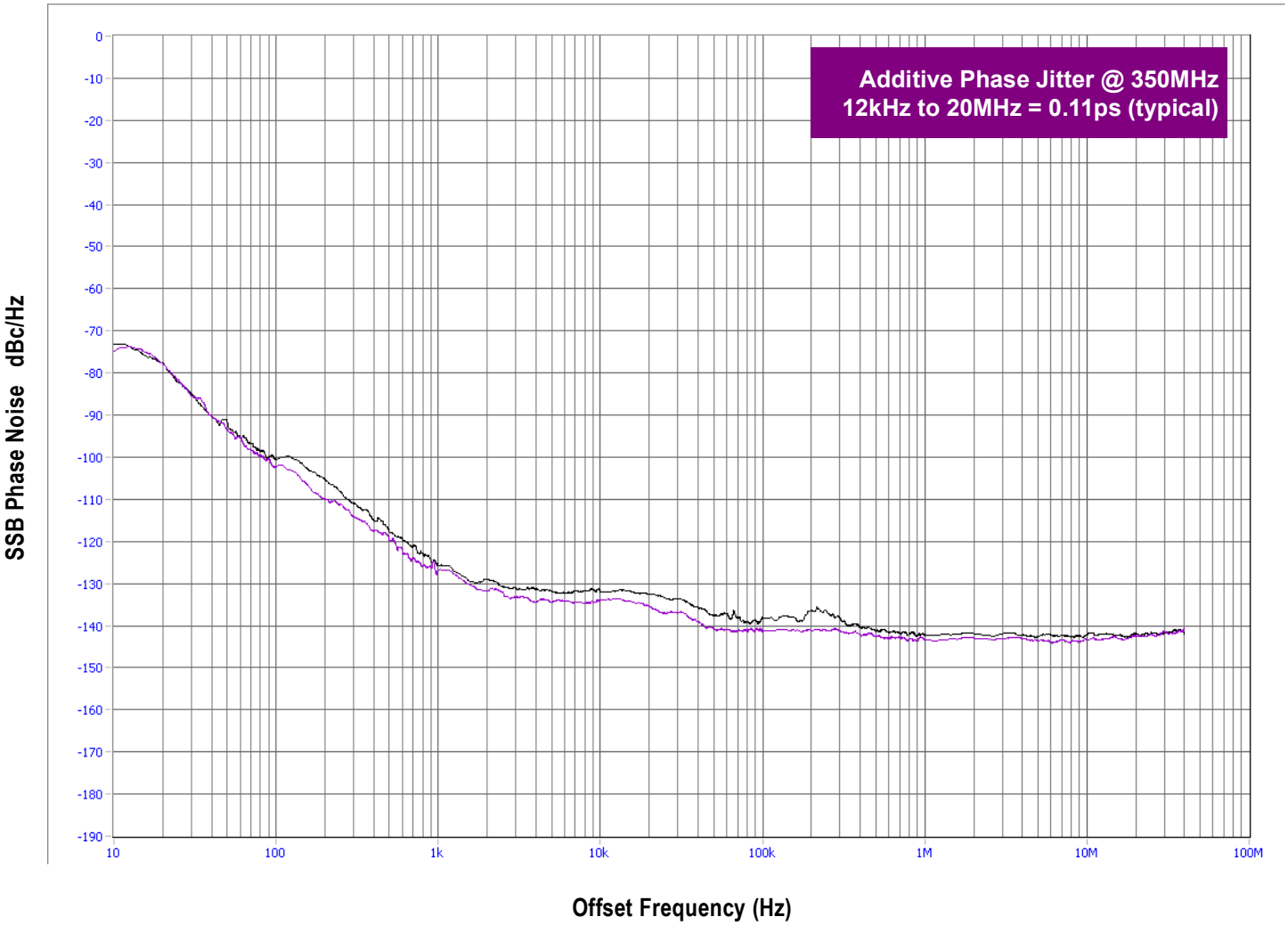
Table 4B. AC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Unit
f_{MAX}	Output Frequency			350		MHz
t_{PD}	Propagation Delay, NOTE 1		1		2	ns
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3				550	ps
*t*jit	Buffer Additive Phase jitter, RMS; refer to Additive Phase Jitter Section	350MHz, Integration Range (12kHz – 20MHz)		0.11	1	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	125		500	ps
odc	Output Duty Cycle	$f \leq$ 266MHz	47		53	%

NOTE 1: Measured from the differential input crossing point to the output at V_{DD}/2.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DD}/2.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

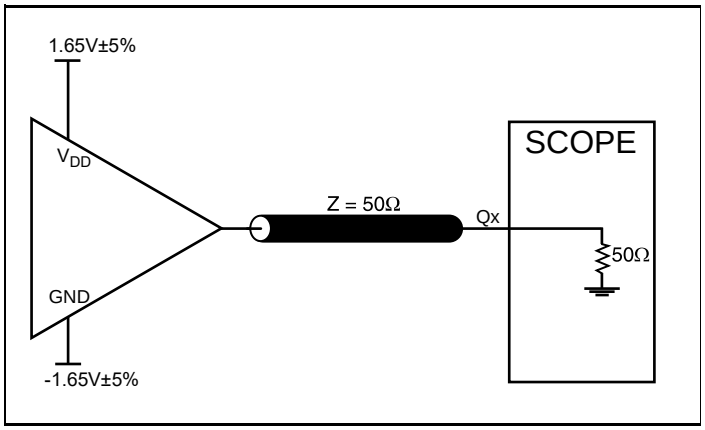
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

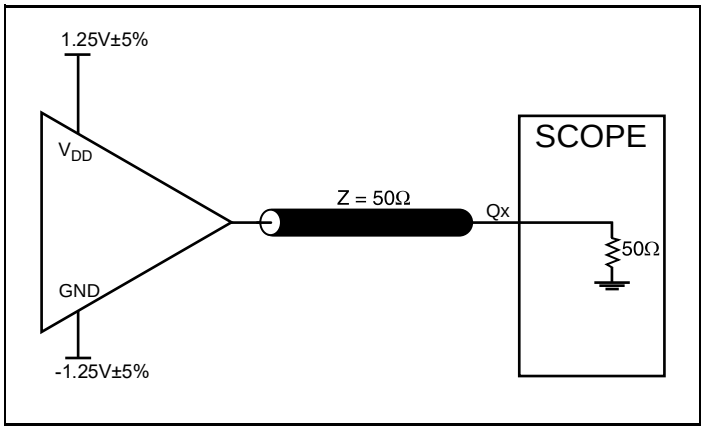


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

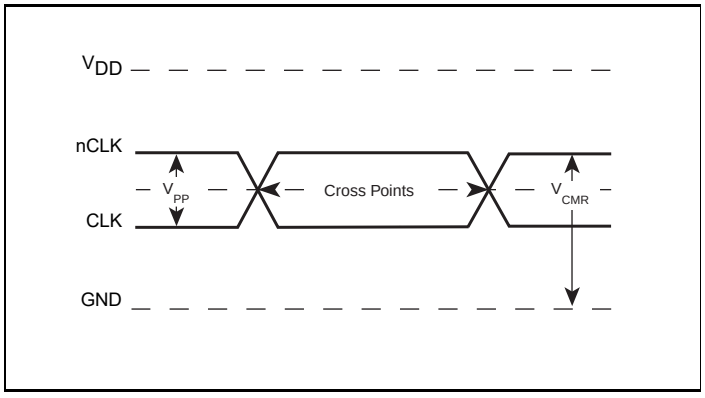
Parameter Measurement Information



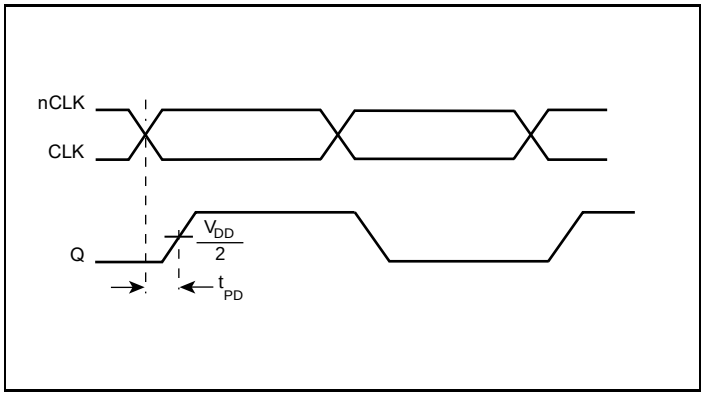
3.3V Core/3.3V LVCMOS Output Load AC Test Circuit



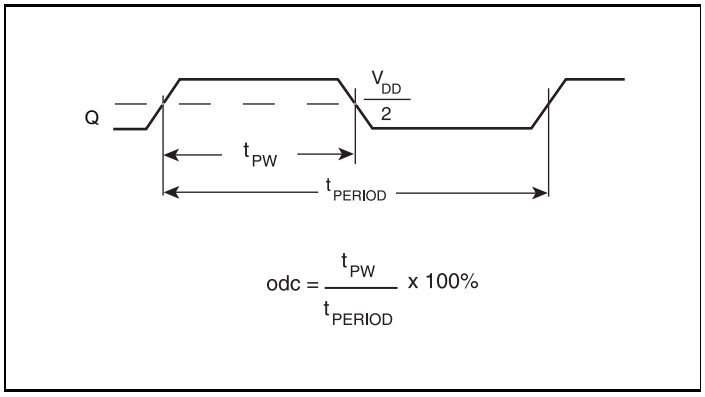
2.5V Core/2.5V LVCMOS Output Load AC Test Circuit



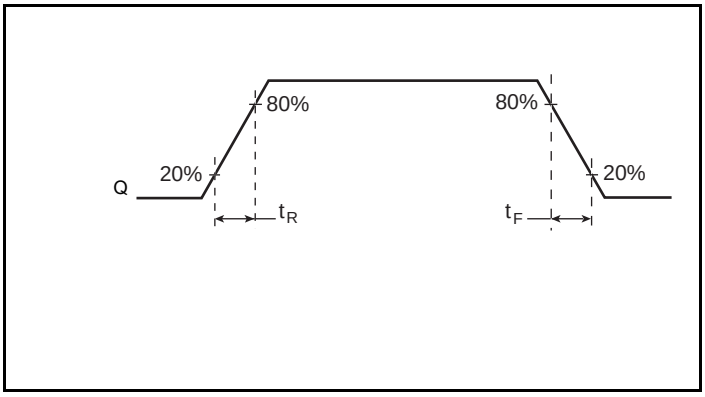
Differential Input Level



Propagation Delay

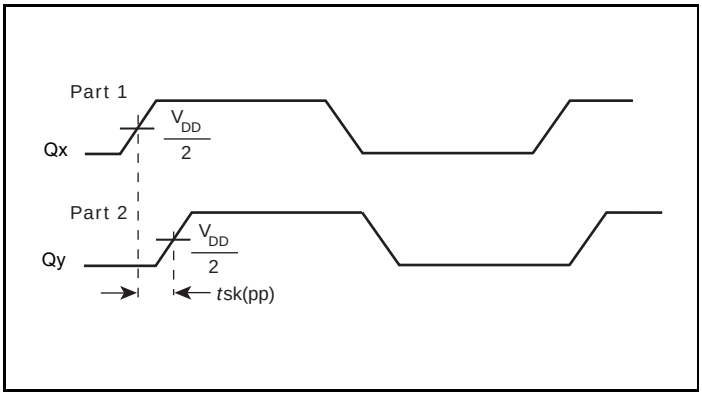


Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Parameter Measurement Information, continued



Part-to-Part Skew

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

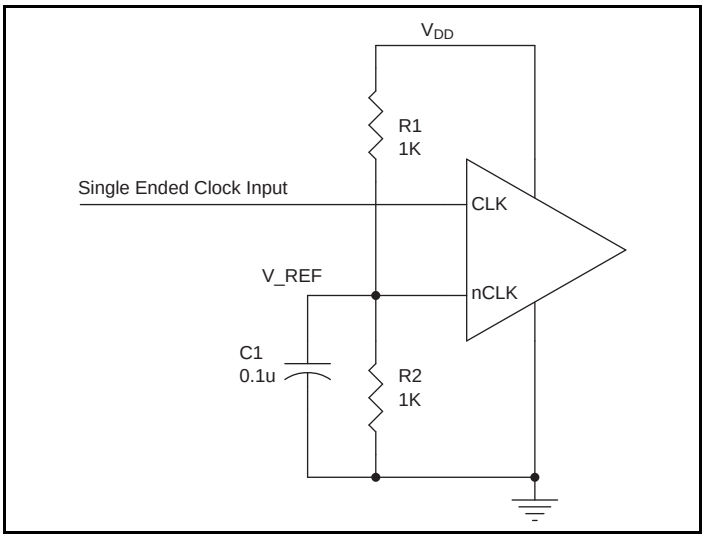


Figure 1. Single-Ended Signal Driving Differential Input

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2F* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

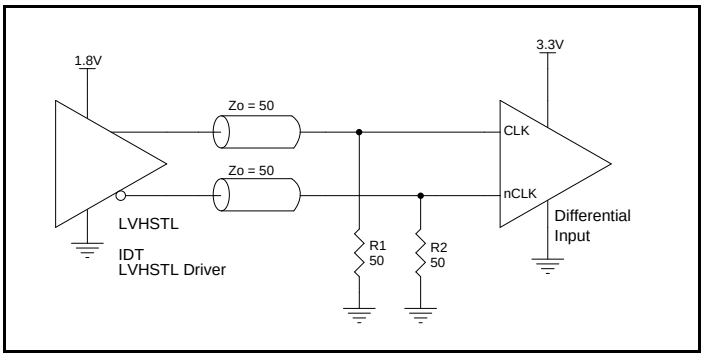


Figure 2A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver

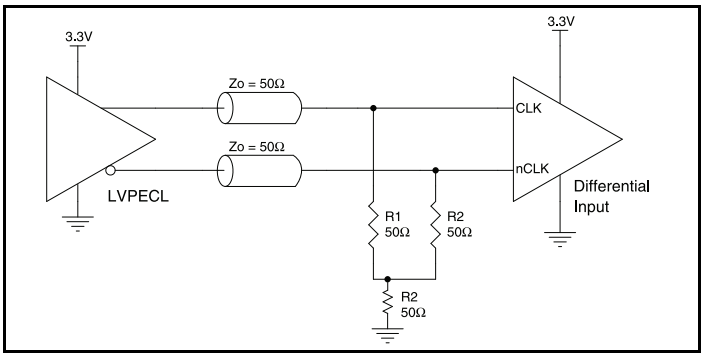


Figure 2B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

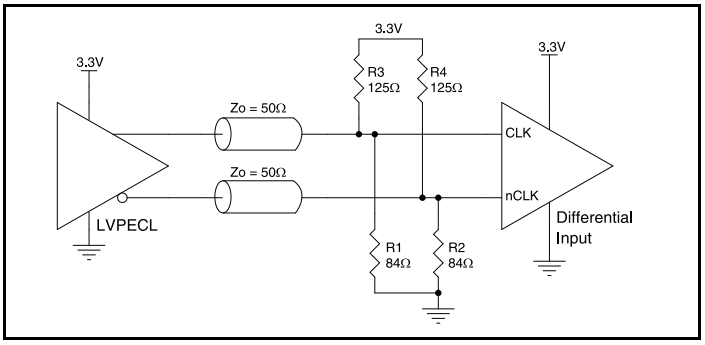


Figure 2C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

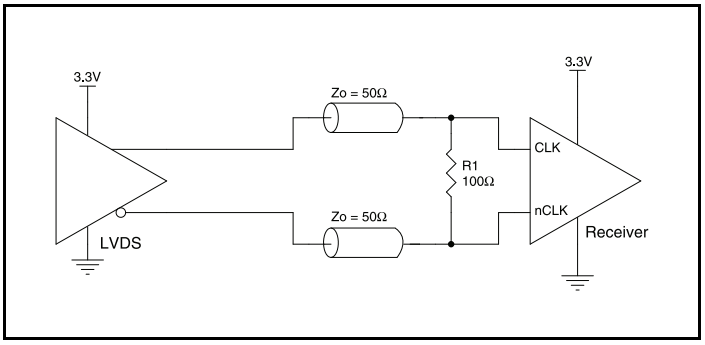


Figure 2D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

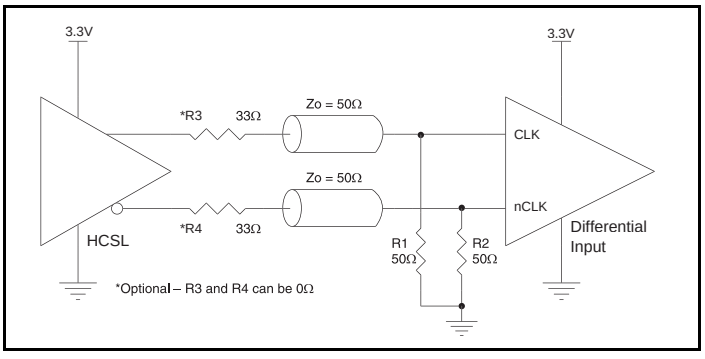


Figure 2E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver

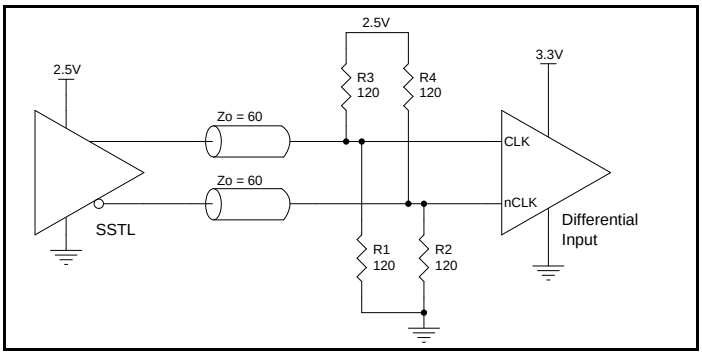


Figure 2F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver

Reliability Information

Table 5. θ_{JA} vs. Air Flow Table for a 8 Lead SOIC

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	93.1°C/W	84.3°C/W	79.6°C/W

Transistor Count

The transistor count for 830s21I is: 214

Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

Ordering Information

Table 7. Ordering Information

Orderable Part Number	Marking	Package	Carrier Type	Temperature Range
830S21AMILF	30S21AIL	“Lead-Free” 8 Lead SOIC	Tube	-40°C to 85°C
830S21AMILFT	30S21AIL	“Lead-Free” 8 Lead SOIC	Tape & Reel	-40°C to 85°C

Revision History

Revision Date	Description
November 7, 2024	Added “Designed for the fanout of 1PPS signals” to Features list.
December 12, 2015	▪ Removed ICS Chip and HiPerClockS under General Description. ▪ Removed ICS in the part numbers. ▪ Removed LF note at the bottom of the Ordering Information table. ▪ Removed the quantity of 2500 from the Tape & Reel in the Ordering information table. ▪ Updated datasheet header and footer.

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