DUAL CHANNEL E1 SHORT HAUL LINE INTERFACE UNIT

IDT82V2052E

FEATURES:

- **Dual channel E1 short haul line interfaces**
- **Supports HPS (Hitless Protection Switching) for 1+1 protection without external relays**
- **Single 3.3 V power supply with 5 V tolerance on digital interfaces**
- **Meets or exceeds specifications in**
  - ANSI T1.102
  - ITU I.431, G.703, G.736, G.775 and G.823
  - ETSI 300-166, 300-233 and TBR12/13
- **Software programmable or hardware selectable on:**
  - Wave-shaping templates
  - Line terminating impedance (E1: 75 Ω/120 Ω)
  - Adjustment of arbitrary pulse shape
  - JA (Jitter Attenuator) position (receive path or transmit path)
  - Single rail/dual rail system interfaces
  - HDB3/AMI line encoding/decoding
  - Active edge of transmit clock (TCLK) and receive clock (RCLK)
  - Active level of transmit data (TDATA) and receive data (RDATA)
  - Receiver or transmitter power down
  - High impedance setting for line drivers
  - PRBS (Pseudo Random Bit Sequence) generation and detection with 2^{15}-1 PRBS polynomials
  - 16-bit BPV (Bipolar Pulse Violation) / Excess Zero/ PRBS error counter
  - Analog loopback, Digital loopback, Remote loopback
- **Adaptive receive sensitivity up to -20 dB (Host Mode only)**
- **Non-intrusive monitoring per ITU G.772 specification**
- **Short circuit protection and internal protection diode for line drivers**
- **LOS (Loss Of Signal) detection with programmable LOS levels (Host Mode only)**
- **AIS (Alarm Indication Signal) detection**
- **JTAG interface**
- **Supports serial control interface, Motorola and Intel Non-Multiplexed interfaces and hardware control mode**
- **Pin compatible to 82V2082 T1/E1/J1 Long Haul/Short Haul LIU and 82V2042E T1/E1/J1 Short Haul LIU**
- **Available in 80-pin TQFP**
  Green package options available

DESCRIPTION:

The IDT82V2052E is a dual channel E1 Line Interface Unit. The IDT82V2052E performs clock/data recovery, AMI/HDB3 line decoding and detects and reports the LOS conditions. An integrated Adaptive Equalizer is available to increase the receive sensitivity and enable programming of LOS levels. In transmit path, there is an AMI/HDB3 encoder and Waveform Shaper. There is one Jitter Attenuator, which can be placed in either the receive path or the transmit path. The Jitter Attenuator can also be disabled. The IDT82V2052E supports both Single Rail and Dual Rail system interfaces. To facilitate the network maintenance, a PRBS generation/detection circuit is integrated in the chip, and different types of loopbacks can be set according to the applications. Two different kinds of line terminating impedance, 75 Ω and 120 Ω are selectable on a per channel basis. The chip also provides driver short-circuit protection and internal protection diode and supports JTAG boundary scanning. The chip can be controlled by either software or hardware.

The IDT82V2052E can be used in LAN, WAN, Routers, Wireless Base Stations, IADs, IMAs, IMAPs, Gateways, Frame Relay Access Devices, CSU/DSU equipment, etc.

FUNCTIONAL BLOCK DIAGRAM

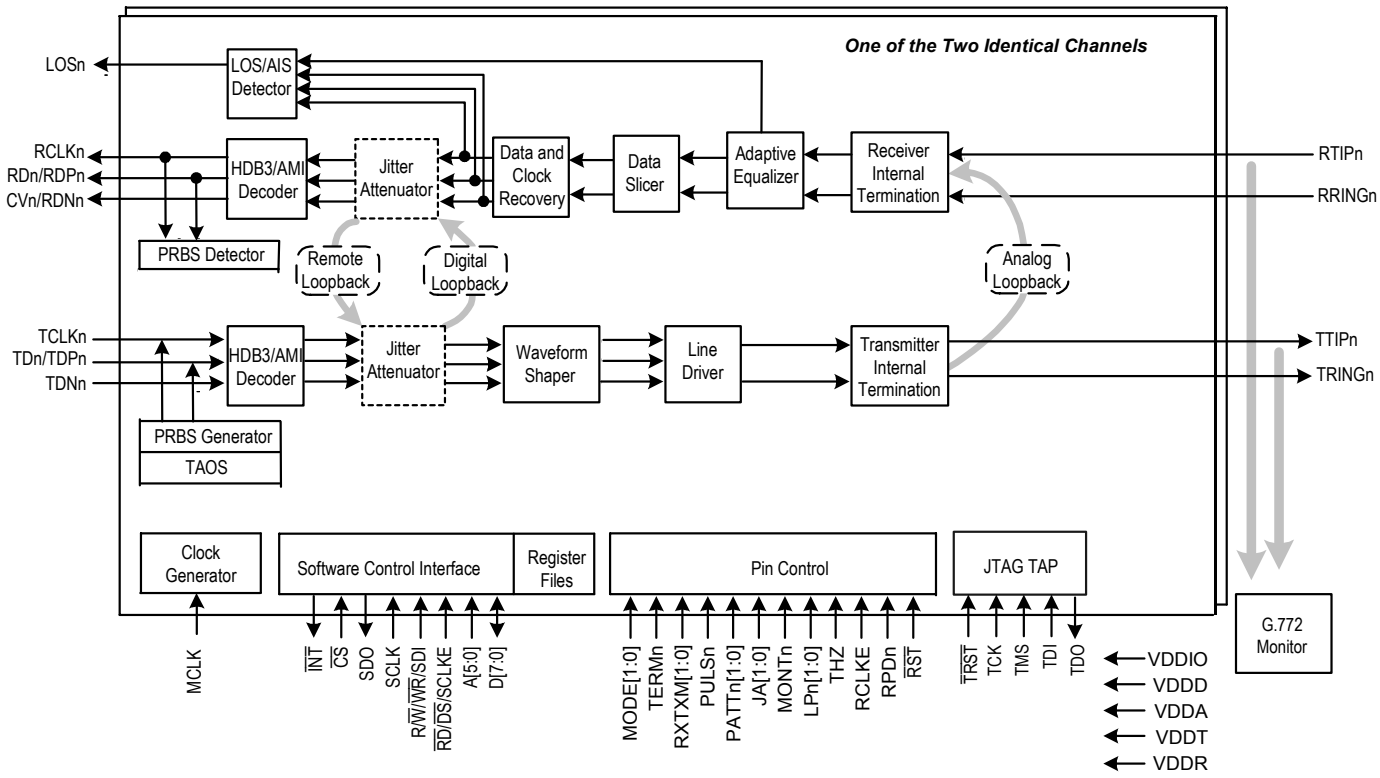

Figure-1 Block Diagram

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1 IDT82V2052E PIN CONFIGURATIONS

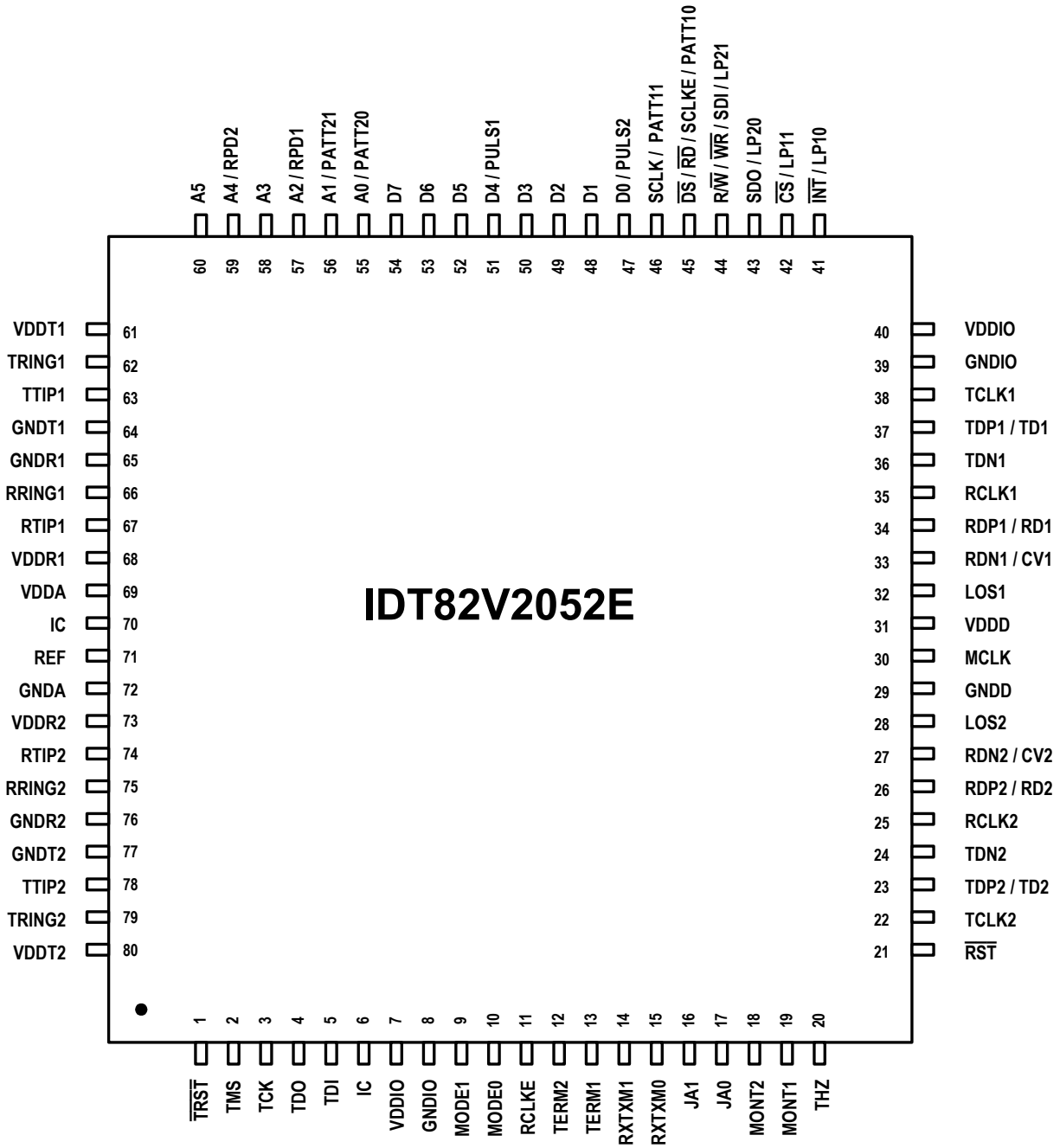


Figure-2 IDT82V2052E TQFP80 Package Pin Assignment

2 PIN DESCRIPTION

Table-1 Pin Description

Name	Type	Pin No.	Description
TTIP1 TTIP2 TRING1 TRING2	Analog Output	63 78 62 79	**TTIPn[1]/TRINGn: Transmit Bipolar Tip/Ring for Channel 1~2** These pins are the differential line driver outputs and can be set to high impedance state globally or individually. A logic high on THZ pin turns all these pins into high impedance state. When THZ bit (**TCF1, 03H...**)[2] is set to '1', the TTIPn/TRINGn in the corresponding channel is set to high impedance state. In summary, these pins will become high impedance in the following conditions: • THZ pin is high: all TTIPn/TRINGn enter high impedance; • THZn bit is set to 1: the corresponding TTIPn/TRINGn become high impedance; • Loss of MCLK: all TTIPn/TRINGn pins become high impedance;· • Loss of TCLKn: the corresponding TTIPn/TRINGn become HZ (exceptions: Remote Loopback; Transmit internal pattern by MCLK); • Transmitter path power down: the corresponding TTIPn/TRINGn become high impedance; • After software reset; pin reset and power on: all TTIPn/TRINGn enter high impedance.
RTIP1 RTIP2 RRING1 RRING2	Analog Input	67 74 66 75	**RTIPn/RRINGn: Receive Bipolar Tip/Ring for Channel 1~2** These signals are the differential receiver inputs.
TD1/TDP1 TD2/TDP2 TDN1 TDN2	I	37 23 36 24	**TDn: Transmit Data for Channel 1~2** When the device is in single rail mode, the NRZ data to be transmitted is input on this pin. Data on TDn pin is sampled into the device on the active edge of TCLKn and is encoded by AMI or HDB3 line code rules before being transmitted. In this mode, TDNn should be connected to ground. **TDPn/TDNn: Positive/Negative Transmit Data** When the device is in dual rail mode, the NRZ data to be transmitted for positive/negative pulse is input on these pins. Data on TDPn/TDNn pin is sampled into the device on the active edge of TCLKn. The active polarity is also selectable. Refer to 3.2.1 TRANSMIT PATH SYSTEM INTERFACE for details. The line code in dual rail mode is as follows: **TDPn / TDNn / Output Pulse** 0 / 0 / Space 0 / 1 / Positive Pulse 1 / 0 / Negative Pulse 1 / 1 / Space
TCLK1 TCLK2	I	38 22	**TCLKn: Transmit Clock for Channel 1~2** This pin inputs a 2.048 MHz transmit clock. The transmit data at TDn/TDPn or TDNn is sampled into the device on the active edge of TCLKn. If TCLKn is missing[3] and the TCLKn missing interrupt is not masked, an interrupt will be generated.

Notes:

1. The footprint 'n' (n = 1~2) represents one of the two channels.
2. The name and address of the registers that contain the preceding bit. Only the address of channel 1 register is listed, the rest addresses are represented by '...'. Users can find these omitted addresses in the *Register Description* section.
3. TCLKn missing: the state of TCLKn continues to be high level or low level over 70 MCLK cycles.

Table-1 Pin Description (Continued)

Name	Type	Pin No.	Description
RD1/RDP1 RD2/RDP2 CV1/RDN1 CV2/RDN2	O	34 26 33 27	**RDn: Receive Data output for Channel 1~2** In single rail mode, this pin outputs NRZ data. The data is decoded according to AMI or HDB3 line code rules. **CVn: Code Violation indication** In single rail mode, the BPV/CV errors in received data stream will be reported by driving the CVn pin to high level for a full clock cycle. HDB3 line code violation can be indicated if the HDB3 decoder is enabled. When AMI decoder is selected, bipolar violation will be indicated. In hardware control mode, the EXZ, BPV/CV errors in received data stream are always monitored by the CVn pin if single rail mode is chosen. **RDPn/RDNn: Positive/Negative Receive Data output for Channel 1~2** In dual rail mode, these pins output the re-timed NRZ data when CDR is enabled, or directly outputs the raw RZ slicer data if CDR is bypassed. **Active edge and level select:** Data on RDPn/RDNn or RDn is clocked with either the rising or the falling edge of RCLKn. The active polarity is also selectable. Refer to 3.3.8 RECEIVE PATH SYSTEM INTERFACE for details.
RCLK1 RCLK2	O	35 25	**RCLKn: Receive Clock output for Channel 1~2** This pin outputs a 2.048 MHz receive clock. Under LOS conditions with AIS enabled (bit AISE=1), RCLKn is derived from MCLK. In clock recovery mode, this signal provides the clock recovered from the RTIPn/RRINGn signal. The receive data (RDn in single rail mode or RDPn and RDNn in dual rail mode) is clocked out of the device on the active edge of RCLKn. If clock recovery is bypassed, RCLKn is the exclusive OR (XOR) output of the dual rail slicer data RDPn and RDNn. This signal can be used in applications with external clock recovery circuitry.
MCLK	I	30	**MCLK: Master Clock input** A built-in clock system that accepts a 2.048 MHz reference clock. This reference clock is used to generate several internal reference signals: • Timing reference for the integrated clock recovery unit. • Timing reference for the integrated digital jitter attenuator. • Timing reference for microcontroller interface. • Generation of RCLKn signal during a loss of signal condition. • Reference clock to transmit All Ones, all zeros and PRBS pattern. Note that for ATAO and AIS, MCLK is always used as the reference clock. • Reference clock during Transmit All Ones (TAO) condition or sending PRBS in hardware control mode. The loss of MCLK will turn TTIP/TRING into high impedance status.
LOS1 LOS2	O	32 28	**LOSn: Loss of Signal Output for Channel 1~2** These pins are used to indicate the loss of received signals. When LOSn pin becomes high, it indicates the loss of received signal in channel n. The LOS pin will become low automatically when valid received signal is detected again. The criteria of loss of signal are described in 3.5 LOS AND AIS DETECTION.
REF	I	71	**REF: reference resister** An external resistor (3kΩ, 1%) is used to connect this pin to ground to provide a standard reference current for internal circuit.

Table-1 Pin Description (Continued)

<table>
<tr><th>Name</th><th>Type</th><th>Pin No.</th><th>Description</th></tr>
<tr><td>MODE1
MODE0</td><td>I</td><td>9
10</td><td>MODE[1:0]: operation mode of control interface select
The level on this pin determines which control mode is used to control the device as follows:
<table><tr><th>MODE[1:0]</th><th>Control Interface mode</th></tr><tr><td>00</td><td>Hardware interface</td></tr><tr><td>01</td><td>Serial Microcontroller Interface</td></tr><tr><td>10</td><td>Motorola non-multiplexed</td></tr><tr><td>11</td><td>Intel non-multiplexed</td></tr></table>• The serial microcontroller interface consists of $\overline{CS}$, SCLK, SCLKE, SDI, SDO and $\overline{INT}$ pins. SCLKE is used for the selection of the active edge of SCLK.
• The parallel non-multiplexed microcontroller interface consists of $\overline{CS}$, A[5:0], D[7:0], $\overline{DS}$/$\overline{RD}$, R/$\overline{W}$/$\overline{WR}$ and $\overline{INT}$ pins. (Refer to 3.11 MICROCONTROLLER INTERFACES for details)
• Hardware interface consists of PULSn, THZ, RCLKE, LPn[1:0], PATTn[1:0], JA[1:0], MONTn, TERMn, RPDn, MODE[1:0] and RXTXM[1:0] (n=1, 2).</td></tr>
<tr><td>RCLKE</td><td>I</td><td>11</td><td>RCLKE: the active edge of RCLKn select
In hardware control mode, this pin selects the active edge of RCLKn
• L= update RDPn/RDNn on the rising edge of RCLKn
• H= update RDPn/RDNn on the falling edge of RCLKn
In software control mode, this pin should be connected to GNDIO.</td></tr>
<tr><td>RXTXM1
RXTXM0</td><td>I</td><td>14
15</td><td>RXTXM[1:0]: Receive and transmit path operation mode select
In hardware control mode, these pins are used to select the single rail or dual rail operation modes as well as AMI or HDB3 line coding:
• 00= single rail with HDB3 coding
• 01= single rail with AMI coding
• 10= dual rail interface with CDR enabled
• 11= slicer mode (dual rail interface with CDR disabled)
In software control mode, these pins should be connected to ground.</td></tr>
<tr><td>$\overline{CS}$

LP11</td><td>I</td><td>42</td><td>$\overline{CS}$: Chip Select
In serial or parallel microcontroller interface mode, this is the active low enable signal. A low level on this pin enables serial or parallel microcontroller interface.

LP11/LP10: Loopback mode select for channel 1
When the chip is configured by hardware, this pin is used to select loopback operation modes for channel 1.:
• 00 = no loopback
• 01 = analog loopback
• 10 = digital loopback
• 11 = remote loopback</td></tr>
<tr><td>$\overline{INT}$

LP10</td><td>O

I</td><td>41</td><td>$\overline{INT}$: Interrupt Request
In software control mode, this pin outputs the general interrupt request for all interrupt sources. If INTM_GLB bit (GCF, 20H) is set to ‘1’, all the interrupt sources will be masked. These interrupt sources can be masked individually via registers (INTM0, 13H...) and (INTM1, 14H...). The interrupt status is reported via the registers (INTCH, 21H), (INTS0, 18H...) and (INTS1, 19H...).

Output characteristics of this pin can be defined to be push-pull (active high or active low) or open-drain (active low) by setting bits INT_PIN[1:0] (GCF, 20H)

LP11/LP10: Loopback mode select for channel 1
See above LP11.</td></tr>
</table>

Table-1 Pin Description (Continued)

<table>
<tr><th>Name</th><th>Type</th><th>Pin No.</th><th>Description</th></tr>
<tr><td>SCLK</td><td>I</td><td>46</td><td>SCLK: Shift Clock
In serial microcontroller interface mode, this signal is the shift clock for the serial interface. Configuration data on SDI pin is sampled on the rising edge of SCLK. Configuration and status data on SDO pin is clocked out of the device on the rising edge of SCLK if SCLKE pin is low, or on the falling edge of SCLK if SCLKE pin is high.
In parallel non-multiplexed interface mode, this pin should be connected to ground.</td></tr>
<tr><td>PATT11</td><td></td><td></td><td>PATT11/PATT10: Transmit pattern select for channel 1
In hardware control mode, this pin selects the transmit pattern
• 00 = normal
• 01= All Ones
• 10= PRBS
• 11= transmitter power down</td></tr>
<tr><td>SCLKE</td><td>I</td><td>45</td><td>SCLKE: Serial Clock Edge Select
In serial microcontroller interface mode, this signal selects the active edge of SCLK for outputting SDO. The output data is valid after some delay from the active clock edge. It can be sampled on the opposite edge of the clock. The active clock edge which clocks the data out of the device is selected as shown below:
<table><tr><th>SCLKE</th><th>SCLK</th></tr><tr><td>Low</td><td>Rising edge is the active edge.</td></tr><tr><td>High</td><td>Falling edge is the active edge.</td></tr></table></td></tr>
<tr><td>$\overline{DS}$</td><td></td><td></td><td>$\overline{DS}$: Data Strobe
In Motorola parallel non-multiplexed interface mode, this signal is the data strobe of the parallel interface. In a write operation (R/$\overline{W}$ = 0), the data on D[7:0] is sampled into the device. In a read operation (R/$\overline{W}$ = 1), the data is driven to D[7:0] by the device.</td></tr>
<tr><td>$\overline{RD}$</td><td></td><td></td><td>$\overline{RD}$: Read Strobe
In Intel parallel non-Multiplexed interface mode, the data is driven to D[7:0] by the device during low level of $\overline{RD}$ in a read operation.</td></tr>
<tr><td>PATT10</td><td></td><td></td><td>PATT11/PATT10: Transmit pattern select for channel 1
See above PATT11.</td></tr>
<tr><td>SDI</td><td>I</td><td>44</td><td>SDI: Serial Data Input
In serial microcontroller interface mode, this signal is the input data to the serial interface. Configuration data at SDI pin is sampled by the device on the rising edge of SCLK.</td></tr>
<tr><td>R/$\overline{W}$</td><td></td><td></td><td>R/$\overline{W}$: Read/Write Select
In Motorola parallel non-multiplexed interface mode, this pin is low for write operation and high for read operation.</td></tr>
<tr><td>$\overline{WR}$</td><td></td><td></td><td>$\overline{WR}$: Write Strobe
In Intel parallel non-multiplexed interface mode, this pin is asserted low by the microcontroller to initiate a write cycle. The data on D[7:0] is sampled into the device in a write operation.</td></tr>
<tr><td>LP21</td><td></td><td></td><td>LP21/LP20: loopback mode select for channel 2
When the chip is configured by hardware, this pin is used to select loopback operation modes for channel 2:.
• 00 = no loopback
• 01 = analog loopback
• 10 = digital loopback
• 11 = remote loopback</td></tr>
</table>

Table-1 Pin Description (Continued)

Name	Type	Pin No.	Description
SDO	O	43	**SDO: Serial Data Output** In serial microcontroller interface mode, this signal is the output data of the serial interface. Configuration or Status data at SDO pin is clocked out of the device on the rising edge of SCLK if SCLKE pin is low, or on the falling edge of SCLK if SCLKE pin is high. In parallel non-multiplexed interface mode, this pin should be left open.
LP20	I		**LP21/LP20: loopback mode select for channel 2** See above LP21.
D7	I/O	54	**D7: Data Bus bit7** In Intel/Motorola non-multiplexed interface mode, this signal is the bi-directional data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor. In Hardware mode, this pin has to be tied to GND.
D6	I/O	53	**D6: Data Bus bit6** In Intel/Motorola non-multiplexed interface mode, this signal is the bi-directional data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor. In Hardware mode, this pin has to be tied to GND.
D5	I/O	52	**D5: Data Bus bit5** In Intel/Motorola non-multiplexed interface mode, this signal is the bi-directional data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor. In Hardware mode, this pin has to be tied to GND.
D4	I/O	51	**D4: Data Bus bit4** In Intel/Motorola non-multiplexed interface mode, this signal is the bi-directional data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor.
PULS1	I		PULS1: This pin is used to select the following functions for Channel 1 in Hardware control mode: • Transmit pulse template • Internal termination impedance (75 Ω / 120 Ω) Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.
D3	I/O	50	**D3: Data Bus bit3** In Intel/Motorola non-multiplexed interface mode, this signal is the bi-directional data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor. In Hardware mode, this pin has to be tied to GND.
D2	I/O	49	**D2: Data Bus bit2** In Intel/Motorola non-multiplexed interface mode, this signal is the bi-directional data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor. In Hardware mode, this pin has to be tied to GND.
D1	I/O	48	**D1: Data Bus bit1** In Intel/Motorola non-multiplexed interface mode, this signal is the bi-directional data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor. In Hardware mode, this pin has to be tied to GND.

Table-1 Pin Description (Continued)

Name	Type	Pin No.	Description
D0	I/O	47	**D0: Data Bus bit0** In Intel/Motorola non-multiplexed interface mode, this signal is the bi-directional data bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground through a 10 kΩ resistor.
PULS2	I		PULS2: This pin is used to select the following functions for Channel 2 in Hardware control mode: • Transmit pulse template • Internal termination impedance (75 Ω / 120 Ω) Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.
A5	I	60	**A5: Address Bus bit5** In Intel/Motorola non-multiplexed interface mode, this signal is the address bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground. In Hardware mode, this pin has to be tied to GND.
A4	I	59	**A4: Address Bus bit4** In Intel/Motorola non-multiplexed interface mode, this signal is the address bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground.
RPD2			**RPD2: Power down control for receiver2 in hardware control mode** 0= receiver 2 normal operation 1= receiver 2 power down
A3	I	58	**A3: Address Bus bit3** In Intel/Motorola non-multiplexed interface mode, this signal is the address bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground. In Hardware mode, this pin has to be tied to GND.
A2	I	57	**A2: Address Bus bit2** In Intel/Motorola non-multiplexed interface mode, this signal is the address bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground.
RPD1			**RPD1: Power down control for receiver1 in hardware control mode** 0= receiver 1 normal operation 1= receiver 1 power down
A1	I	56	**A1: Address Bus bit1** In Intel/Motorola non-multiplexed interface mode, this signal is the address bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground.
PATT21			**PATT21/PATT20: Transmit pattern select for channel 2** In hardware control mode, this pin selects the transmit pattern 00 = normal 01= All Ones 10= PRBS 11= transmitter power down
A0	I	55	**A0: Address Bus bit 0** In Intel/Motorola non-multiplexed interface mode, this signal is the address bus of the microcontroller interface. In serial microcontroller interface mode, this pin should be connected to ground.
PATT20			See above
TERM1 TERM2	I	13 12	**TERMn: Selects internal or external impedance matching for channel 1 and channel 2 in hardware control mode** 0 = ternary interface with internal impedance matching network 1 = ternary interface with external impedance matching network In software control mode, this pin should be connected to ground.

Table-1 Pin Description (Continued)

Name	Type	Pin No.	Description
JA1	I	16	**JA[1:0]: Jitter attenuation position, bandwidth and the depth of FIFO select for channel 1 and channel 2 (only used in hardware control mode)** • 00 = JA is disabled • 01= JA in receiver, broad bandwidth, FIFO=64 bits • 10 = JA in receiver, narrow bandwidth, FIFO=128 bits • 11= JA in transmitter, narrow bandwidth, FIFO=128 bits In software control mode, this pin should be connected to ground.
JA0	I	17	See above.
MONT2	I	18	**MONT2: Receive Monitor gain select for channel 2** In hardware control mode with ternary interface, this pin selects the receive monitor gain of receiver: 0= 0dB 1= 26dB In software control mode, this pin should be connected to ground.
MONT1	I	19	**MONT1: Receive Monitor gain select for channel 1** In hardware control mode with ternary interface, this pin selects the receive monitor gain of receiver: 0= 0dB 1= 26dB In software control mode, this pin should be connected to ground.
$\overline{\text{RST}}$	I	21	**$\overline{\text{RST}}$: Hardware Reset** The chip is forced to reset state if a low signal is input on this pin for more than 100ns. MCLK must be active during reset.
THZ	I	20	**THZ: Transmitter Driver High Impedance Enable** This signal enables or disables all transmitter drivers on a global basis. A low level on this pin enables the driver while a high level on this pin places all drivers in high impedance state. Note that the functionality of the internal circuits is not affected by this signal.
JTAG Signals			
$\overline{\text{TRST}}$	I Pullup	1	**$\overline{\text{TRST}}$: JTAG Test Port Reset** This is the active low asynchronous reset to the JTAG Test Port. This pin has an internal pull-up resistor. To ensure deterministic operation of the test logic, TMS should be held high while the signal applied to $\overline{\text{TRST}}$ changes from low to high. For normal signal processing, this pin should be connected to ground. If JTAG is not used, this pin must be connected to ground.
TMS	I Pullup	2	**TMS: JTAG Test Mode Select** This pin is used to control the test logic state machine and is sampled on the rising edge of TCK. TMS has an internal pull-up resistor. If JTAG is not used, this pin may be left unconnected.
TCK	I	3	**TCK: JTAG Test Clock** This is the input clock for JTAG. The data on TDI and TMS are clocked into the device on the rising edge of TCK while the data on TDO is clocked out of the device on the falling edge of TCK. When TCK is idle at low state, all the stored-state devices contained in the test logic will retain their state indefinitely. If JTAG is not used, this pin may be left unconnected.
TDO	O	4	**TDO: JTAG Test Data Output** This output pin is high impedance normally and is used for reading all the serial configuration and test data from the test logic. The data on TDO is clocked out of the device on the falling edge of TCK. If JTAG is not used, this pin should be left unconnected.
TDI	I Pullup	5	**TDI: JTAG Test Data Input** This pin is used for loading instructions and data into the test logic and has an internal pull-up resistor. The data on TDI is clocked into the device on the rising edge of TCK. If JTAG is not used, this pin may be left unconnected.
Power Supplies and Grounds			
VDDIO	-	7,40	**3.3 V I/O power supply**
GNDIO	-	8,39	**I/O ground**

Table-1 Pin Description (Continued)

Name	Type	Pin No.	Description
VDDT1 VDDT2	-	61 80	3.3 V power supply for transmitter driver
GNDT1 GNDT2	-	64 77	Analog ground for transmitter driver
VDDR1 VDDR2	-	68 73	Power supply for receive analog circuit
GNDR1 GNDR2	-	65 76	Analog ground for receive analog circuit
VDDD	-	31	3.3V digital core power supply
GNDD	-	29	Digital core ground
VDDA	-	69	Analog core circuit power supply
GNDA	-	72	Analog core circuit ground
Others			
IC	-	70	**IC: Internal Connection** Internal Use. This pin should be left open in normal operation.
IC	-	6	**IC: Internal Connection** Internal Use. This pin should be connected to ground in normal operation.

3 FUNCTIONAL DESCRIPTION

3.1 CONTROL MODE SELECTION

The IDT82V2052E can be configured by software or by hardware. The software control mode supports Serial Control Interface, Motorola non-Multiplexed Control Interface and Intel non-Multiplexed Control Interface. The Control mode is selected by MODE1 and MODE0 pins as follows:

	Control Interface Mode
00	Hardware interface
01	Serial Microcontroller Interface.
10	Parallel -non-Multiplexed -Motorola Interface
11	Parallel -non-Multiplexed -Intel Interface

- The serial microcontroller Interface consists of $\overline{CS}$, SCLK, SCLKE, SDI, SDO and $\overline{INT}$ pins. SCLKE is used for the selection of active edge of SCLK.
- The parallel non-Multiplexed microcontroller Interface consists of $\overline{CS}$, A[5:0], D[7:0], $\overline{DS}$/$\overline{RD}$, R/$\overline{W}$/$\overline{WR}$ and $\overline{INT}$ pins.
- Hardware interface consists of PULSn, THZ, RCLKE, LPn[1:0], PATTn[1:0], JA[1:0], MONTn, TERMn, RPDn, MODE[1:0] and RXTXM[1:0] (n=1, 2). Refer to 5 HARDWARE CONTROL PIN SUMMARY for details about hardware control.

3.2 TRANSMIT PATH

The transmit path of each channel of IDT82V2052E consists of an Encoder, an optional Jitter Attenuator, a Waveform Shaper, a Line Driver and a Programmable Transmit Termination.

3.2.1 TRANSMIT PATH SYSTEM INTERFACE

The transmit path system interface consists of TCLKn pin, TDn/TDPn pin and TDNn pin. TCLKn is a 2.048 MHz clock. If TCLKn is missing for more than 70 MCLK cycles, an interrupt will be generated if it is not masked.

Transmit data is sampled on the TDn/TDPn and TDNn pins by the active edge of TCLKn. The active edge of TCLKn can be selected by the TCLK_SEL bit (**TCF0, 04H...**). And the active level of the data on TDn/TDPn and TDNn can be selected by the TD_INV bit (**TCF0, 04H...**). In hardware control mode, the falling edge of TCLKn and the active high of transmit data are always used.

The transmit data from the system side can be provided in two different ways: Single Rail and Dual Rail. In Single Rail mode, only TDn pin is used for transmitting data and the T_MD[1] bit (**TCF0, 04H...**) should be set to '0'. In Dual Rail Mode, both TDPn pin and TDNn pin are used for transmitting data, the T_MD[1] bit (**TCF0, 04H...**) should be set to '1'.

3.2.2 ENCODER

In Single Rail mode, the Encoder can be configured to be a HDB3 encoder or an AMI encoder by setting T_MD[0] bit (**TCF0, 04H...**).

In Dual Rail mode, the Encoder is by-passed. In Dual Rail mode, a logic '1' on the TDPn pin and a logic '0' on the TDNn pin results in a negative pulse on the TTIPn/TRINGn; a logic '0' on TDPn pin and a logic '1' on TDNn pin results in a positive pulse on the TTIPn/TRINGn. If both TDPn and TDNn are high or low, the TTIPn/TRINGn outputs a space (Refer to TDn/TDPn, TDNn Pin Description).

In hardware control mode, the operation mode of receive and transmit path can be selected by setting RXTXM1 and RXTXM0 pins on a global basis. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.

3.2.3 PULSE SHAPER

The IDT82V2052E provides two ways of manipulating the pulse shape before sending it. One is to use preset pulse templates; the other is to use user-programmable arbitrary waveform template.

In software control mode, the pulse shape can be selected by setting the related registers.

In hardware control mode, the pulse shape can be selected by setting PULSn pins on a per channel basis. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.

3.2.3.1 Preset Pulse Templates

The pulse shape is shown in Figure-3 according to the G.703 and the measuring diagram is shown in Figure-4. In internal impedance matching mode, if the cable impedance is 75 Ω, the PULS[3:0] bits (**TCF1, 05H...**) should be set to '0000'; if the cable impedance is 120 Ω, the PULS[3:0] bits (**TCF1, 05H...**) should be set to '0001'. In external impedance matching mode, for both E1/75 Ω and E1/120 Ω cable impedance, PULS[3:0] should be set to '0001'.

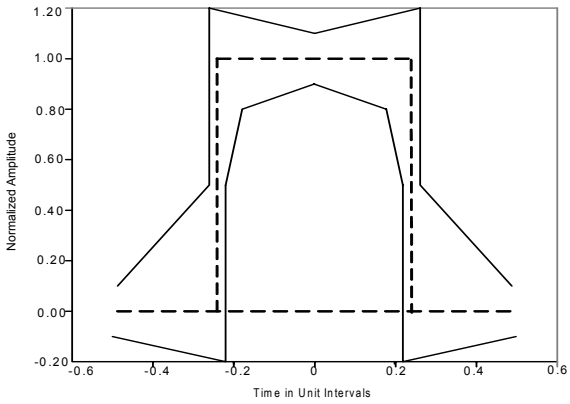
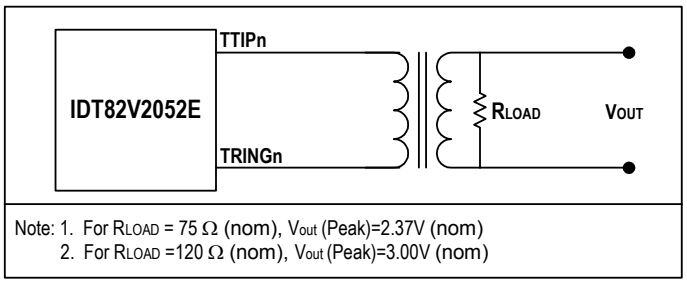


Figure-3 E1 Waveform Template Diagram



Note: 1. For R_{LOAD} = 75 Ω (nom), V_{out} (Peak)=2.37V (nom)
2. For R_{LOAD} =120 Ω (nom), V_{out} (Peak)=3.00V (nom)

Figure-4 E1 Pulse Template Test Circuit

3.2.3.2 User-Programmable Arbitrary Waveform

When the PULS[3:0] bits are set to '11xx', user-programmable arbitrary waveform generator mode can be used in the corresponding channel. This allows the transmitter performance to be tuned for a wide variety of line condition or special application.

Each pulse shape can extend up to 4 UIs (Unit Interval), addressed by UI[1:0] bits (**TCF3, 07H...**) and each UI is divided into 16 sub-phases, addressed by the SAMP[3:0] bits (**TCF3, 07H...**). The pulse amplitude of each phase is represented by a binary byte, within the range from +63 to -63, stored in WDAT[6:0] bits (**TCF4, 08H...**) in signed magnitude form. The most positive number +63 (D) represents the maximum positive amplitude of the transmit pulse while the most negative number -63 (D) represents the maximum negative amplitude of the transmit pulse. Therefore, up to 64 bytes are used. For each channel, a 64 bytes RAM is available.

There are two standard templates which are stored in an on-chip ROM. User can select one of them as reference and make some changes to get the desired waveform.

User can change the wave shape and the amplitude to get the desired pulse shape. In order to do this, firstly, users can choose a set of waveform value from the following two tables, which is the most similar to the desired pulse shape. Table-2 and Table-3 list the sample data and scaling data of each of the two templates. Then modify the corresponding sample data to get the desired transmit pulse shape.

Secondly, through the value of SCAL[5:0] bits increased or decreased by 1, the pulse amplitude can be scaled up or down at the percentage ratio against the standard pulse amplitude if needed. For different pulse shapes, the value of SCAL[5:0] bits and the scaling percentage ratio are different. The following two tables list these values.

Do the followings step by step, the desired waveform can be programmed, based on the selected waveform template:

(1).Select the UI by UI[1:0] bits (**TCF3, 07H...**)

(2).Specify the sample address in the selected UI by SAMP [3:0] bits (**TCF3, 07H...**)

(3).Write sample data to WDAT[6:0] bits (**TCF4, 08H...**). It contains the data to be stored in the RAM, addressed by the selected UI and the corresponding sample address.

(4).Set the RW bit (**TCF3, 07H...**) to '0' to implement writing data to RAM, or to '1' to implement read data from RAM

(5).Implement the Read from RAM/Write to RAM by setting the DONE bit (**TCF3, 07H...**)

Repeat the above steps until all the sample data are written to or read from the internal RAM.

(6).Write the scaling data to SCAL[5:0] bits (**TCF2, 06H...**) to scale the amplitude of the waveform based on the selected standard pulse amplitude

When more than one UI is used to compose the pulse template, the overlap of two consecutive pulses could make the pulse amplitude overflow (exceed the maximum limitation) if the pulse amplitude is not set properly. This overflow is captured by DAC_OV_IS bit (**INTS1, 19H...**), and, if enabled by the DAC_OV_IM bit (**INTM1, 14H...**), an interrupt will be generated.

The following tables give all the sample data based on the preset pulse templates in detail for reference. For preset pulse templates, scaling up/down against the pulse amplitude is not supported.

1. Table-2 Transmit Waveform Value for E1 75 Ω
2. Table-3 Transmit Waveform Value for E1 120 Ω

Table-2 Transmit Waveform Value For E1 75 Ohm

Sample	UI 1	UI 2	UI 3	UI 4
1	0000000	0000000	0000000	0000000
2	0000000	0000000	0000000	0000000
3	0000000	0000000	0000000	0000000
4	0001100	0000000	0000000	0000000
5	0110000	0000000	0000000	0000000
6	0110000	0000000	0000000	0000000
7	0110000	0000000	0000000	0000000
8	0110000	0000000	0000000	0000000
9	0110000	0000000	0000000	0000000
10	0110000	0000000	0000000	0000000
11	0110000	0000000	0000000	0000000
12	0110000	0000000	0000000	0000000
13	0000000	0000000	0000000	0000000
14	0000000	0000000	0000000	0000000
15	0000000	0000000	0000000	0000000
16	0000000	0000000	0000000	0000000

SCAL[5:0] = 100001 (default), One step change of this value of SCAL[5:0] results in 3% scaling up/down against the pulse amplitude.

Table-3 Transmit Waveform Value For E1 120 Ohm

Sample	UI 1	UI 2	UI 3	UI 4
1	0000000	0000000	0000000	0000000
2	0000000	0000000	0000000	0000000
3	0000000	0000000	0000000	0000000
4	0001111	0000000	0000000	0000000
5	0111100	0000000	0000000	0000000
6	0111100	0000000	0000000	0000000
7	0111100	0000000	0000000	0000000
8	0111100	0000000	0000000	0000000
9	0111100	0000000	0000000	0000000
10	0111100	0000000	0000000	0000000
11	0111100	0000000	0000000	0000000
12	0111100	0000000	0000000	0000000
13	0000000	0000000	0000000	0000000
14	0000000	0000000	0000000	0000000
15	0000000	0000000	0000000	0000000
16	0000000	0000000	0000000	0000000

SCAL[5:0] = 100001 (default), One step change of this value of SCAL[5:0] results in 3% scaling up/down against the pulse amplitude.

3.2.4 TRANSMIT PATH LINE INTERFACE

The transmit line interface consists of TTIPn and TRINGn pins. The impedance matching can be realized by the internal impedance matching circuit or the external impedance matching circuit. If T_TERM[2] is set to '0', the internal impedance matching circuit will be selected. In this case, the T_TERM[1:0] bits (**TERM, 02H...**) can be set to choose 75 Ω or 120 Ω internal impedance of TTIPn/TRINGn. If T_TERM[2] is set to '1', the internal impedance matching circuit will be disabled. In this case, the external impedance matching circuit will be used to realize the impedance matching.

Figure-6 shows the appropriate external components to connect with the cable for one channel. Table-4 is the list of the recommended impedance matching for transmitter.

In hardware control mode, TERMn pin can be used to select impedance matching for both receiver and transmitter on a per channel basis. If TERMn pin is low, internal impedance network will be used. If TERMn pin is high, external impedance network will be used. When internal impedance network is used, PULSn pins should be set to select the specific internal impedance in the corresponding channel. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.

The TTIPn/TRINGn can also be turned into high impedance globally by pulling THZ pin to high or individually by setting the THZ bit (**TCF1, 05H...**) to '1'. In this state, the internal transmit circuits are still active.

In hardware control mode, TTIPn/TRINGn pins can be turned into high impedance globally by pulling THZ pin to high. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.

Besides, in the following cases, TTIPn/TRINGn will also become high impedance:

- Loss of MCLK;
- Loss of TCLKn (exceptions: Remote Loopback; Transmit internal pattern by MCLK);
- Transmit path power down;
- After software reset; pin reset and power on.

Table-4 Impedance Matching for Transmitter

Cable Configuration	Internal Termination			External Termination		
	T_TERM[2:0]	PULS[3:0]	R_T	T_TERM[2:0]	PULS[3:0]	R_T
E1 / 75 Ω	000	0000	0 Ω	1XX	0001	9.4 Ω
E1 / 120 Ω	001	0001			0001	

Note: The precision of the resistors should be better than ± 1%

3.2.5 TRANSMIT PATH POWER DOWN

The transmit path can be powered down individually by setting the T_OFF bit (**TCF0, 04H...**) to '1'. In this case, the TTIPn/TRINGn pins are turned into high impedance.

In hardware control mode, the transmit path can be powered down by setting PATTn[1:0] pins to '11' on a per channel basis. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.

3.3 RECEIVE PATH

The receive path consists of Receive Internal Termination, Monitor Gain, Amplitude/Wave Shape Detector, Digital Tuning Controller, Adaptive Equalizer, Data Slicer, CDR (Clock & Data Recovery), Optional Jitter Attenuator, Decoder and LOS/AIS Detector. Refer to Figure-5.

3.3.1 RECEIVE INTERNAL TERMINATION

The impedance matching can be realized by the internal impedance matching circuit or the external impedance matching circuit. If R_TERM[2] is set to '0', the internal impedance matching circuit will be selected. In this case, the R_TERM[1:0] bits (**TERM, 02H...**) can be set to choose 75 Ω or 120 Ω internal impedance of RTIPn/RRINGn. If R_TERM[2] is set to '1', the internal impedance matching circuit will be disabled. In this case, the external impedance matching circuit will be used to realize the impedance matching.

Figure-6 shows the appropriate external components to connect with the cable for one channel. Table-5 is the list of the recommended impedance matching for receiver.

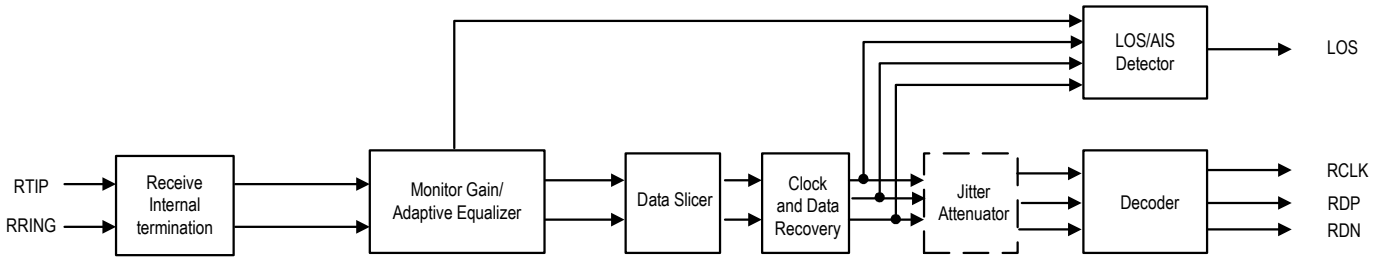
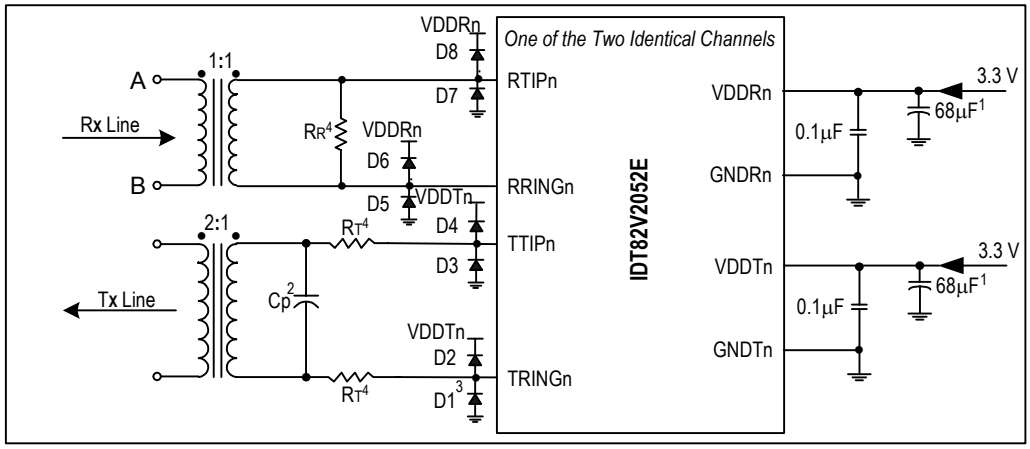


Figure-5 Receive Path Function Block Diagram

Table-5 Impedance Matching for Receiver

Cable Configuration	Internal Termination		External Termination	
	R_TERM[2:0]	R_R	R_TERM[2:0]	R_R
E1 / 75 Ω	000	120 Ω	1XX	75 Ω
E1 / 120 Ω	001			120 Ω



Note:
1. Common decoupling capacitor. One per chip
2. Cp 0-560 (pF)
3. D1 - D8, Motorola - MBR0540T1; International Rectifier - 11DQ04 or 10BQ060
4. R_T/ R_R: refer to Table-4 and Table-5 respecivley for R_T and R_R values

Figure-6 Transmit/Receive Line Circuit

In hardware control mode, TERMn, PULSn pins can be used to select impedance matching for both receiver and transmitter on a per channel basis. If TERMn pin is low, internal impedance network will be used. If TERMn pin is high, external impedance network will be used. When internal impedance network is used, PULSn pins should be set to select specific internal impedance for the corresponding channel. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.

3.3.2 LINE MONITOR

The non-intrusive monitoring on channels located in other chips can be performed by tapping the monitored channel through a high impedance bridging circuit. Refer to Figure-7 and Figure-8.

After a high resistance bridging circuit, the signal arriving at the RTIPn/ RRINGn is dramatically attenuated. To compensate this attenuation, the Monitor Gain can be used to boost the signal by 22 dB, 26 dB and 32 dB, selected by MG[1:0] bits (**RCF2, 0BH...**). For normal operation, the Monitor Gain should be set to 0 dB.

In hardware control mode, MONTn pin can be used to set the Monitor Gain on a per channel basis. When MONTn pin is low, the Monitor Gain for the specific channel is 0 dB. When MONTn pin is high, the Monitor Gain for the specific channel is 26 dB. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.

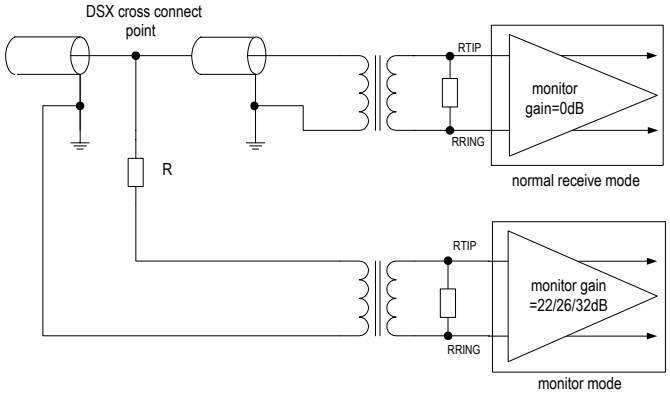


Figure-7 Monitoring Receive Line in Another Chip

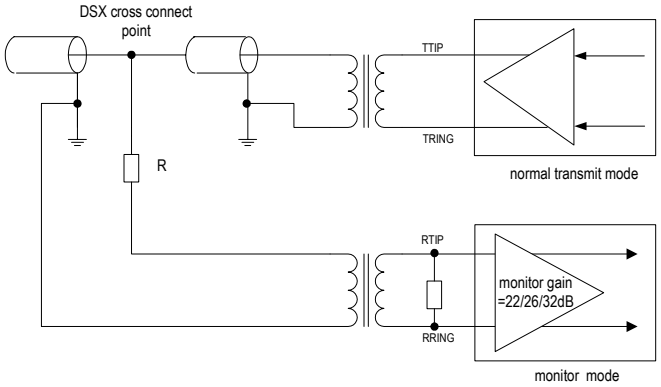


Figure-8 Monitor Transmit Line in Another Chip

3.3.3 ADAPTIVE EQUALIZER

The Adaptive Equalizer can be enabled to increase the receive sensitivity and to allow programming of the LOS level up to -24 dB. See section 3.5 LOS AND AIS DETECTION. It can be enabled or disabled by setting EQ_ON bit to '1' or '0' (**RCF1, 0AH...**).

3.3.4 RECEIVE SENSITIVITY

In Host mode, the Receive Sensitivity is -10 dB. With the Adaptive Equalizer enabled, the receive sensitivity will be -20 dB.

In Hardware mode, the Adaptive Equalizer can not be enabled and the receive sensitivity is fixed at -10 dB. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.

3.3.5 DATA SLICER

The Data Slicer is used to generate a standard amplitude mark or a space according to the amplitude of the input signals. The threshold can be 40%, 50%, 60% or 70%, as selected by the SLICE[1:0] bits (**RCF2, 0BH...**). The output of the Data Slicer is forwarded to the CDR (Clock & Data Recovery) unit or to the RDPn/RDNn pins directly if the CDR is disabled.

3.3.6 CDR (Clock & Data Recovery)

The CDR is used to recover the clock and data from the received signal. The recovered clock tracks the jitter in the data output from the Data Slicer and keeps the phase relationship between data and clock during the absence of the incoming pulse. The CDR can also be by-passed in the Dual Rail mode. When CDR is by-passed, the data from the Data Slicer is output to the RDPn/RDNn pins directly.

3.3.7 DECODER

The R_MD[1:0] bits (**RCF0, 09H...**) are used to select the AMI decoder or HDB3 decoder.

When the chip is configured by hardware, the operation mode of receive and transmit path can be selected by setting RXTXM[1:0] pins on a global basis. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.

3.3.8 RECEIVE PATH SYSTEM INTERFACE

The receive path system interface consists of RCLKn pin, RDn/RDPn pin and RDNn pin. The RCLKn outputs a recovered 2.048 MHz clock. The received data is updated on the RDn/RDPn and RDNn pins on the active edge of RCLKn. The active edge of RCLKn can be selected by the RCLK_SEL bit (**RCF0, 09H...**). And the active level of the data on RDn/RDPn and RDNn can be selected by the RD_INV bit (**RCF0, 09H...**).

In hardware control mode, only the active edge of RCLKn can be selected. If RCLKE is set to high, the falling edge will be chosen as the active edge of RCLKn. If RCLKE is set to low, the rising edge will be chosen as the active edge of RCLKn. The active level of the data on RDn/RDPn and RDNn is the same as that in software control mode.

The received data can be output to the system side in two different ways: Single Rail or Dual Rail, as selected by R_MD bit [1] (**RCF0, 09H...**). In Single Rail mode, only RDn pin is used to output data and the RDNn/CVn pin is used to report the received errors. In Dual Rail Mode, both RDPn pin and RDNn pin are used for outputting data.

In the receive Dual Rail mode, the CDR unit can be by-passed by setting R_MD[1:0] to '11' (binary). In this situation, the output data from the Data Slicer will be output to the RDPn/RDNn pins directly, and the RCLKn outputs the exclusive OR (XOR) of the RDPn and RDNn. This is called receiver slicer mode. In this case, the transmit path is still operating in Dual Rail mode.

3.3.9 RECEIVE PATH POWER DOWN

The receive path can be powered down individually by setting R_OFF bit (**RCF0, 09H...**) to '1'. In this case, the RCLKn, RDn/RDPn, RDNn and LOSn will be logic low.

In hardware control mode, receiver power down can be selected by pulling RPDn pin to high on a per channel basis. Refer to 5 HARDWARE CONTROL PIN SUMMARY for more details.

3.3.10 G.772 NON-INTRUSIVE MONITORING

In applications using only one channel, channel 1 can be configured to monitor the data received or transmitted in channel 2. The MONT[1:0] bits (**GCF, 20H**) determine which direction (transmit/receive) will be monitored. The monitoring is non-intrusive per ITU-T G.772. Figure-9 illustrates the concept.

The monitored line signal (transmit or receive) goes through Channel 1's Clock and Data Recovery. The signal can be observed digitally at the RCLK1, RD1/RDP1 and RDN1. If Channel 1 is configured to Remote Loopback while in the Monitoring mode, the monitored data will be output on TTIP1/TRING1.

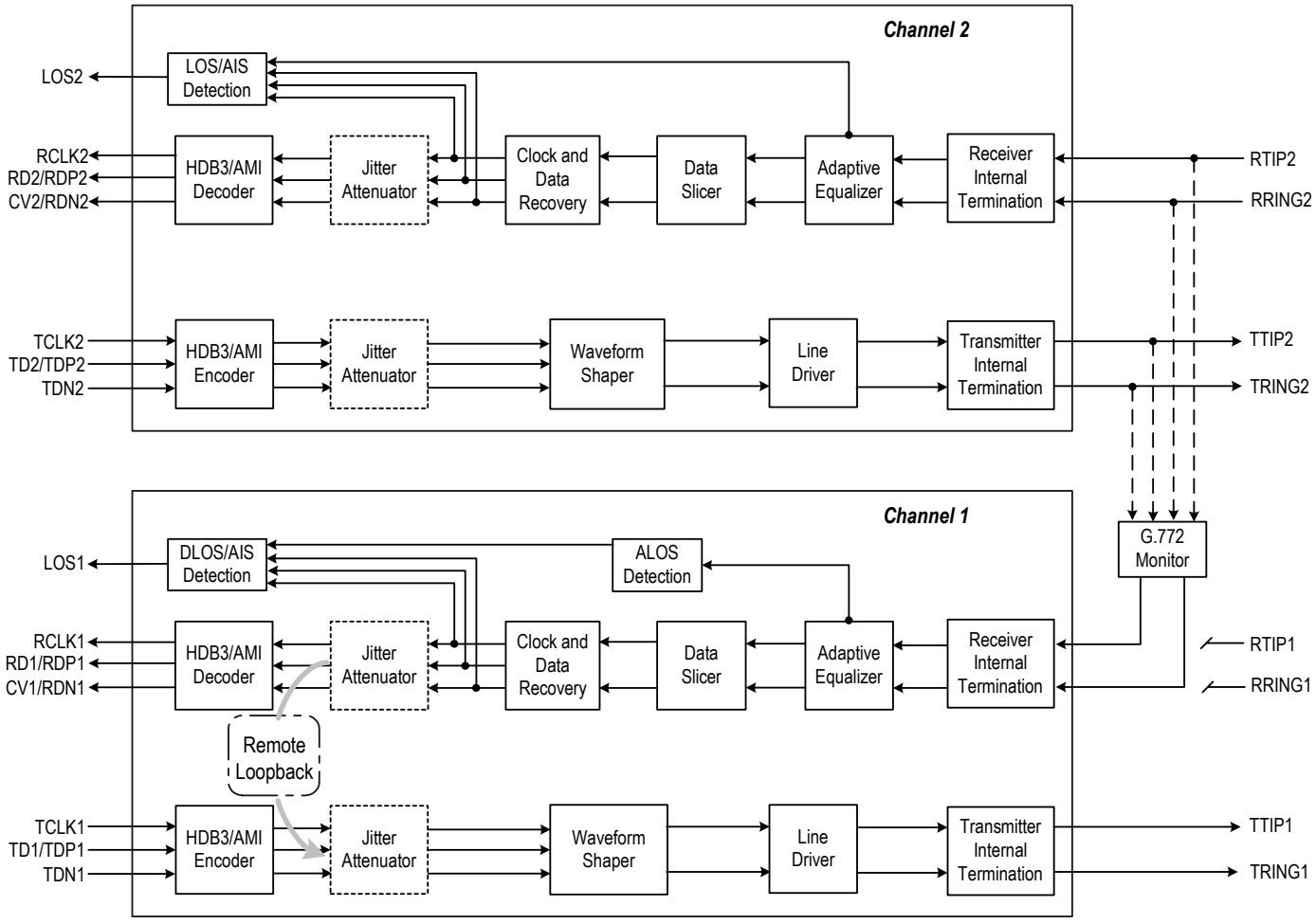


Figure-9 G.772 Monitoring Diagram

3.4 JITTER ATTENUATOR

There is one Jitter Attenuator in each channel of the LIU. The Jitter Attenuator can be deployed in the transmit path or the receive path, and can also be disabled. This is selected by the JACF[1:0] bits (**JACF, 03H...**).

In hardware control mode, Jitter Attenuator position, bandwidth and the depth of FIFO can be selected by JA[1:0] pins on a global basis. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.

3.4.1 JITTER ATTENUATION FUNCTION DESCRIPTION

The Jitter Attenuator is composed of a FIFO and a DPLL, as shown in Figure-10. The FIFO is used as a pool to buffer the jittered input data, then the data is clocked out of the FIFO by a de-jittered clock. The depth of the FIFO can be 32 bits, 64 bits or 128 bits, as selected by the JADP[1:0] bits (**JACF, 03H...**). In hardware control mode, the depth of FIFO can be selected by JA[1:0] pins on a global basis. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details. Consequently, the constant delay of the Jitter Attenuator will be 16 bits, 32 bits or 64 bits. Deeper FIFO can tolerate larger jitter, but at the cost of increasing data latency time.

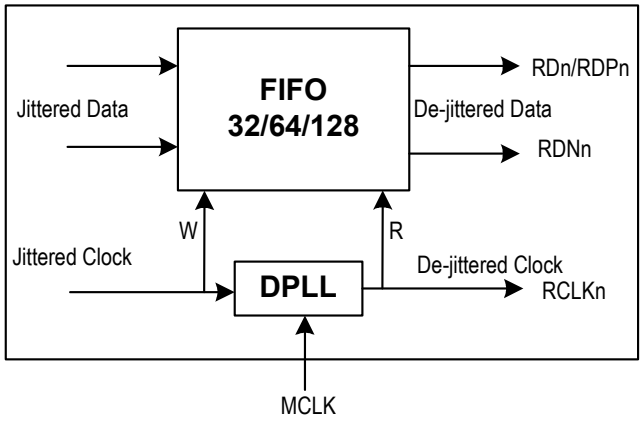


Figure-10 Jitter Attenuator

The Corner Frequency of the DPLL can be 0.9 Hz or 6.8 Hz, as selected by the JABW bit (**JACF, 03H...**). The lower the Corner Frequency is, the longer time is needed to achieve synchronization.

When the incoming data moves faster than the outgoing data, the FIFO will overflow. This overflow is captured by the JAOV_IS bit (**INTS1, 19H...**). If the incoming data moves slower than the outgoing data, the FIFO will underflow. This underflow is captured by the JAUD_IS bit (**INTS1, 19H...**). For some applications that are sensitive to data corruption, the JA limit mode can be enabled by setting JA_LIMIT bit (**JACF, 03H...**) to '1'. In the JA limit mode, the speed of the outgoing data will be adjusted automatically when the FIFO is close to its full or emptiness. The criteria of starting speed adjustment are shown in Table-6. The JA limit mode can reduce the possibility of FIFO overflow and underflow, but the quality of jitter attenuation is deteriorated.

Table-6 Criteria of Starting Speed Adjustment

FIFO Depth	Criteria for Adjusting Data Outgoing Speed
32 Bits	2 bits close to its full or emptiness
	3 bits close to its full or emptiness
	4 bits close to its full or emptiness

3.4.2 JITTER ATTENUATOR PERFORMANCE

The performance of the Jitter Attenuator in the IDT82V2052E meets the ITU-T I.431, G.703, G.736-739, G.823, G.824, ETSI 300011, ETSI TBR12/13 specifications. Details of the Jitter Attenuator performance is shown in Table-52 Jitter Tolerance and Table-53 Jitter Attenuator Characteristics.

3.5 LOS AND AIS DETECTION

3.5.1 LOS DETECTION

The Loss of Signal Detector monitors the amplitude of the incoming signal level and pulse density of the received signal on RTIPn and RRINGn.

- **LOS declare (LOS=1)**

A LOS is detected when the incoming signal has “no transitions”, i.e., when the signal level is less than Q dB below nominal for N consecutive pulse intervals. Here N is defined by LAC bit (**MAINT0, 0CH...**). LOS will be declared by pulling LOSn pin to high (LOS=1) and LOS interrupt will be generated if it is not masked.

- **LOS clear (LOS=0)**

The LOS is cleared when the incoming signal has “transitions”, i.e., when the signal level is greater than P dB below nominal and has an average pulse density of at least 12.5% for M consecutive pulse intervals, starting with the receipt of a pulse. Here M is defined by LAC bit (**MAINT0, 0CH...**). LOS status is cleared by pulling LOSn pin to low.

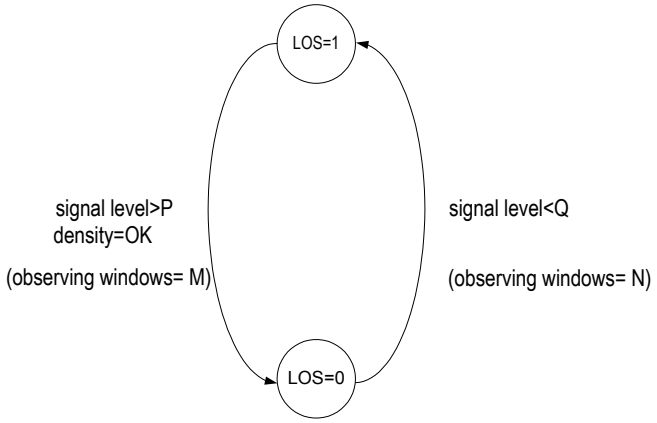


Figure-11 LOS Declare and Clear

- **LOS detect level threshold**

With the Adaptive Equalizer off, the amplitude threshold Q is fixed on 800 mVpp, while P=Q+200 mVpp (200 mVpp is the LOS level detect hysteresis).

With the Adaptive Equalizer on, the value of Q can be selected by LOS[4:0] bit (**RCF1, 0AH...**), while P=Q+4 dB (4 dB is the LOS level detect hysteresis). Refer to Table 27, “RCF1: Receiver Configuration Register 1,” on page 42 for LOS[4:0] bit values available.

When the chip is configured by hardware, the Adaptive Equalizer can not be enabled and Programmable LOS levels are not available (pin 58 & pin 60 have to be set to ‘0’).

- **Criteria for declare and clear of a LOS detect**

The detection supports G.775 and ETSI 300233/I.431. The criteria can be selected by LAC bit (**MAINT0, 0CH...**).

Table-7 and Table-8 summarize LOS declare and clear criteria for both with and without the Adaptive Equalizer enabled.

- **All Ones output during LOS**

On the system side, the RDPn/RDNn will reflect the input pulse “transition” at the RTIPn/RRINGn side and output recovered clock (but the quality of the output clock can not be guaranteed when the input level is lower than the maximum receive sensitivity) when AISE bit (**MAINT0, 0CH...**) is 0; or output All Ones as AIS when AISE bit (**MAINT0, 0CH...**) is 1. In this case RCLKn output is replaced by MCLK.

On the line side, the TTIPn/TRINGn will output All Ones as AIS when ATAO bit (**MAINT0, 0CH...**) is 1. The All Ones pattern uses MCLK as the reference clock.

LOS indicator is always active for all kinds of loopback modes.

Table-7 LOS Declare and Clear Criteria, Adaptive Equalizer Disabled

Control bit (LAC)	LOS declare threshold	LOS clear threshold
0 = G.775	Level < 800 mVpp; N=32 bits	Level > 1 Vpp; M=32 bits; 12.5% mark density; <16 consecutive zeroes
1 = I.431/ETSI	Level < 800 mVpp; N=2048 bits	Level > 1 Vpp; M=32 bits; 12.5% mark density; <16 consecutive zeroes

Table-8 LOS Declare and Clear Criteria, Adaptive Equalizer Enabled

Control bit				LOS declare threshold	LOS clear threshold	Note
LAC		LOS[4:0]	Q (dB)			
0	-	00000 … 00010	-4 … -8	Level < Q N=32 bits	Level > Q+ 4dB M=32 bits 12.5% mark density <16 consecutive zeroes	G.775 Level detect range is -9 to -35 dB.
	G.775	00011 … 01010 01011 - 11111	-10 … -24 Reserved			
1	-	00000	-4	Level < Q N=2048 bits	Level > Q+ 4dB M=32 bits 12.5% mark density <16 consecutive zeroes	I.431 Level detect range is -6 to -20 dB.
	I.431/ETSI	00001 … 01010 01011 - 11111	-6 … -24 Reserved			

3.5.2 AIS DETECTION

The Alarm Indication Signal can be detected by the IDT82V2052E when the Clock & Data Recovery unit is enabled. The status of AIS detection is reflected in the AIS_S bit (**STAT0, 16H...**). The criteria for declaring/clearing AIS detection comply with the ITU G.775 or the ETSI 300233, as selected by the LAC bit (**MAINT0, 0CH...**). Table-9 summarizes different criteria for AIS detection Declaring/Clearing.

Table-9 AIS Condition

	ITU G.775 (LAC bit is set to '0' by default)	ETSI 300233 (LAC bit is set to '1')
AIS Detected	Less than 3 zeros contained in each of two consecutive 512-bit streams are received	Less than 3 zeros contained in a 512-bit stream are received
AIS Cleared	3 or more zeros contained in each of two consecutive 512-bit streams are received	3 or more zeros contained in a 512-bit stream are received

3.6 TRANSMIT AND DETECT INTERNAL PATTERNS

The internal patterns (All Ones, All Zeros and PRBS pattern) will be generated and detected by IDT82V2052E. TCLKn is used as the reference clock by default. MCLK can also be used as the reference clock by setting the PATT_CLK bit (**MAINT0, 0CH...**) to '1'.

If the PATT_CLK bit (**MAINT0, 0CH...**) is set to '0' and the PATT[1:0] bits (**MAINT0, 0CH...**) are set to '00', the transmit path will operate in normal mode.

When the chip is configured by hardware, the transmit path will operate in normal mode by setting PATTn[1:0] pins to '00' on a per channel basis. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.

3.6.1 TRANSMIT ALL ONES

In transmit direction, the All Ones data can be inserted into the data stream when the PATT[1:0] bits (**MAINT0, 0CH...**) are set to '01'. The transmit data stream is output from TTIPn/TRINGn. In this case, either TCLKn or MCLK can be used as the transmit clock, as selected by the PATT_CLK bit (**MAINT0, 0CH...**).

In hardware control mode, the All Ones data can be inserted into the data stream in transmit direction by setting PATTn[1:0] pins to '01' on a per channel basis. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.

3.6.2 TRANSMIT ALL ZEROS

If the PATT_CLK bit (**MAINT0, 0CH...**) is set to '1', the All Zeros will be inserted into the transmit data stream when the PATT[1:0] bits (**MAINT0, 0CH...**) are set to '00'.

3.6.3 PRBS GENERATION AND DETECTION

A PRBS will be generated in the transmit direction and detected in the receive direction by IDT82V2052E. The PRBS is 2^{15}-1, with maximum zero restrictions according to ITU-T O.151.

When the PATT[1:0] bits (**MAINT0, 0CH...**) are set to '10', the PRBS pattern will be inserted into the transmit data stream with the MSB first. The PRBS pattern will be transmitted directly or invertedly.

In hardware control mode, the PRBS data will be generated in the transmit direction and inserted into the transmit data stream by setting PATTn[1:0] pins to '10' on a per channel basis. Refer to 5 HARDWARE CONTROL PIN SUMMARY for details.

The PRBS in the received data stream will be monitored. If the PRBS has reached synchronization status, the PRBS_S bit (**STAT0, 16H...**) will be set to '1', even in the presence of a logic error rate less than or equal to 10^{-1}. The criteria for setting/clearing the PRBS_S bit are shown in Table-10.

Table-10 Criteria for Setting/Clearing the PRBS_S Bit

PRBS Detection	6 or less than 6 bit errors detected in a 64 bits hopping window.
PRBS Missing	More than 6 bit errors detected in a 64 bits hopping window.

PRBS data can be inverted through setting the PRBS_INV bit (**MAINT0, 0CH...**).

Any change of PRBS_S bit will be captured by PRBS_IS bit (**INTS0, 18H...**). The PRBS_IES bit (**INTES, 15H...**) can be used to determine whether the '0' to '1' change of PRBS_S bit will be captured by the PRBS_IS bit or any changes of PRBS_S bit will be captured by the PRBS_IS bit. When the PRBS_IS bit is '1', an interrupt will be generated if the PRBS_IM bit (**INTM0, 13H...**) is set to '1'.

The received PRBS logic errors can be counted in a 16-bit counter if the ERR_SEL [1:0] bits (**MAINT6, 12H...**) are set to '00'. Refer to 3.8 ERROR DETECTION/COUNTING AND INSERTION for the operation of the error counter.

3.7 LOOPBACK

To facilitate testing and diagnosis, the IDT82V2052E provides three different loopback configurations: Analog Loopback, Digital Loopback and Remote Loopback.

3.7.1 ANALOG LOOPBACK

When the ALP bit (**MAINT1, 0DH...**) is set to '1', the corresponding channel is configured in Analog Loopback mode. In this mode, the transmit signals are looped back to the Receiver Internal Termination in the receive path then output from RCLKn, RDn, RDPn/RDNn. The all-ones pattern can be generated during analog loopback. At the same time, the transmit signals are still output to TTIPn/TRINGn in transmit direction. Figure-12 shows the process.

In hardware control mode, Analog Loopback can be selected by setting LPn[1:0] pins to '01' on a per channel basis.

3.7.2 DIGITAL LOOPBACK

When the DLP bit (**MAINT1, 0DH...**) is set to '1', the corresponding channel is configured in Digital Loopback mode. In this mode, the transmit signals are looped back to the jitter attenuator (if enabled) and decoder in receive path, then output from RCLKn, RDn, RDPn/RDNn. At the same time, the transmit signals are still output to TTIPn/TRINGn in transmit direction. Figure-13 shows the process.

Both Analog Loopback mode and Digital Loopback mode allow the sending of the internal patterns (All Ones, All Zeros, PRBS, etc.) which will overwrite the transmit signals. In this case, either TCLKn or MCLK can be used as the reference clock for internal patterns transmission.

In hardware control mode, Digital Loopback can be selected by setting LPn[1:0] pins to '10' on a per channel basis.

3.7.3 REMOTE LOOPBACK

When the RLP bit (**MAINT1, 0DH...**) is set to '1', the corresponding channel is configured in Remote Loopback mode. In this mode, the recovered clock and data output from Clock and Data Recovery on the receive path is looped back to the jitter attenuator (if enabled) and Waveform Shaper in transmit path. Figure-14 shows the process.

In hardware control mode, Remote Loopback can be selected by setting LPn[1:0] pins to '11' on a per channel basis.

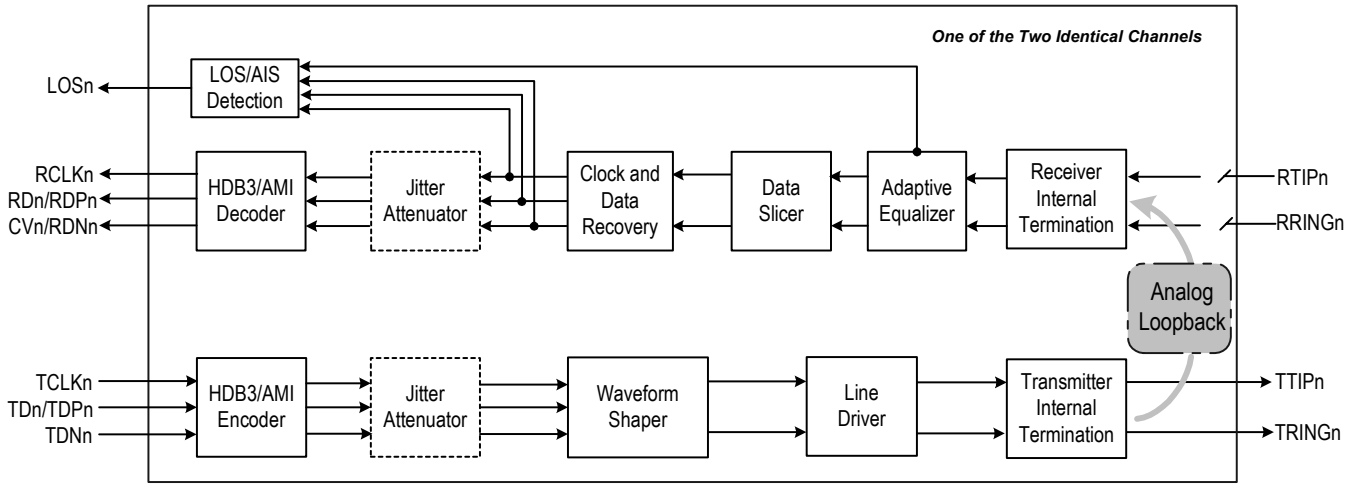


Figure-12 Analog Loopback

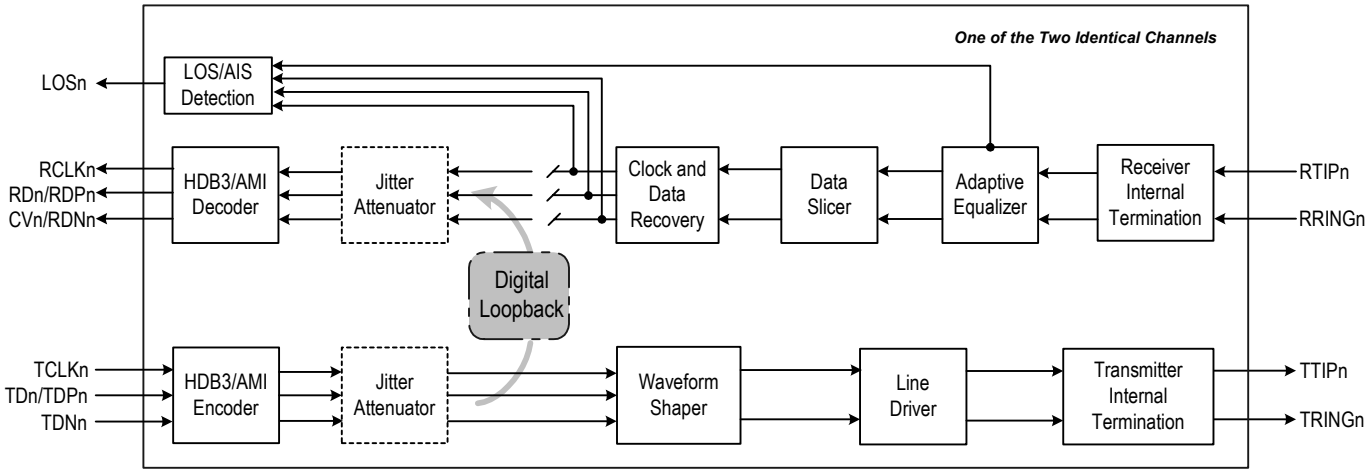


Figure-13 Digital Loopback

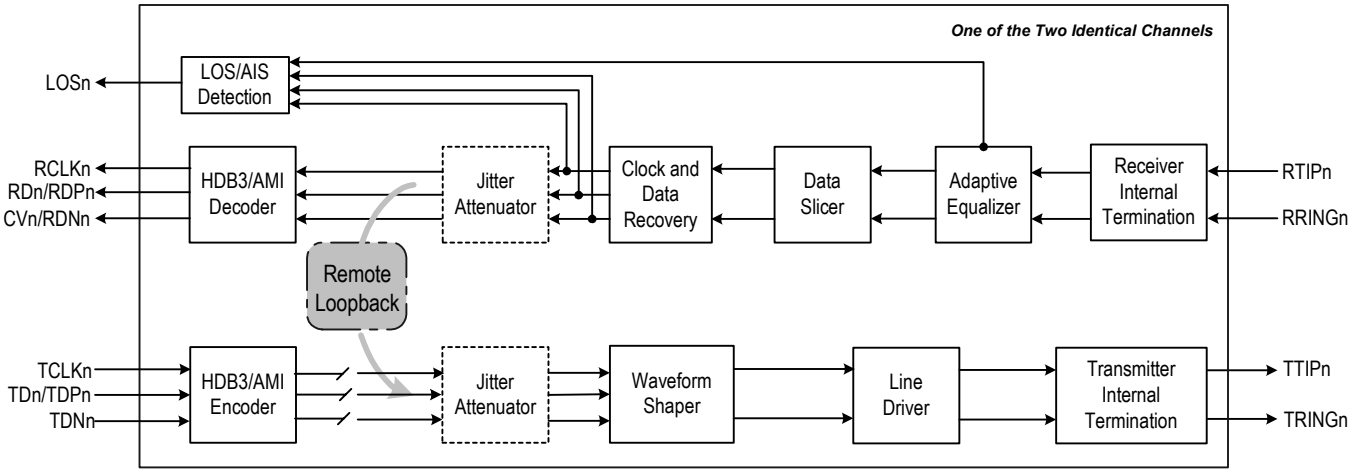


Figure-14 Remote Loopback

3.8 ERROR DETECTION/COUNTING AND INSERTION

3.8.1 DEFINITION OF LINE CODING ERROR

The following line encoding errors can be detected and counted by the IDT82V2052E:

- Received Bipolar Violation (BPV) Error: In AMI coding, when two consecutive pulses of the same polarity are received, a BPV error is declared.
- HDB3 Code Violation (CV) Error: In HDB3 coding, a CV error is declared when two consecutive BPV errors are detected, and the pulses that have the same polarity as the previous pulse are not the HDB3 zero substitution pulses.
- Excess Zero (EXZ) Error: There are two standards defining the EXZ errors: ANSI and FCC. The EXZ_DEF bit (**MAINT6, 12H...**) chooses which standard will be adopted by the corresponding channel to judge the EXZ error. Table-11 shows definition of EXZ. In hardware control mode, only ANSI standard is adopted.

Table-11 EXZ Definition

	EXZ Definition	
	ANSI	**FCC**
AMI	More than 15 consecutive zeros are detected	More than 80 consecutive zeros are detected
HDB3	More than 3 consecutive zeros are detected	More than 3 consecutive zeros are detected

3.8.2 ERROR DETECTION AND COUNTING

Which type of the receiving errors (Received CV/BPV errors, excess zero errors and PRBS logic errors) will be counted is determined by ERR_SEL[1:0] bits (**MAINT6, 12H...**). Only one type of receiving error can be counted at a time except that when the ERR_SEL[1:0] bits are set to '11', both CV/BPV and EXZ errors will be detected and counted.

The selected type of receiving errors is counted in an internal 16-bit Error Counter. Once an error is detected, an error interrupt which is indicated by corresponding bit in (**INTS1, 19H...**) will be generated if it is not masked. This Error Counter can be operated in two modes: Auto Report Mode and Manual Report Mode, as selected by the CNT_MD bit (**MAINT6, 12H...**). In Single Rail mode, once BPV or CV errors are detected, the CVn pin will be driven to high for one RCLK period.

• Auto Report Mode

In Auto Report Mode, the internal counter starts to count the received errors when the CNT_MD bit (**MAINT6, 12H...**) is set to '1'. A one-second timer is used to set the counting period. The received errors are counted within one second. If the one-second timer expires, the value in the internal counter will be transferred to (**CNT0, 1AH...**) and (**CNT1, 1BH...**), then the internal counter will be reset and start to count received errors for the next second. The errors occurred during the transfer will be accumulated to the next round. The expiration of the one-second timer will set TMOV_IS bit (**INTS1, 19H...**) to '1', and will generate an interrupt if the TIMER_IM bit (**INTM1, 14H...**) is set to '0'. The TMOV_IS bit (**INTS1, 19H...**) will be cleared after the interrupt register is read. The content in the (**CNT0, 1AH...**) and (**CNT1, 1BH...**) should be read within the next second. If the counter overflows, a counter overflow interrupt which is indicated by CNT_OV_IS bit (**INTS1, 19H...**) will be generated if it is not masked by CNT_IM bit (**INTM1, 14H...**).

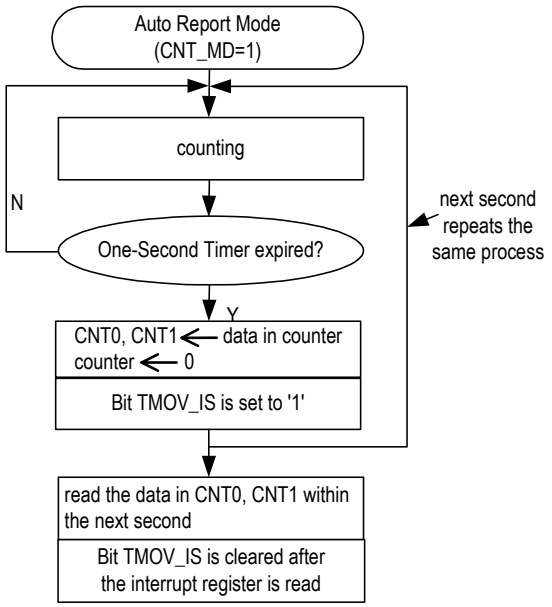


Figure-15 Auto Report Mode

• Manual Report Mode

In Manual Report Mode, the internal Error Counter starts to count the received errors when the CNT_MD bit **(MAINT6, 12H...)** is set to '0'. When there is a '0' to '1' transition on the CNT_TRF bit **(MAINT6, 12H...)**, the data in the counter will be transferred to **(CNT0, 1AH...)** and **(CNT1, 1BH...)**, then the counter will be reset. The errors occurred during the transfer will be accumulated to the next round. If the counter overflows, a counter overflow interrupt indicated by CNT_OV_IS bit **(INTS1, 19H...)** will be generated if it is not masked by CNT_IM bit **(INTM1, 14H...)**.

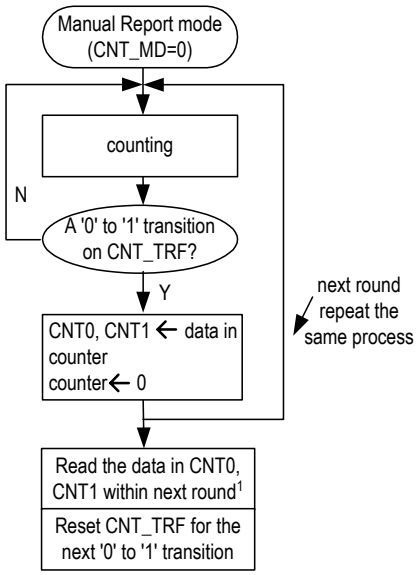


Figure-16 Manual Report Mode

Note: It is recommended that users should do the followings within next round of error counting: Read the data in CNT0 and CNT1; Reset CNT_TRF bit for the next '0' to '1' transition on this bit.

3.8.3 BIPOLAR VIOLATION AND PRBS ERROR INSERTION

Only when three consecutive '1's are detected in the transmit data stream, will a '0' to '1' transition on the BPV_INS bit (**MAINT6, 12H...**) generate a bipolar violation pulse, and the polarity of the second '1' in the series will be inverted.

A '0' to '1' transition on the EER_INS bit (**MAINT6, 12H...**) will generate a logic error during the PRBS transmission.

3.9 LINE DRIVER FAILURE MONITORING

The transmit driver failure monitor can be enabled or disabled by setting DFM_OFF bit (**TCF1, 05H...**). If the transmit driver failure monitor is enabled, the transmit driver failure will be captured by DF_S bit (**STAT0, 16H...**). The transition of the DF_S bit is reflected by DF_IS bit (**INTS0, 18H...**), and, if enabled by DF_IM bit (**INTM0, 13H...**), will generate an interrupt. When there is a short circuit on the TTIPn/TRINGn port, the output current will be limited to 100 mA (typical), and an interrupt will be generated.

In hardware control mode, the transmit driver failure monitor is always enabled.

3.10 MCLK AND TCLK

3.10.1 MASTER CLOCK (MCLK)

MCLK is an independent, free-running reference clock. MCLK is 2.048 MHz. This reference clock is used to generate several internal reference signals:

- Timing reference for the integrated clock recovery unit.
- Timing reference for the integrated digital jitter attenuator.
- Timing reference for microcontroller interface.
- Generation of RCLK signal during a loss of signal condition if AIS is enabled.
- Reference clock during Transmit All Ones (TAOS), all zeros and PRBS if it is selected as the reference clock. For ATAO and AIS, MCLK is always used as the reference clock.
- Reference clock during Transmit All Ones (TAO) condition or sending PRBS in hardware control mode.

Figure-17 shows the chip operation status in different conditions of MCLK and TCLKn. The missing of MCLK will set all the TTIPn/TRINGn to high impedance state.

3.10.2 TRANSMIT CLOCK (TCLK)

TCLKn is used to sample the transmit data on TDn/TDPn, TDNn. The active edge of TCLKn can be selected by the TCLK_SEL bit (**TCF0, 04H...**). During Transmit All Ones or PRBS pattern, either TCLKn or MCLK can be used as the reference clock. This is selected by the PATT_CLK bit (**MAINT0, 0CH...**).

But for Automatic Transmit All Ones and AIS, only MCLK is used as the reference clock and the PATT_CLK bit is ignored. In Automatic Transmit All Ones condition, the ATAO bit (**MAINT0, 0CH**) is set to '1'. In AIS condition, the AISE bit (**MAINT0, 0CH**) is set to '1'.

If TCLKn has been missing for more than 70 MCLK cycles, TCLK_LOS bit (**STAT0, 16H...**) will be set, and the corresponding TTIPn/TRINGn will become high impedance if this channel is not used for remote loopback or is not using MCLK to transmit internal patterns (TAOS, All Zeros and PRBS). When TCLK is detected again, TCLK_LOS bit (**STAT0, 16H...**) will be cleared. The reference frequency to detect a TCLK loss is derived from MCLK.

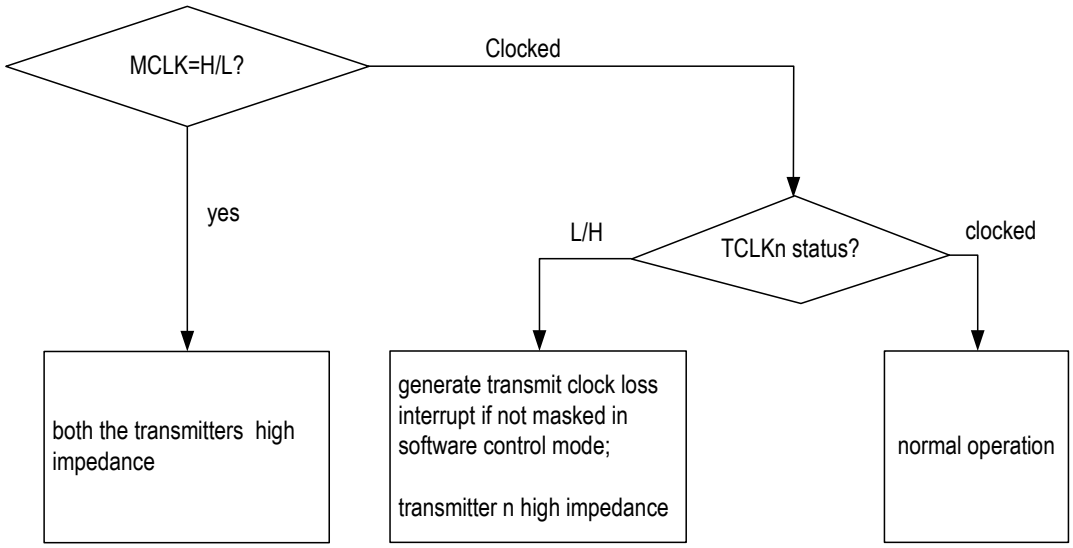


Figure-17 TCLK Operation Flowchart

3.11 MICROCONTROLLER INTERFACES

The microcontroller interface provides access to read and write the registers in the device. The chip supports serial microcontroller interface and two kinds of parallel microcontroller interface: Motorola non-Multiplexed mode and Intel non-Multiplexed mode. Different microcontroller interfaces can be selected by setting MODE[1:0] pins to different values. Refer to MODE1 and MODE0 in pin description and 8 MICROCONTROLLER INTERFACE TIMING CHARACTERISTICS for details

3.11.1 PARALLEL MICROCONTROLLER INTERFACE

The interface is compatible with Motorola or Intel microcontroller. When MODE[1:0] pins are set to '10', Parallel-non-Multiplexed-Motorola interface is selected. When MODE[1:0] pins are set to '11', Parallel-non-Multiplexed-Intel Interface is selected. Refer to 8 MICROCONTROLLER INTERFACE TIMING CHARACTERISTICS for details.

3.11.2 SERIAL MICROCONTROLLER INTERFACE

When MODE[1:0] pins are set to '01', Serial Interface is selected. In this mode, the registers are programmed through a 16-bit word which contains an 8-bit address/command byte (6 address bits A0~A5 and bit R/$\overline{W}$) and an 8-bit data byte (D0~D7). When bit R/$\overline{W}$ is '1', data is read out from pin SDO. When bit R/$\overline{W}$ is '0', data is written into SDI pin. Refer to Figure-18.

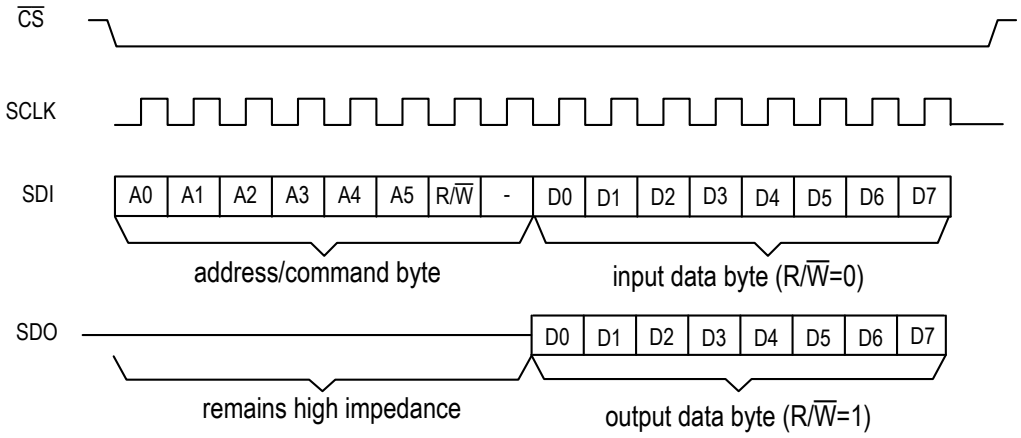


Figure-18 Serial Microcontroller Interface Function Timing

3.12 INTERRUPT HANDLING

All kinds of interrupt of the IDT82V2052E are indicated by the $\overline{INT}$ pin. When the INT_PIN[0] bit (**GCF, 20H**) is '0', the $\overline{INT}$ pin is open drain active low, with a 10 KΩ external pull-up resistor. When the INT_PIN[1:0] bits (**GCF, 20H**) are '01', the $\overline{INT}$ pin is push-pull active low; when the INT_PIN[1:0] bits are '10', the $\overline{INT}$ pin is push-pull active high.

All the interrupt can be disabled by the INTM_GLB bit (**GCF, 20H**). When the INTM_GLB bit (**GCF, 20H**) is set to '0', an active level on the $\overline{INT}$ pin represents an interrupt of the IDT82V2052E. The INT_CH[1:0] (**GCF, 20H**) should be read to identify which channel(s) generate the interrupt.

The interrupt event is captured by the corresponding bit in the Interrupt Status Register **(INTS0, 18H...)** or **(INTS1, 19H...)**. Every kind of interrupt can be enabled/disabled individually by the corresponding bit in the register **(INTM0, 13H...)** or **(INTM1, 14H...)**. Some event is reflected by the corresponding bit in the Status Register **(STAT0, 16H...)** or **(STAT1, 17H...)**, and the Interrupt Trigger Edge Selection Register can be used to determine how the Status Register sets the Interrupt Status Register.

After the Interrupt Status Register **(INTS0, 18H...)** or **(INTS1, 19H...)** is read, the corresponding bit indicating which channel generates the interrupt in the **INTCH** register (**21H**) will be reset. Only when all the pending interrupt is acknowledged through reading the Interrupt Status Registers of all the channels **(INTS0, 18H...)** or **(INTS1, 19H...)** will all the bits in the **INTCH** register (**21H**) be reset and the $\overline{INT}$ pin become inactive.

There are totally twelve kinds of events that could be the interrupt source for one channel:

(1).LOS Detected
(2).AIS Detected
(3).Driver Failure Detected
(4).TCLK Loss
(5).Synchronization Status of PRBS
(6).PRBS Error Detected
(7).Code Violation Received
(8).Excessive Zeros Received
(9).JA FIFO Overflow/Underflow
(10).One-Second Timer Expired
(11). Error Counter Overflow
(12).Arbitrary Waveform Generator Overflow

Table-12 is a summary of all kinds of interrupt and the associated Status bit, Interrupt Status bit, Interrupt Trigger Edge Selection bit and Interrupt Mask bit.

Table-12 Interrupt Event

Interrupt Event	Status bit (STAT0, STAT1)	Interrupt Status bit (INTS0, INTS1)	Interrupt Edge Selection bit (INTES)	Interrupt Mask bit (INTM0, INTM1)
LOS Detected	LOS_S	LOS_IS	LOS_IES	LOS_IM
AIS Detected	AIS_S	AIS_IS	AIS_IES	AIS_IM
Driver Failure Detected	DF_S	DF_IS	DF_IES	DF_IM
TCLK Loss	TCLK_LOS	TCLK_LOS_IS	TCLK_IES	TCLK_IM
Synchronization Status of PRBS	PRBS_S	PRBS_IS	PRBS_IES	PRBS_IM
PRBS Error		ERR_IS		ERR_IM
Code Violation Received		CV_IS		CV_IM
Excessive Zeros Received		EXZ_IS		EXZ_IM
JA FIFO Overflow		JAOV_IS		JAOV_IM
JA FIFO Underflow		JAUD_IS		JAUD_IM
One-Second Timer Expired		TMOV_IS		TIMER_IM
Error Counter Overflow		CNT_OV_IS		CNT_IM
Arbitrary Waveform Generator Overflow		DAC_OV_IS		DAC_OV_IM

3.13 5V TOLERANT I/O PINS

All digital input pins will tolerate 5.0 ± 10% volts and are compatible with TTL logic.

3.14 RESET OPERATION

The chip can be reset in two ways:

- Software Reset: Writing to the **RST** register (**01H**) will reset the chip in 1 µs.
- Hardware Reset: Asserting the $\overline{RST}$ pin low for a minimum of 100 ns will reset the chip.

After reset, all drivers output are in high impedance state, all the internal flip-flops are reset, and all the registers are initialized to default values.

3.15 POWER SUPPLY

This chip uses a single 3.3 V power supply.

4 PROGRAMMING INFORMATION

4.1 REGISTER LIST AND MAP

The IDT82V2052E registers can be divided into Global Registers and Local Registers. The operation on the Global Registers affects both of the two channels while the operation on Local Registers only affects the specific channel. For different channel, the address of Local Register is different. Table-13 is the map of Global Registers and Table-14 is the map of Local Registers. If the configuration of both of the two channels is the same, the COPY bit (**GCF, 20H**) can be set to '1' to establish the Broadcasting mode. In the Broadcasting mode, the Writing operation on any of the two channels' registers will be copied to the corresponding registers of the other channel.

4.2 Reserved Registers

When writing to registers with reserved bit locations, the default state must be written to the reserved bits to ensure proper device operation.

Table-13 Global Register List and Map

Address (hex)		Register	R/W	MAP							
CH1	CH2			b7	b6	b5	b4	b3	b2	b1	b0
00		ID	R	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
01		RST	W								
20		GCF	R/W	MONT1	MONT0	-	-	COPY	INTM_GLB	INT_PIN1	INT_PIN0
21		INTCH	R	-	-	-	-	-	-	INT_CH2	INT_CH1

Table-14 Per Channel Register List and Map

Address (hex)		Register	R/W	MAP							
CH1	CH2			b7	b6	b5	b4	b3	b2	b1	b0
Transmit and receive termination register											
02	22	TERM	R/W	-	-	T_TERM2	T_TERM1	T_TERM0	R_TERM2	R_TERM1	R_TERM0
Jitter attenuation control register											
03	23	JACF	R/W	-	-	JA_LIMIT	JACF1	JACF0	JADP1	JADP0	JABW
Transmit path control registers											
04	24	TCF0	R/W	-	-	-	T_OFF	TD_INV	TCLK_SEL	T_MD1	T_MD0
05	25	TCF1	R/W	-	-	DFM_OFF	THZ	PULS3	PULS2	PULS1	PULS0
06	26	TCF2	R/W	-	-	SCAL5	SCAL4	SCAL3	SCAL2	SCAL1	SCAL0
07	27	TCF3	R/W	DONE	RW	UI1	UI0	SAMP3	SAMP2	SAMP1	SAMP0
08	28	TCF4	R/W	-	WDAT6	WDAT5	WDAT4	WDAT3	WDAT2	WDAT1	WDAT0
Receive path control registers											
09	29	RCF0	R/W	-	-	-	R_OFF	RD_INV	RCLK_SEL	R_MD1	R_MD0
0A	2A	RCF1	R/W	-	EQ_ON	-	LOS4	LOS3	LOS2	LOS1	LOS0
0B	2B	RCF2	R/W	-	-	SLICE1	SLICE0	-	-	MG1	MG0
Network Diagnostics control registers											
0C	2C	MAINT0	R/W	-	PATT1	PATT0	PATT_CLK	PRBS_INV	LAC	AISE	ATAO
0D	2D	MAINT1		-	-	-	-	-	RLP	ALP	DLP
0E-11	2E-31	MAINT2-MAINT5	R/W	-	-	-	-	-	-	-	-
12	32	MAINT6	R/W	-	BPV_INS	ERR_INS	EXZ_DEF	ERR_SEL1	ERR_SEL0	CNT_MD	CNT_TRF
Interrupt control registers											
13	33	INTM0	R/W	-	-	-	PRBS_IM	TCLK_IM	DF_IM	AIS_IM	LOS_IM
14	34	INTM1	R/W	DAC_OV_IM	JAOV_IM	JAUD_IM	ERR_IM	EXZ_IM	CV_IM	TIMER_IM	CNT_IM
15	35	INTES	R/W	-	-	-	PRBS_IES	TCLK_IES	DF_IES	AIS_IES	LOS_IES
Line status registers											
16	36	STAT0	R	-	-	-	PRBS_S	TCLK_LOS	DF_S	AIS_S	LOS_S
17	37	STAT1	R	-	-	RLP_S	-	-	-	-	-
Interrupt status registers											
18	38	INTS0	R	-	-	-	PRBS_IS	TCLK_LOS_IS	DF_IS	AIS_IS	LOS_IS
19	39	INTS1	R	DAC_OV_IS	JAOV_IS	JAUD_IS	ERR_IS	EXZ_IS	CV_IS	TMOV_IS	CNT_OV_IS
Counter registers											
1A	3A	CNT0	R	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1B	3B	CNT1	R	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8

4.3 REGISTER DESCRIPTION

4.3.1 GLOBAL REGISTERS

Table-15 ID: Device Revision Register
(R, Address = 00H)

Symbol	Bit	Default	Description
ID[7:0]	7-0	00H	Current Silicon Chip ID.

Table-16 RST: Reset Register
(W, Address = 01H)

Symbol	Bit	Default	Description
RST[7:0]	7-0	00H	Software reset. A write operation on this register will reset all internal registers to their default values, and the status of all ports are set to the default status. The content in this register can not be changed. After reset, all drivers output are in high impedance state.

Table-17 GCF: Global Configuration Register
(R/W, Address = 20H)

Symbol	Bit	Default	Description
MONT[1:0]	7-6	00	G.772 monitor = 00/10: Normal = 01: Receiver 1 monitors the receive path of channel 2 = 11: Receiver 1 monitors the transmit path of channel 2
-	5-4	00	Reserved.
COPY	3	0	Enable broadcasting mode. = 0: Broadcasting mode disabled = 1: Broadcasting mode enabled. Writing operation on one channel's register will be copied exactly to the corresponding registers in other channel.
INTM_GLB	2	1	Global interrupt enable = 0: Interrupt is globally enabled. But for each individual interrupt, it still can be disabled by its corresponding Interrupt mask Bit. = 1: All the interrupts are disabled for both channels.
INT_PIN[1:0]	1-0	00	Interrupt pin control = x0: Open drain, active low (with an external pull-up resistor) = 01: Push-pull, active low = 11: Push-pull, active high

Table-18 INTCH: Interrupt Channel Indication Register
(R, Address =21H)

Symbol	Bit	Default	Description
-	7-2	000000	Reserved.
INT_CH[1:0]	1-0	00	INT_CH[n]=0 indicates that an interrupt was generated by channel [n+1].

4.3.2 TRANSMIT AND RECEIVE TERMINATION REGISTER

Table-19 TERM: Transmit and Receive Termination Configuration Register
(R/W, Address = 02H, 22H)

Symbol	Bit	Default	Description
-	7-6	00	Reserved.
T_TERM[2:0]	5-3	000	These bits select the internal termination for transmit line impedance matching. = 000: Internal 75 Ω impedance matching = 001: Internal 120 Ω impedance matching = 010 / 011: Reserved = 1xx: Selects external impedance matching resistors (see Table-4).
R_TERM[2:0]	2-0	000	These bits select the internal termination for receive line impedance matching. = 000: Internal 75 Ω impedance matching = 001: Internal 120 Ω impedance matching = 010 / 011: Reserved = 1xx: Selects external impedance matching resistors (see Table-5).

4.3.3 JITTER ATTENUATION CONTROL REGISTER

Table-20 JACF: Jitter Attenuation Configuration Register
(R/W, Address = 03H, 23H)

Symbol	Bit	Default	Description
-	7-6	00	Reserved.
JA_LIMIT	5	1	= 0: Normal mode = 1: JA limit mode
JACF[1:0]	4-3	00	Jitter Attenuation configuration = 00/10: JA not used = 01: JA in transmit path = 11: JA in receive path
JADP[1:0]	2-1	00	Jitter Attenuation depth select = 00: 128 bits = 01: 64 bits = 1x: 32 bits
JABW	0	0	Jitter transfer function bandwidth select = 0: 6.8 Hz = 1: 0.9 Hz

4.3.4 TRANSMIT PATH CONTROL REGISTERS

Table-21 TCF0: Transmitter Configuration Register 0
(R/W, Address = 04H, 24H)

Symbol	Bit	Default	Description
-	7-5	000	Reserved
T_OFF	4	0	Transmitter power down enable = 0: Transmitter power up = 1: Transmitter power down (line driver high impedance)
TD_INV	3	0	Transmit data invert = 0: Data on TDn or TDPn/TDNn is active high = 1: Data on TDn or TDPn/TDNn is active low
TCLK_SEL	2	0	Transmit clock edge select = 0: Data on TDPn/TDNn is sampled on the falling edge of TCLKn = 1: Data on TDPn/TDNn is sampled on the rising edge of TCLKn
T_MD[1:0]	0-1	00	Transmitter operation mode control T_MD[1:0] select different stages of the transmit data path = 00: Enable HDB3 encoder and waveform shaper blocks. Input on pin TDn is single rail NRZ data = 01: Enable AMI encoder and waveform shaper blocks. Input on pin TDn is single rail NRZ data = 1x: Encoder is bypassed, dual rail NRZ transmit data input on pin TDPn/TDNn

Table-22 TCF1: Transmitter Configuration Register 1
(R/W, Address = 05H, 25H)

<table>
<tr><th>Symbol</th><th>Bit</th><th>Default</th><th colspan="4">Description</th></tr>
<tr><td>-</td><td>7-6</td><td>00</td><td colspan="4">Reserved. This bit should be ‘0’ for normal operation.</td></tr>
<tr><td>DFM_OFF</td><td>5</td><td>0</td><td colspan="4">Transmit driver failure monitor disable
= 0: DFM is enabled
= 1: DFM is disabled</td></tr>
<tr><td>THZ</td><td>4</td><td>1</td><td colspan="4">Transmit line driver high impedance enable
= 0: Normal state
= 1: Transmit line driver high impedance enable (other transmit path still work normally).</td></tr>
<tr><td rowspan="6">PULS[3:0]</td><td rowspan="6">3-0</td><td rowspan="6">0000</td><td colspan="4">These bits select the transmit template:</td></tr>
<tr><td></td><td>TCLK</td><td>Cable impedance</td><td>Allowable Cable loss</td></tr>
<tr><td>0000[1]</td><td>2.048 MHz</td><td>75 Ω</td><td>0-24 dB</td></tr>
<tr><td>0001</td><td>2.048 MHz</td><td>120 Ω</td><td>0-24 dB</td></tr>
<tr><td>0010 - 1011</td><td colspan="3">Reserved</td></tr>
<tr><td>11xx</td><td colspan="3">User programmable waveform setting</td></tr>
</table>

1. In internal impedance matching mode, for E1/75 Ω cable impedance, the PULS[3:0] bits (**TCF1, 05H...**) should be set to ‘0000’. In external impedance matching mode, for E1/75 Ω cable impedance, the PULS[3:0] bits should be set to ‘0001’.

Table-23 TCF2: Transmitter Configuration Register 2
(R/W, Address = 06H, 26H)

Symbol	Bit	Default	Description
-	7-6	00	Reserved.
SCAL[5:0]	5-0	100001	SCAL specifies a scaling factor to be applied to the amplitude of the user-programmable arbitrary pulses which is to be transmitted if needed. The default value of SCAL[5:0] is '100001'. Refer to 3.2.3.2 User-Programmable Arbitrary Waveform. = 100001: Default value for 75 Ω and 120 Ω. One step change of this value results in 3% scaling up/down against the pulse amplitude.

Table-24 TCF3: Transmitter Configuration Register 3
(R/W, Address = 07H, 27H)

Symbol	Bit	Default	Description
DONE	7	0	After '1' is written to this bit, a read or write operation is implemented.
RW	6	0	This bit selects read or write operation = 0: Write to RAM = 1: Read from RAM
UI[1:0]	5-4	00	These bits specify the unit interval address. There are totally 4 unit intervals. = 00: UI address is 0 (The most left UI) = 01: UI address is 1 = 10: UI address is 2 = 11: UI address is 3
SAMP[3:0]	3-0	0000	These bits specify the sample address. Each UI has totally 16 samples. = 0000: Sample address is 0 (The most left sample) = 0001: Sample address is 1 = 0010: Sample address is 2 …… = 1110: Sample address is 14 = 1111: Sample address is 15

Table-25 TCF4: Transmitter Configuration Register 4
(R/W, Address = 08H, 28H)

Symbol	Bit	Default	Description
-	7	0	Reserved
WDAT[6:0]	6-0	0000000	In Indirect Write operation, the WDAT[6:0] will be loaded to the pulse template RAM, specifying the amplitude of the Sample. After an Indirect Read operation, the amplitude data of the Sample in the pulse template RAM will be output to the WDAT[6:0].

4.3.5 RECEIVE PATH CONTROL REGISTERS

Table-26 RCF0: Receiver Configuration Register 0
(R/W, Address = 09H, 29H)

Symbol	Bit	Default	Description
-	7-5	000	Reserved
R_OFF	4	0	Receiver power down enable = 0: Receiver power up = 1: Receiver power down
RD_INV	3	0	Receive data invert = 0: Data on RDn or RDPn/RDNn is active high = 1: Data on RDn or RDPn/RDNn is active low
RCLK_SEL	2	0	Receive clock edge select (this bit is ignored in slicer mode) = 0: Data on RDn or RDPn/RDNn is updated on the rising edge of RCLKn = 1: Data on RDn or RDPn/RDNn is updated on the falling edge of RCLKn
R_MD[1:0]	1-0	00	Receive path decoding selection = 00: Receive data is HDB3 decoded and output on RDn pin with single rail NRZ format = 01: Receive data is AMI decoded and output on RDn pin with single rail NRZ format = 10: Decoder is bypassed, re-timed dual rail data with NRZ format output on RDPn/RDNn (dual rail mode with clock recovery) = 11: CDR and decoder are bypassed, slicer data with RZ format output on RDPn/RDNn (slicer mode)

Table-27 RCF1: Receiver Configuration Register 1
(R/W, Address= 0AH, 2AH)

Symbol	Bit	Default	Description		
-	7	0	Reserved		
EQ_ON	6	0	= 0: Receive equalizer off = 1: Receive equalizer on (LOS programming enabled)		
-	5	0	Reserved.		
LOS[4:0]	4:0	10101		LOS Clear Level (dB)	LOS Declare Level (dB)
			00000	0	<-4
			00001	>-2	<-6
			00010	>-4	<-8
			00011	>-6	<-10
			00100	>-8	<-12
			00101	>-10	<-14
			00110	>-12	<-16
			00111	>-14	<-18
			01000	>-16	<-20
			01001	>-18	<-22
			01010	>-20	<-24
			01011 - 11111	Reserved	

Table-28 RCF2: Receiver Configuration Register 2
(R/W, Address = 0BH, 2BH)

Symbol	Bit	Default	Description
-	7-6	00	Reserved.
SLICE[1:0]	5-4	01	Receive slicer threshold = 00: The receive slicer generates a mark if the voltage on RTIPn/RRINGn exceeds 40% of the peak amplitude. = 01: The receive slicer generates a mark if the voltage on RTIPn/RRINGn exceeds 50% of the peak amplitude. = 10: The receive slicer generates a mark if the voltage on RTIPn/RRINGn exceeds 60% of the peak amplitude. = 11: The receive slicer generates a mark if the voltage on RTIPn/RRINGn exceeds 70% of the peak amplitude.
-	3-2	10	Reserved
MG[1:0]	1-0	00	Monitor gain setting: these bits select the internal linear gain boost = 00: 0 dB = 01: 22 dB = 10: 26 dB = 11: 32 dB

4.3.6 NETWORK DIAGNOSTICS CONTROL REGISTERS

Table-29 MAINT0: Maintenance Function Control Register 0
(R/W, Address = 0CH, 2CH)

Symbol	Bit	Default	Description
-	7	0	Reserved.
PATT[1:0]	6-5	00	These bits select the internal pattern and insert it into transmit data stream. = 00: Normal operation (PATT_CLK = 0) / insert all zeros (PATT_CLK = 1) = 01: Insert All Ones = 10: Insert PRBS (E1: 2^{15}-1) = 11: Reserved
PATT_CLK	4	0	Selects reference clock for transmitting internal pattern = 0: Uses TCLKn as the reference clock = 1: Uses MCLK as the reference clock
PRBS_INV	3	0	Inverts PRBS = 0: The PRBS data is not inverted = 1: The PRBS data is inverted before transmission and detection
LAC	2	0	LOS/AIS criterion is selected as below: = 0: G.775 = 1: ETSI 300233& I.431
AISE	1	0	AIS enable during LOS = 0: AIS insertion on RDPn/RDNn/RCLKn is disabled during LOS = 1: AIS insertion on RDPn/RDNn/RCLKn is enabled during LOS
ATAO	0	0	Automatically Transmit All Ones (enabled only when PATT[1:0] = 00) = 0: Disabled = 1: Automatically Transmit All Ones pattern at TTIPn/TRINGn during LOS

Table-30 MAINT1: Maintenance Function Control Register 1
(R/W, Address= 0DH, 2DH)

Symbol	Bit	Default	Description
-	7-3	00000	Reserved
RLP	2	0	Remote loopback enable = 0: Disables remote loopback (normal transmit and receive operation) = 1: Enables remote loopback
ALP	1	0	Analog loopback enable = 0: Disables analog loopback (normal transmit and receive operation) = 1: Enables analog loopback
DLP	0	0	Digital loopback enable = 0: Disables digital loopback (normal transmit and receive operation) = 1: Enables digital loopback

Table-31 MAINT6: Maintenance Function Control Register 6
(R/W, Address = 12H, 32H)

Symbol	Bit	Default	Description
-	7	0	Reserved.
BPV_INS	6	0	BPV error insertion A '0' to '1' transition on this bit will cause a single bipolar violation error to be inserted into the transmit data stream. This bit must be cleared and set again for a subsequent error to be inserted.
ERR_INS	5	0	PRBS logic error insertion A '0' to '1' transition on this bit will cause a single PRBS logic error to be inserted into the transmit PRBS data stream. This bit must be cleared and set again for a subsequent error to be inserted.
EXZ_DEF	4	0	EXZ definition select = 0: ANSI = 1: FCC
ERR_SEL	3-2	00	These bits choose which type of error will be counted = 00: The PRBS logic error is counted by a 16-bit error counter = 01: The EXZ error is counted by a 16-bit error counter = 10: The Received CV (BPV) error is counted by a 16-bit error counter = 11: Both CV (BPV) and EXZ errors are counted by a 16-bit error counter.
CNT_MD	1	0	Counter operation mode select = 0: Manual Report mode = 1: Auto Report mode
CNT_TRF	0	0	= 0: Clear this bit for the next '0' to '1' transition on this bit. = 1: Error counting result is transferred to CNT0 and CNT1 and the error counter is reset.

4.3.7 INTERRUPT CONTROL REGISTERS

Table-32 INTM0: Interrupt Mask Register 0
(R/W, Address = 13H, 33H)

Symbol	Bit	Default	Description
-	7-5	111	Reserved
PRBS_IM	4	1	PRBS synchronic signal detect interrupt mask = 0: PRBS synchronic signal detect interrupt enabled = 1: PRBS synchronic signal detect interrupt masked
TCLK_IM	3	1	TCLK loss detect interrupt mask = 0: TCLK loss detect interrupt enabled = 1: TCLK loss detect interrupt masked
DF_IM	2	1	Driver Failure interrupt mask = 0: Driver Failure interrupt enabled = 1: Driver Failure interrupt masked
AIS_IM	1	1	Alarm Indication Signal interrupt mask = 0: Alarm Indication Signal interrupt enabled = 1: Alarm Indication Signal interrupt masked
LOS_IM	0	1	Loss Of Signal interrupt mask = 0: Loss Of Signal interrupt enabled = 1: Loss Of Signal interrupt masked

Table-33 INTM1: Interrupt Masked Register 1
(R/W, Address = 14H, 34H)

Symbol	Bit	Default	Description
DAC_OV_IM	7	1	DAC arithmetic overflow interrupt mask = 0: DAC arithmetic overflow interrupt enabled = 1: DAC arithmetic overflow interrupt masked
JAOV_IM	6	1	JA overflow interrupt mask = 0: JA overflow interrupt enabled = 1: JA overflow interrupt masked
JAUD_IM	5	1	JA underflow interrupt mask = 0: JA underflow interrupt enabled = 1: JA underflow interrupt masked
ERR_IM	4	1	PRBS logic error detect interrupt mask = 0: PRBS logic error detect interrupt enabled = 1: PRBS logic error detect interrupt masked
EXZ_IM	3	1	Receive excess zeros interrupt mask = 0: Receive excess zeros interrupt enabled = 1: Receive excess zeros interrupt masked
CV_IM	2	1	Receive error interrupt mask = 0: Receive error interrupt enabled = 1: Receive error interrupt masked
TIMER_IM	1	1	One-Second Timer expiration interrupt mask = 0: One-Second Timer expiration interrupt enabled = 1: One-Second Timer expiration interrupt masked
CNT_IM	0	1	Counter overflow interrupt mask = 0: Counter overflow interrupt enabled = 1: Counter overflow interrupt masked

Table-34 INTES: Interrupt Trigger Edge Select Register
(R/W, Address = 15H, 35H)

Symbol	Bit	Default	Description
-	7-5	000	Reserved
PRBS_IES	4	0	This bit determines the PRBS synchronization status interrupt event. = 0: Interrupt event is generated as a '0' to '1' transition of the PRBS_S bit in STAT0 status register = 1: Interrupt event is generated as either a '0' to '1' transition or a '1' to '0' transition of the PRBS_S bit in STAT0 status register
TCLK_IES	3	0	This bit determines the TCLK Loss interrupt event. = 0: Interrupt event is generated as a '0' to '1' transition of the TCLK_LOS bit in STAT0 status register = 1: Interrupt event is generated as either a '0' to '1' transition or a '1' to '0' transition of the TCLK_LOS bit in STAT0 status register
DF_IES	2	0	This bit determines the Driver Failure interrupt event. = 0: Interrupt event is generated as a '0' to '1' transition of the DF_S bit in STAT0 status register = 1: Interrupt event is generated as either a '0' to '1' transition or a '1' to '0' transition of the DF_S bit in STAT0 status register
AIS_IES	1	0	This bit determines the AIS interrupt event. = 0: Interrupt event is generated as a '0' to '1' transition of the AIS_S bit in STAT0 status register = 1: Interrupt event is generated as either a '0' to '1' transition or a '1' to '0' transition of the AIS_S bit in STAT0 status register
LOS_IES	0	0	This bit determines the LOS interrupt event. = 0: Interrupt is generated as a '0' to '1' transition of the LOS_S bit in STAT0 status register = 1: Interrupt is generated as either a '0' to '1' transition or a '1' to '0' transition of the LOS_S bit in STAT0 status register

4.3.8 LINE STATUS REGISTERS

Table-35 STAT0: Line Status Register 0 (real time status monitor)
(R, Address = 16H, 36H)

Symbol	Bit	Default	Description
-	7-5	000	Reserved
PRBS_S	4	0	Synchronous status indication of PRBS (real time) = 0: 2^{15}-1 PRBS not detected = 1: 2^{15}-1 PRBS detected Note: If PRBS_IM=0: A '0' to '1' transition on this bit causes a synchronous status detected interrupt if PRBS _IES bit is '0'. Any changes of this bit causes an interrupt if PRBS_IES bit is set to '1'.
TCLK_LOS	3	0	TCLKn loss indication = 0: Normal = 1: TCLK pin has not toggled for more than 70 MCLK cycles Note: If TCLK_IM=0: A '0' to '1' transition on this bit causes an interrupt if TCLK _IES bit is '0'. Any changes of this bit causes an interrupt if TCLK_IES bit is set to '1'.
DF_S	2	0	Line driver status indication = 0: Normal operation = 1: Line driver short circuit is detected. Note: If DF_IM=0 A '0' to '1' transition on this bit causes an interrupt if DF _IES bit is '0'. Any changes of this bit causes an interrupt if DF_IES bit is set to '1'.
AIS_S	1	0	Alarm Indication Signal status detection = 0: No AIS signal is detected in the receive path = 1: AIS signal is detected in the receive path Note: If AIS_IM=0 A '0' to '1' transition on this bit causes an interrupt if AIS _IES bit is '0'. Any changes of this bit causes an interrupt if AIS_IES bit is set to '1'.
LOS_S	0	0	Loss Of Signal status detection = 0: Loss of signal on RTIPn/RRINGn is not detected = 1: Loss of signal on RTIPn/RRINGn is detected. Note: If LOS_IM=0 A '0' to '1' transition on this bit causes an interrupt if LOS _IES bit is '0'. Any changes of this bit causes an interrupt if LOS_IES bit is set to '1'.

Table-36 STAT1: Line Status Register 1 (real time status monitor)
(R, Address = 17H, 37H)

Symbol	Bit	Default	Description
-	7-6	00	Reserved.
RLP_S	5	0	Indicating the status of Remote Loopback = 0: The remote loopback is inactive. = 1: The remote loopback is active (closed).
-	4-0	00000	Reserved

4.3.9 INTERRUPT STATUS REGISTERS

Table-37 INTS0: Interrupt Status Register 0
(R, Address = 18H, 38H) (this register is reset and relevant interrupt request is cleared after a read)

Symbol	Bit	Default	Description
-	7-5	000	Reserved
PRBS_IS	4	0	This bit indicates the occurrence of the interrupt event generated by the PRBS synchronization status. = 0: No PRBS synchronization status interrupt event occurred = 1: PRBS synchronization status interrupt event occurred
TCLK_LOS_IS	3	0	This bit indicates the occurrence of the interrupt event generated by the TCLK loss detection. = 0: No TCLK loss interrupt event. = 1:TCLK loss interrupt event occurred.
DF_IS	2	0	This bit indicates the occurrence of the interrupt event generated by the Driver Failure. = 0: No Driver Failure interrupt event occurred = 1: Driver Failure interrupt event occurred
AIS_IS	1	0	This bit indicates the occurrence of the AIS (Alarm Indication Signal) interrupt event. = 0: No AIS interrupt event occurred = 1: AIS interrupt event occurred
LOS_IS	0	0	This bit indicates the occurrence of the LOS (Loss of signal) interrupt event. = 0: No LOS interrupt event occurred = 1: LOS interrupt event occurred

Table-38 INTS1: Interrupt Status Register 1

(R, Address = 19H, 39H) (this register is reset and the relevant interrupt request is cleared after a read)

Symbol	Bit	Default	Description
DAC_OV_IS	7	0	This bit indicates the occurrence of the pulse amplitude overflow of Arbitrary Waveform Generator interrupt event. = 0: No pulse amplitude overflow of Arbitrary Waveform Generator interrupt event occurred = 1: The pulse amplitude overflow of Arbitrary Waveform Generator interrupt event occurred
JAOV_IS	6	0	This bit indicates the occurrence of the Jitter Attenuator Overflow interrupt event. = 0: No JA Overflow interrupt event occurred = 1: JA Overflow interrupt event occurred
JAUD_IS	5	0	This bit indicates the occurrence of the Jitter Attenuator Underflow interrupt event. = 0: No JA Underflow interrupt event occurred = 1: JA Underflow interrupt event occurred
ERR_IS	4	0	This bit indicates the occurrence of the interrupt event generated by the detected PRBS logic error. = 0: No PRBS logic error interrupt event occurred = 1: PRBS logic error interrupt event occurred
EXZ_IS	3	0	This bit indicates the occurrence of the Excessive Zeros interrupt event. = 0: No Excessive Zeros interrupt event occurred = 1: EXZ interrupt event occurred
CV_IS	2	0	This bit indicates the occurrence of the Code Violation interrupt event. = 0: No Code Violation interrupt event occurred = 1: Code Violation interrupt event occurred
TMOV_IS	1	0	This bit indicates the occurrence of the One-Second Timer Expiration interrupt event. = 0: No One-Second Timer Expiration interrupt event occurred = 1: One-Second Timer Expiration interrupt event occurred
CNT_OV_IS	0	0	This bit indicates the occurrence of the Counter Overflow interrupt event. = 0: No Counter Overflow interrupt event occurred = 1: Counter Overflow interrupt event occurred

4.3.10 COUNTER REGISTERS

Table-39 CNT0: Error Counter L-byte Register 0

(R, Address = 1AH, 3AH)

Symbol	Bit	Default	Description
CNT_L[7:0]	7-0	00H	This register contains the lower eight bits of the 16-bit error counter. CNT_L[0] is the LSB.

Table-40 CNT1: Error Counter H-byte Register 1

(R, Address = 1BH, 3BH)

Symbol	Bit	Default	Description
CNT_H[7:0]	7-0	00H	This register contains the upper eight bits of the 16-bit error counter. CNT_H[7] is the MSB.

5 HARDWARE CONTROL PIN SUMMARY

Table-41 Hardware Control Pin Summary

<table>
<tr><th>Pin No.
TQFP</th><th>Symbol</th><th>Description</th></tr>
<tr><td>9
10</td><td>MODE1
MODE0</td><td>MODE[1:0]: Operation mode of Control interface select (global control)
00= Hardware interface
01= Serial interface
10= Parallel - non-Multiplexed - Motorola Interface
11= Parallel - non-Multiplexed - Intel Interface</td></tr>
<tr><td>13
12</td><td>TERM1
TERM2</td><td>TERMn: Termination interface select (per channel control)
These pins select internal or external impedance matching for channel n (n=1 or 2)
0 = ternary interface with internal impedance matching network.
1 = ternary interface with external impedance matching network</td></tr>
<tr><td>14
15</td><td>RXTXM1
RXTXM0</td><td>RXTXM[1:0]: Receive and transmit path operation mode select (global control)
00= single rail with HDB3 coding
01= single rail with AMI coding
10= dual rail interface with CDR enable
11= slicer mode</td></tr>
<tr><td>51

47</td><td>PULS1

PULS2</td><td>PULSn: These pins are used to select the following functions (per channel control):
• Transmit pulse template
• Internal termination impedance (75 Ω / 120 Ω)
<table>
<tr><th>PULSn</th><th>TCLK</th><th>Cable impedance (internal matching impedance)</th><th>Cable loss</th></tr>
<tr><td>0</td><td>2.048 MHz</td><td>75Ω</td><td>0-24 dB</td></tr>
<tr><td>1</td><td>2.048 MHz</td><td>120Ω</td><td>0-24 dB</td></tr>
</table></td></tr>
<tr><td>57
59</td><td>RPD1
RPD2</td><td>RPDn: Receiver power down control (per channel control)
0= Normal operation
1= receiver power down</td></tr>
<tr><td>46
45

56
55</td><td>PATT11
PATT10

PATT21
PATT20</td><td>PATTn[1:0]: Transmit test pattern select (per channel control)
In hardware control mode, these pins select the transmit pattern for channel n (n=1 or 2)
00 = normal
01= All Ones
10= PRBS
11= transmitter power down</td></tr>
<tr><td>16
17</td><td>JA1
JA0</td><td>JA[1:0]: Jitter attenuation position, bandwidth and the depth of FIFO select (global control)
00= JA is disabled
01= JA in receiver, broad bandwidth, FIFO=64 bits
10= JA in receiver, narrow bandwidth, FIFO=128 bits
11= JA in transmitter, narrow bandwidth, FIFO=128 bits</td></tr>
<tr><td>19
18</td><td>MONT1
MONT2</td><td>MONTn: Receive Monitor n gain select (per channel control)
In hardware control mode with ternary interface, this pin selects the receive monitor gain for receiver n (n=1 or 2)
0= 0 dB
1= 26 dB</td></tr>
<tr><td>42
41

44
43</td><td>LP11
LP10

LP21
LP20</td><td>LPn[1:0]: Loopback mode select (per channel control)
When the chip is configured by hardware, these pins are used to select loopback operation modes for channel n.
00= no loopback
01= analog loopback
10= digital loopback
11= remote loopback</td></tr>
<tr><td>20</td><td>THZ</td><td>THZ: Transmitter Driver High Impedance Enable (global control)
This signal enables or disables both of the transmitter drivers. A low level on this pin enables both of the two drivers while a high level on this pin places both of the two drivers in high impedance state.</td></tr>
</table>

Table-41 Hardware Control Pin Summary (Continued)

Pin No. TQFP	Symbol	Description
11	RCLKE	**RCLKE: the active edge of RCLKn select when hardware control mode is used (global control)** 0= select the rising edge as active edge of RCLKn 1= select the falling edge as active edge of RCLKn
48 49 50 52 53 54 58 60	-	In Hardware mode, these pins have to be tied to GND.

6 IEEE STD 1149.1 JTAG TEST ACCESS PORT

The IDT82V2052E supports the digital Boundary Scan Specification as described in the IEEE 1149.1 standards.

The boundary scan architecture consists of data and instruction registers plus a Test Access Port (TAP) controller. Control of the TAP is performed through signals applied to the Test Mode Select (TMS) and Test Clock (TCK) pins. Data is shifted into the registers via the Test Data Input (TDI) pin, and shifted out of the registers via the Test Data Output (TDO) pin. Both TDI and TDO are clocked at a rate determined by TCK.

The JTAG boundary scan registers include BSR (Boundary Scan Register), IDR (Device Identification Register), BR (Bypass Register) and IR (Instruction Register). These will be described in the following pages. Refer to Figure-19 for architecture.

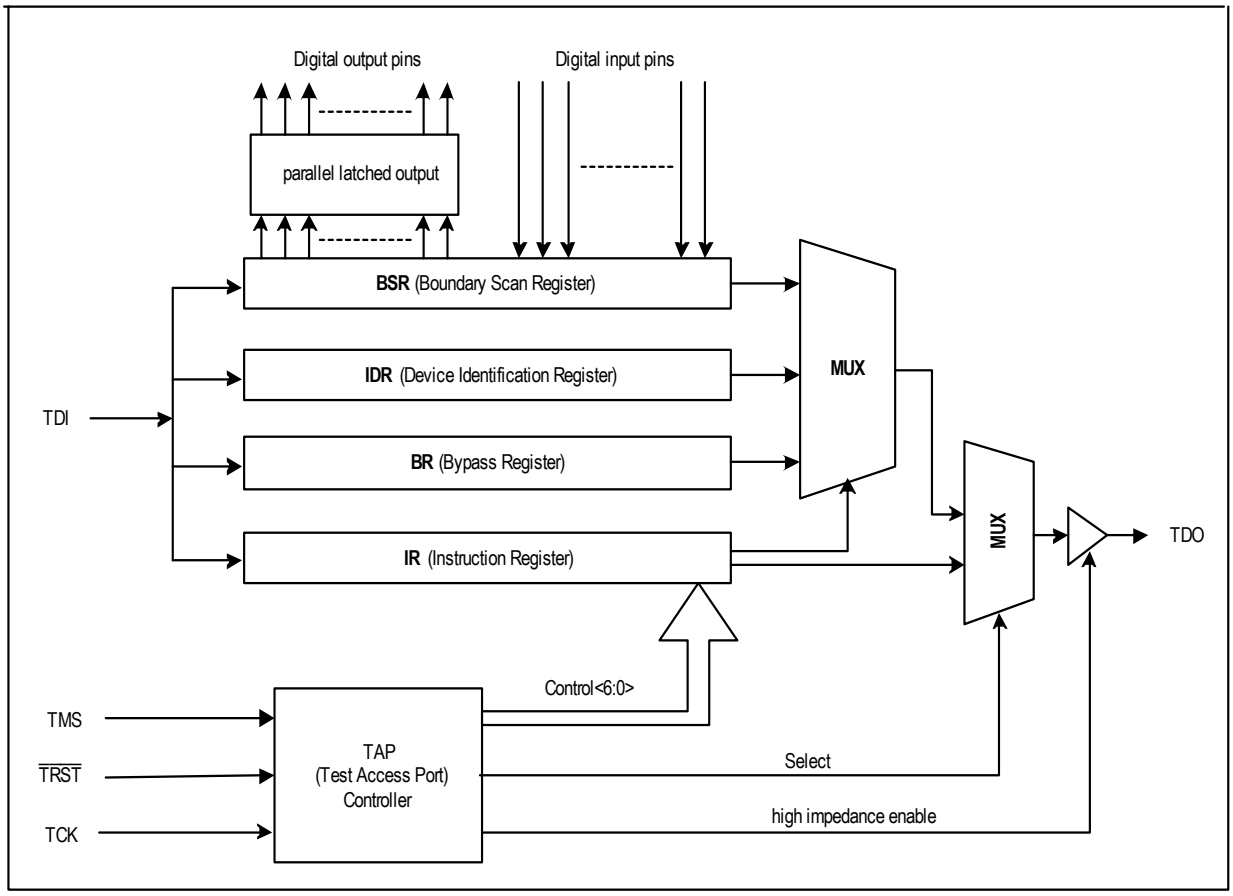


Figure-19 JTAG Architecture

6.1 JTAG INSTRUCTIONS AND INSTRUCTION REGISTER

The IR (Instruction Register) with instruction decode block is used to select the test to be executed or the data register to be accessed or both.

The instructions are shifted in LSB first to this 3-bit register. See Table-42 for details of the codes and the instructions related.

Table-42 Instruction Register Description

IR CODE	INSTRUCTION	COMMENTS
000	Extest	The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is placed between TDI and TDO. The signal on the input pins can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. The signal on the output pins can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.
100	Sample / Preload	The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. The normal path between IDT82V2052E logic and the I/O pins is maintained. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.
110	Idcode	The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.
111	Bypass	The bypass instruction shifts data from input TDI to output TDO with one TCK clock period delay. The instruction is used to bypass the device.

6.2 JTAG DATA REGISTER

6.2.1 DEVICE IDENTIFICATION REGISTER (IDR)

The IDR can be set to define the producer number, part number and the device revision, which can be used to verify the proper version or revision number that has been used in the system under test. The IDR is 32 bits long and is partitioned as in Table-43. Data from the IDR is shifted out to TDO LSB first.

Table-43 Device Identification Register Description

Bit No.	Comments
0	Set to '1'
1-11	Producer Number
12-27	Part Number
28-31	Device Revision

6.2.2 BYPASS REGISTER (BR)

The BR consists of a single bit. It can provide a serial path between the TDI input and TDO output, bypassing the BSR to reduce test access times.

6.2.3 BOUNDARY SCAN REGISTER (BSR)

The BSR can apply and read test patterns in parallel to or from all the digital I/O pins. The BSR is a 98 bits long shift register and is initialized and read using the instruction EXTEST or SAMPLE/PRELOAD. Each pin is related to one or more bits in the BSR. For details, please refer to the BSDL file.

6.2.4 TEST ACCESS PORT CONTROLLER

The TAP controller is a 16-state synchronous state machine. Figure-20 shows its state diagram following the description of each state. Note that the figure contains two main branches to access either the data or instruction registers. The value shown next to each state transition in this figure states the value present at TMS at each rising edge of TCK. Please refer to Table-44 for details of the state description.

Table-44 TAP Controller State Description

STATE	DESCRIPTION
Test Logic Reset	In this state, the test logic is disabled. The device is set to normal operation. During initialization, the device initializes the instruction register with the IDCODE instruction. Regardless of the original state of the controller, the controller enters the Test-Logic-Reset state when the TMS input is held high for at least 5 rising edges of TCK. The controller remains in this state while TMS is high. The device processor automatically enters this state at power-up.
Run-Test/Idle	This is a controller state between scan operations. Once in this state, the controller remains in the state as long as TMS is held low. The instruction register and all test data registers retain their previous state. When TMS is high and a rising edge is applied to TCK, the controller moves to the Select-DR state.
Select-DR-Scan	This is a temporary controller state and the instruction does not change in this state. The test data register selected by the current instruction retains its previous state. If TMS is held low and a rising edge is applied to TCK when in this state, the controller moves into the Capture-DR state and a scan sequence for the selected test data register is initiated. If TMS is held high and a rising edge applied to TCK, the controller moves to the Select-IR-Scan state.
Capture-DR	In this state, the Boundary Scan Register captures input pin data if the current instruction is EXTEST or SAMPLE/PRELOAD. The instruction does not change in this state. The other test data registers, which do not have parallel input, are not changed. When the TAP controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-DR state if TMS is high or the Shift-DR state if TMS is low.
Shift-DR	In this controller state, the test data register connected between TDI and TDO as a result of the current instruction shifts data on stage toward its serial output on each rising edge of TCK. The instruction does not change in this state. When the TAP controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-DR state if TMS is high or remains in the Shift-DR state if TMS is low.
Exit1-DR	This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-DR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Pause-DR state. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.
Pause-DR	The pause state allows the test controller to temporarily halt the shifting of data through the test data register in the serial path between TDI and TDO. For example, this state could be used to allow the tester to reload its pin memory from disk during application of a long test sequence. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state. The controller remains in this state as long as TMS is low. When TMS goes high and a rising edge is applied to TCK, the controller moves to the Exit2-DR state.
Exit2-DR	This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-DR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Shift-DR state. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.
Update-DR	The Boundary Scan Register is provided with a latched parallel output to prevent changes while data is shifted in response to the EXTEST and SAMPLE/PRELOAD instructions. When the TAP controller is in this state and the Boundary Scan Register is selected, data is latched into the parallel output of this register from the shift-register path on the falling edge of TCK. The data held at the latched parallel output changes only in this state. All shift-register stages in the test data register selected by the current instruction retain their previous value and the instruction does not change during this state.
Select-IR-Scan	This is a temporary controller state. The test data register selected by the current instruction retains its previous state. If TMS is held low and a rising edge is applied to TCK when in this state, the controller moves into the Capture-IR state, and a scan sequence for the instruction register is initiated. If TMS is held high and a rising edge is applied to TCK, the controller moves to the Test-Logic-Reset state. The instruction does not change during this state.
Capture-IR	In this controller state, the shift register contained in the instruction register loads a fixed value of '100' on the rising edge of TCK. This supports fault-isolation of the board-level serial test data path. Data registers selected by the current instruction retain their value and the instruction does not change during this state. When the controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-IR state if TMS is held high, or the Shift-IR state if TMS is held low.
Shift-IR	In this state, the shift register contained in the instruction register is connected between TDI and TDO and shifts data one stage towards its serial output on each rising edge of TCK. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state. When the controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-IR state if TMS is held high, or remains in the Shift-IR state if TMS is held low.
Exit1-IR	This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-IR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Pause-IR state. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.
Pause-IR	The pause state allows the test controller to temporarily halt the shifting of data through the instruction register. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state. The controller remains in this state as long as TMS is low. When TMS goes high and a rising edge is applied to TCK, the controller moves to the Exit2-IR state.

Table-44 TAP Controller State Description (Continued)

STATE	DESCRIPTION
Exit2-IR	This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-IR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Shift-IR state. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.
Update-IR	The instruction shifted into the instruction register is latched into the parallel output from the shift-register path on the falling edge of TCK. When the new instruction has been latched, it becomes the current instruction. The test data registers selected by the current instruction retain their previous value.

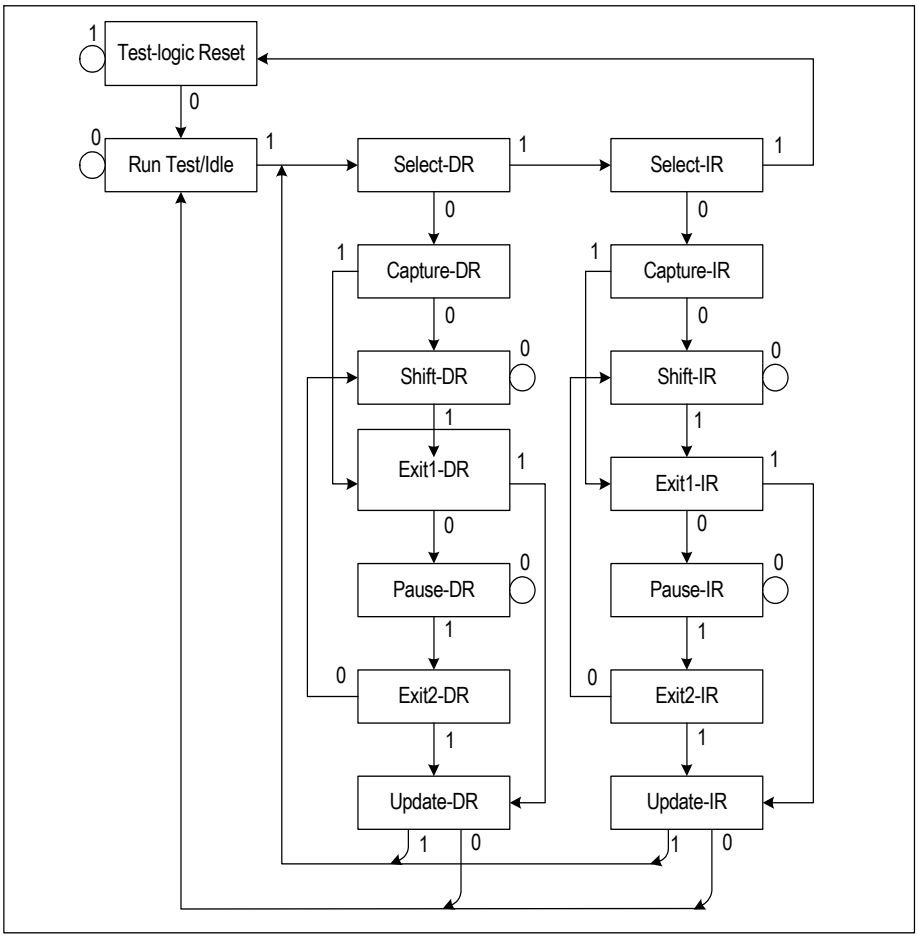


Figure-20 JTAG State Diagram

7 TEST SPECIFICATIONS

Table-45 Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit
VDDA, VDDD	Core Power Supply	-0.5	4.6	V
VDDIO	I/O Power Supply	-0.5	4.6	V
VDDT1-2	Transmit Power Supply	-0.5	4.6	V
VDDR1-2	Receive Power Supply	-0.5	4.6	V
Vin	Input Voltage, Any Digital Pin	GND-0.5	5.5	V
	Input Voltage, Any RTIPn and RRINGn pin[1]	GND-0.5	VDDR+0.5	V
	ESD Voltage, any pin	2000 [2]		V
		500 [3]		V
Iin	Transient latch-up current, any pin		100	mA
	Input current, any digital pin [4]	-10	10	mA
	DC Input current, any analog pin [4]		±100	mA
Pd	Maximum power dissipation in package		1.23	W
Tc	Case Temperature		120	°C
Ts	Storage Temperature	-65	+150	°C
CAUTION: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.				

1.Reference to ground
2.Human body model
3.Charge device model
4.Constant input current

Table-46 Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDDA,VDDD	Core Power Supply	3.13	3.3	3.47	V
VDDIO	I/O Power Supply	3.13	3.3	3.47	V
VDDT	Transmitter Power Supply	3.13	3.3	3.47	V
VDDR	Receive Power Supply	3.13	3.3	3.47	V
TA	Ambient operating temperature	-40	25	85	°C
Total current dissipation[1,2,3]	75 Ω load				
	50% ones density data	-	100	110	mA
	100% ones density data	-	130	140	
	120 Ω Load				
	50% ones density data	-	110	120	mA
	100% ones density data	-	130	140	

1.Power consumption includes power consumption on device and load. Digital levels are 10% of the supply rails and digital outputs driving a 50 pF capacitive load.
2.Maximum power consumption over the full operating temperature and power supply voltage range.
3.In short haul mode, if internal impedance matching is chosen, 75Ω power dissipation values are measured with template PULS[3:0] = 0000; 120Ω power dissipation values are measured with template PULS[3:0] = 0001.

Table-47 Power Consumption

Symbol	Parameter	Min	Typ	Max[1,2]	Unit
	3.3 V, 75 Ω Load				
	50% ones density data:	-	330	-	mW
	100% ones density data:	-	430	490	
	3.3 V, 120 Ω Load				
	50% ones density data:	-	370	-	mW
	100% ones density data:	-	430	490	

1.Maximum power and current consumption over the full operating temperature and power supply voltage range. Includes all channels.
2.Power consumption includes power absorbed by line load and external transmitter components.

Table-48 DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input Low Level Voltage	-	-	0.8	V
V_{IH}	Input High Voltage	2.0	-	-	V
V_{OL}	Output Low level Voltage (Iout=1.6mA)	-	-	0.4	V
V_{OH}	Output High level Voltage (Iout=400μA)	2.4	-	VDDIO	V
V_{MA}	Analog Input Quiescent Voltage (RTIPn, RRINGn pin while floating)		1.5		V
I_I	Input Leakage Current				
	TMS, TDI, $\overline{TRST}$			50	μA
	All other digital input pins	-10		10	μA
I_{ZL}	High Impedance Leakage Current	-10		10	μA
Ci	Input capacitance			15	pF
Co	Output load capacitance			50	pF
Co	Output load capacitance (bus pins)			100	pF

Table-49 Receiver Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test conditions
	Receiver sensitivity Adaptive Equalizer disabled: Adaptive Equalizer enabled:			 -10 -20	 dB	
	Analog LOS level Adaptive Equalizer disabled: Adaptive Equalizer enabled:	 -4	 800 	 -24	 mVp-p dB	A LOS level is programmable with Adaptive Equalizer enabled. Not available in Hardware mode.
	Allowable consecutive zeros before LOS G.775: I.431/ETSI300233:		 32 2048			
	LOS reset	12.5			% ones	G.775, ETSI 300 233
	Receive Intrinsic Jitter 20Hz - 100kHz			 0.05	 U.I.	JA enabled
	Input Jitter Tolerance 1 Hz – 20 Hz 20 Hz – 2.4 KHz 18 KHz – 100 KHz	 37 5 2			 U.I. U.I. U.I.	G.823, with 6 dB cable attenuation
ZDM	Receiver Differential Input Impedance	20			KΩ	Internal mode
	Input termination resistor tolerance			±1%		
RRX	Receive Return Loss 51 KHz – 102 KHz 102 KHz - 2.048 MHz 2.048 MHz – 3.072 MHz	 20 20 20			 dB dB dB	G.703 Internal termination
RPD	Receive path delay Single rail Dual rail		 7 2		 U.I. U.I.	JA disabled

Table-50 Transmitter Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Vo-p	Output pulse amplitudes 75Ω load 120Ω load	 2.14 2.7	 2.37 3.0	 2.60 3.3	 V V
Vo-s	Zero (space) level 75Ω load 120Ω load	 -0.237 -0.3		 0.237 0.3	 V V
	Transmit amplitude variation with supply	-1		+1	%
	Difference between pulse sequences for 17 consecutive pulses (T1.102)			200	mV
Tpw	Output Pulse Width at 50% of nominal amplitude	232	244	256	ns
	Ratio of the amplitudes of Positive and Negative Pulses at the center of the pulse interval (G.703)	0.95		1.05	
	Ratio of the width of Positive and Negative Pulses at the center of the pulse interval (G.703)	0.95		1.05	
RTX	Transmit Return Loss (G.703)				
	51 KHz – 102 KHz 102 KHz - 2.048 MHz 2.048 MHz – 3.072 MHz		20 15 12		dB dB dB
JTXp-p	Intrinsic Transmit Jitter (TCLK is jitter free)				
	20 Hz – 100 KHz			0.050	U.I.
Td	Transmit path delay (JA is disabled)				
	Single rail Dual rail		8.5 4.5		U.I. U.I.
Isc	Line short circuit current; tested on the TTIP/TRING pins		100		mAp

Table-51 Transmitter and Receiver Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
	MCLK frequency		2.048		MHz
	MCLK tolerance	-100		100	ppm
	MCLK duty cycle	30		70	%
Transmit path					
	TCLK frequency		2.048		MHz
	TCLK tolerance	-50		+50	ppm
	TCLK Duty Cycle	10		90	%
t1	Transmit Data Setup Time	40			ns
t2	Transmit Data Hold Time	40			ns
	Delay time of THZ low to driver high impedance			10	us
	Delay time of TCLK low to driver high impedance		75		U.I.
Receive path					
	Clock recovery capture range [1]		± 80		ppm
	RCLK duty cycle [2]	40	50	60	%
t4	RCLK pulse width [2]	457	488	519	ns
t5	RCLK pulse width low time	203	244	285	ns
t6	RCLK pulse width high time	203	244	285	ns
	Rise/fall time [3]			20	ns
t7	Receive Data Setup Time	200	244		ns
t8	Receive Data Hold Time	200	244		ns

1.Relative to nominal frequency, MCLK= ± 100 ppm

2.RCLK duty cycle widths will vary depending on extent of received pulse jitter displacement. Maximum and minimum RCLK duty cycles are for worst case jitter conditions (0.2UI displacement for E1 per ITU G.823).

3.For all digital outputs. C load = 15pF

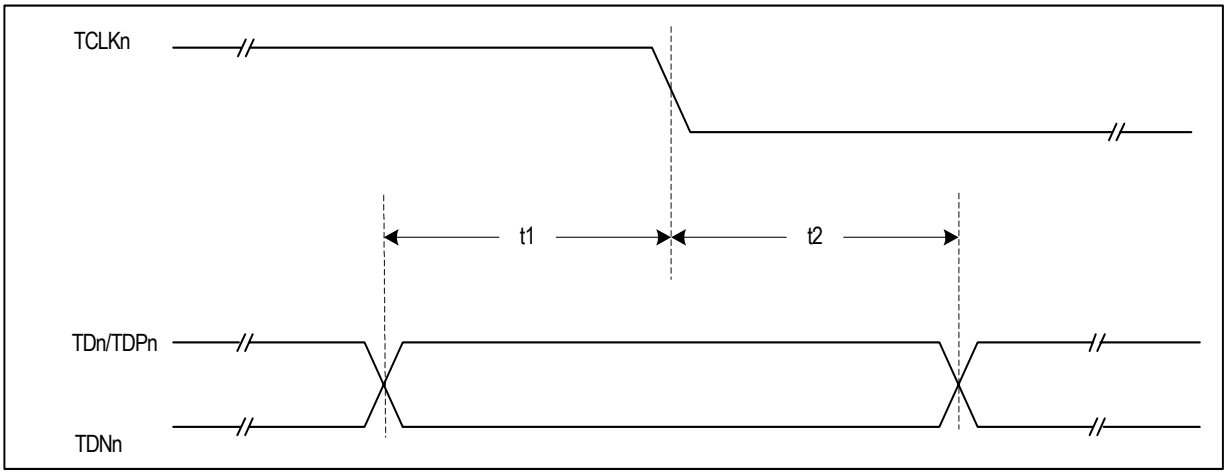


Figure-21 Transmit System Interface Timing

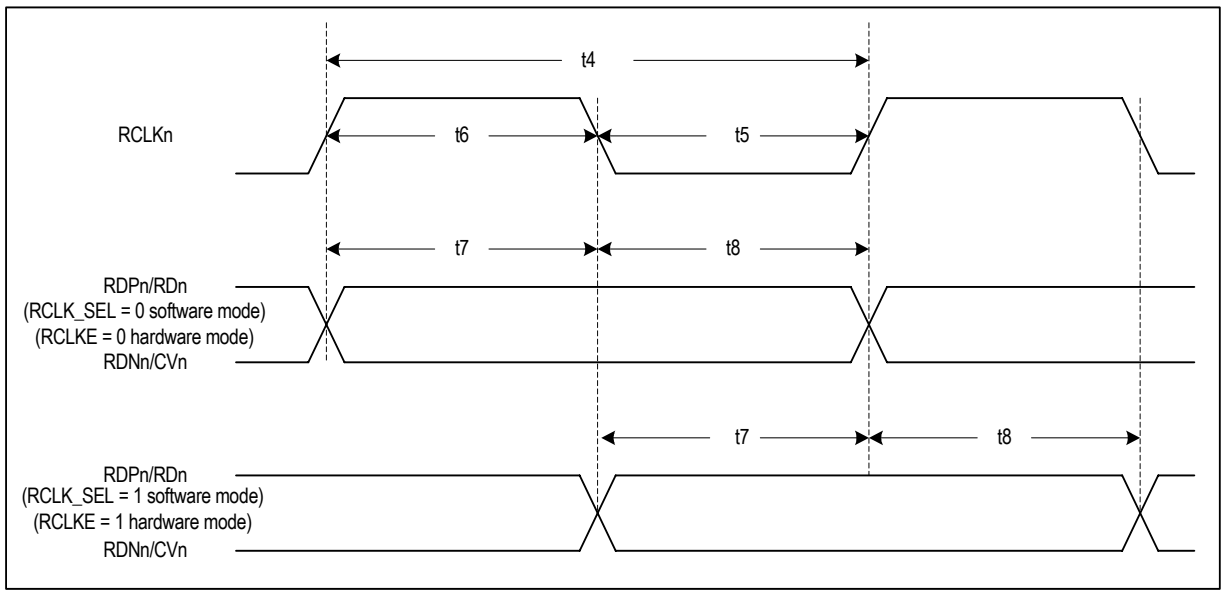


Figure-22 Receive System Interface Timing

Table-52 Jitter Tolerance

Jitter Tolerance	Min	Typ	Max	Unit	Standard
1 Hz	37			U.I.	G.823
20 Hz – 2.4 KHz	1.5			U.I.	Cable attenuation is 6dB
18 KHz – 100 KHz	0.2			U.I.	

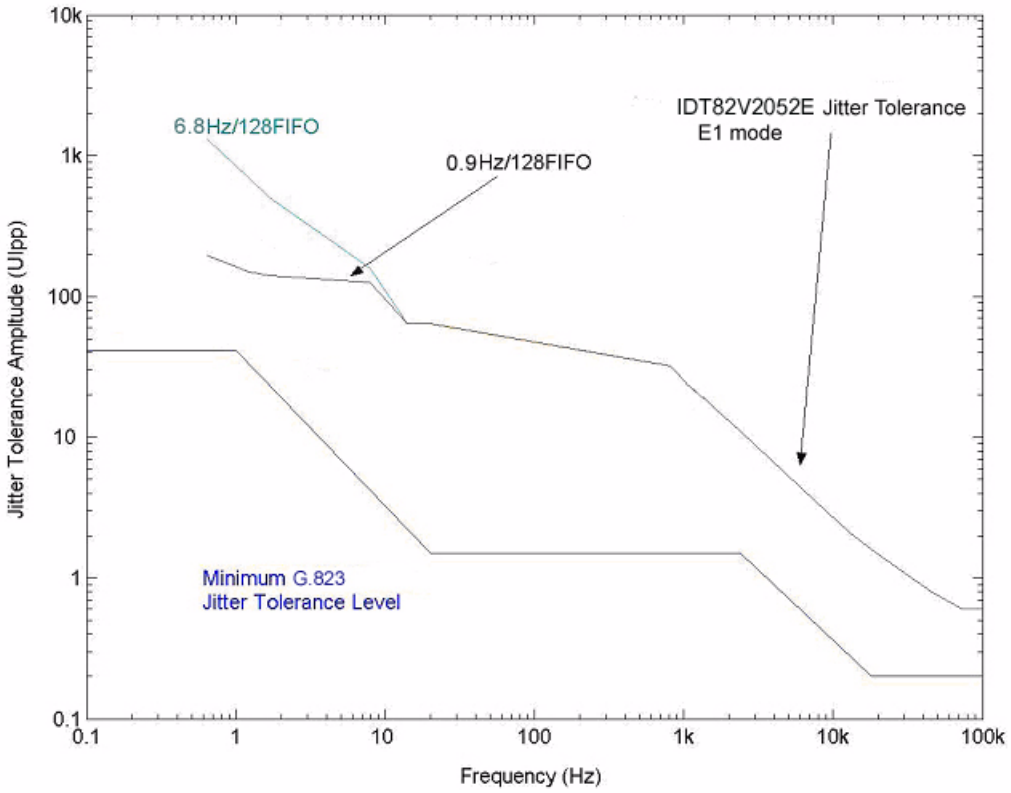


Figure-23 E1 Jitter Tolerance Performance

Table-53 Jitter Attenuator Characteristics

Parameter		Min	Typ	Max	Unit
Jitter Transfer Function Corner (-3dB) Frequency					
	32/64/128 bits FIFO JABW = 0: JABW = 1:		 6.8 0.9		 Hz Hz
Jitter Attenuator					
(G.736) @ 3 Hz @ 40 Hz @ 400 Hz @ 100 kHz		 -0.5 -0.5 +19.5 +19.5			 dB
Jitter Attenuator Latency Delay					
32 bits FIFO: 64 bits FIFO: 128 bits FIFO:			16 32 64		U.I. U.I. U.I.
Input jitter tolerance before FIFO overflow or underflow 32 bits FIFO: 64 bits FIFO: 128 bits FIFO:			 28 58 120		 U.I. U.I. U.I.

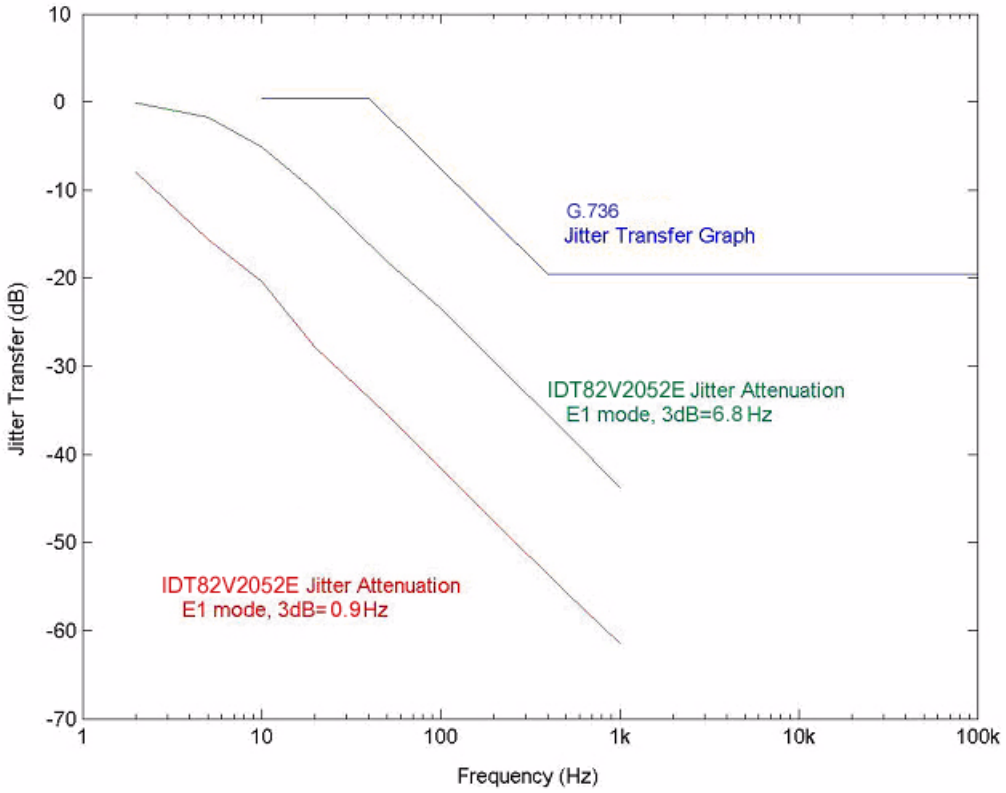


Figure-24 E1 Jitter Transfer Performance

Table-54 JTAG Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t1	TCK Period	100			ns
t2	TMS to TCK setup Time TDI to TCK Setup Time	25			ns
t3	TCK to TMS Hold Time TCK to TDI Hold Time	25			ns
t4	TCK to TDO Delay Time			50	ns

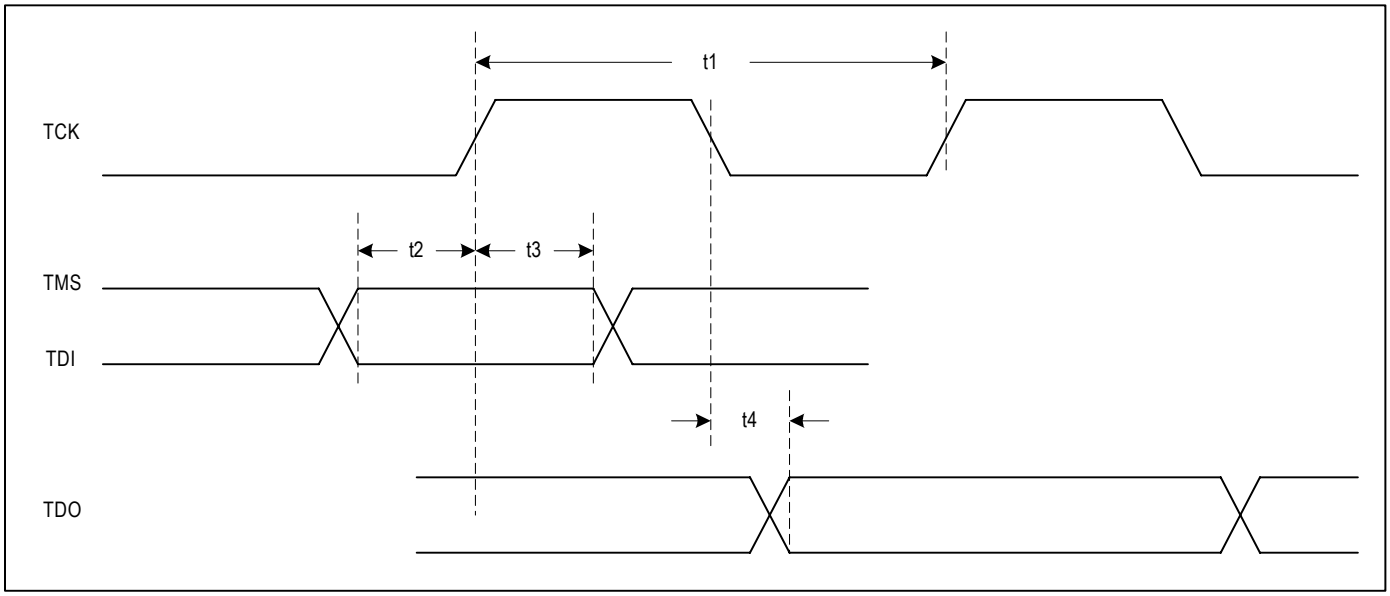


Figure-25 JTAG Interface Timing

8 MICROCONTROLLER INTERFACE TIMING CHARACTERISTICS

8.1 SERIAL INTERFACE TIMING

Table-55 Serial Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
t1	SCLK High Time	100			ns	
t2	SCLK Low Time	100			ns	
t3	Active $\overline{CS}$ to SCLK Setup Time	5			ns	
t4	Last SCLK Hold Time to Inactive $\overline{CS}$ Time	41			ns	
t5	$\overline{CS}$ Idle Time	41			ns	
t6	SDI to SCLK Setup Time	0			ns	
t7	SCLK to SDI Hold Time	82			ns	
t10	SCLK to SDO Valid Delay Time			95	ns	
t11	Inactive $\overline{CS}$ to SDO High Impedance Hold Time			90	ns	

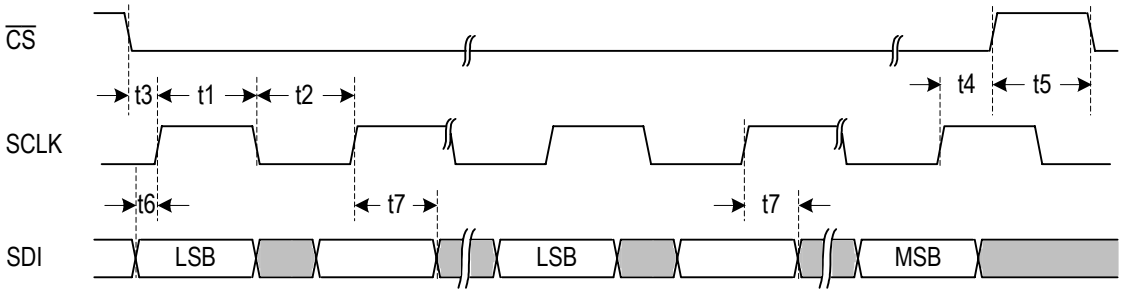


Figure-26 Serial Interface Write Timing

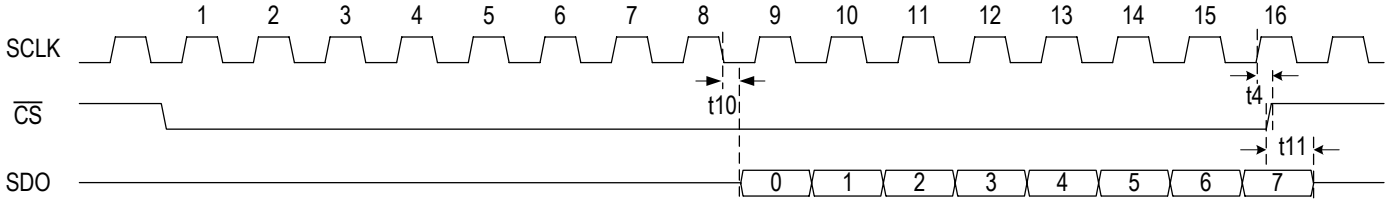


Figure-27 Serial Interface Read Timing with SCLKE=1

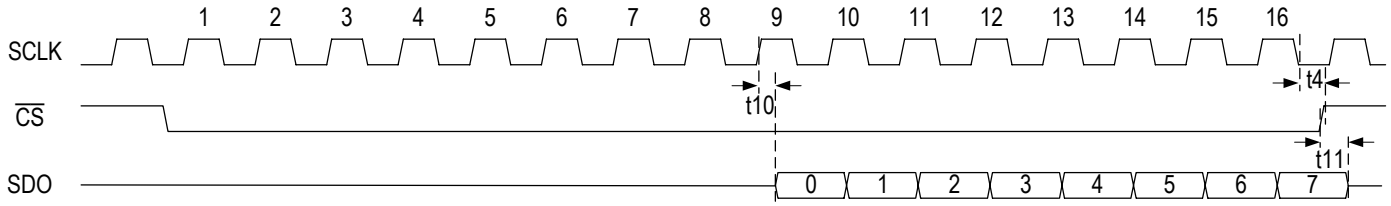


Figure-28 Serial Interface Read Timing with SCLKE=0

8.2 PARALLEL INTERFACE TIMING

Table-56 Non-Multiplexed Motorola Read Timing Characteristics

Symbol	Parameter	Min	Max	Unit
tRC	Read Cycle Time	190		ns
tDW	Valid $\overline{DS}$ Width	180		ns
tRWV	Delay from $\overline{DS}$ to Valid Read Signal		15	ns
tRWH	R/$\overline{W}$ to $\overline{DS}$ Hold Time	65		ns
tAV	Delay from $\overline{DS}$ to Valid Address		15	ns
tADH	Address to $\overline{DS}$ Hold Time	65		ns
tPRD	$\overline{DS}$ to Valid Read Data Propagation Delay		175	ns
tDAZ	Delay from $\overline{DS}$ inactive to data bus High Impedance	5	20	ns
tRecovery	Recovery Time from Read Cycle	5		ns

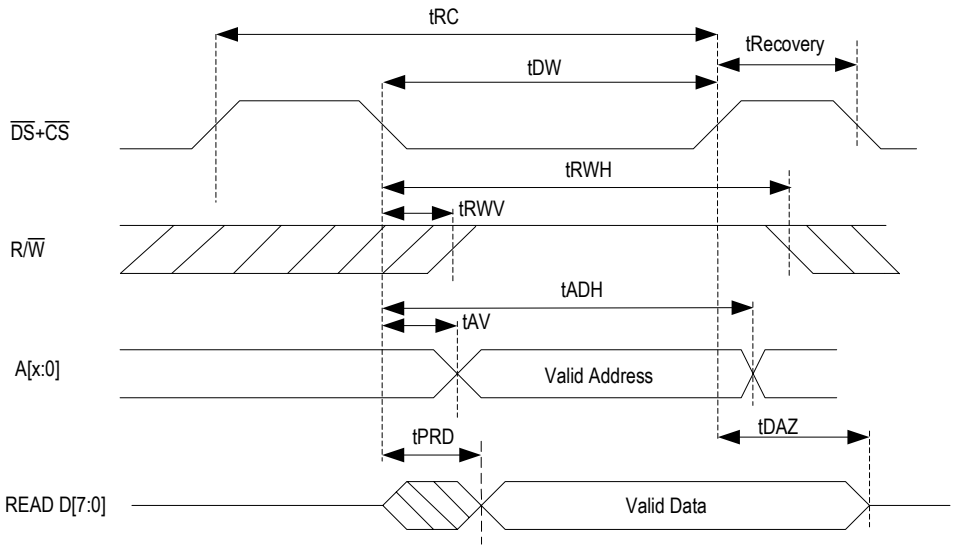


Figure-29 Non-Multiplexed Motorola Read Timing

Table-57 Non-Multiplexed Motorola Write Timing Characteristics

Symbol	Parameter	Min	Max	Unit
tWC	Write Cycle Time	120		ns
tDW	Valid $\overline{DS}$ Width	100		ns
tRWV	Delay from $\overline{DS}$ to Valid Write Signal		15	ns
tRWH	R/$\overline{W}$ to $\overline{DS}$ Hold Time	65		ns
tAV	Delay from $\overline{DS}$ to Valid Address		15	ns
tAH	Address to $\overline{DS}$ Hold Time	65		ns
tDV	Delay from $\overline{DS}$ to Valid Write Data		15	ns
tDHW	Write Data to $\overline{DS}$ Hold Time	65		ns
tRecovery	Recovery Time from Write Cycle	5		ns

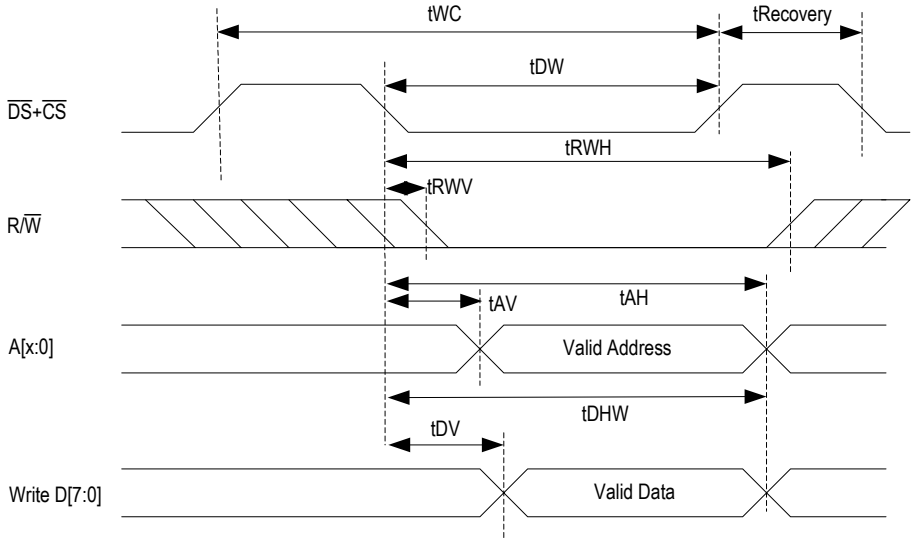
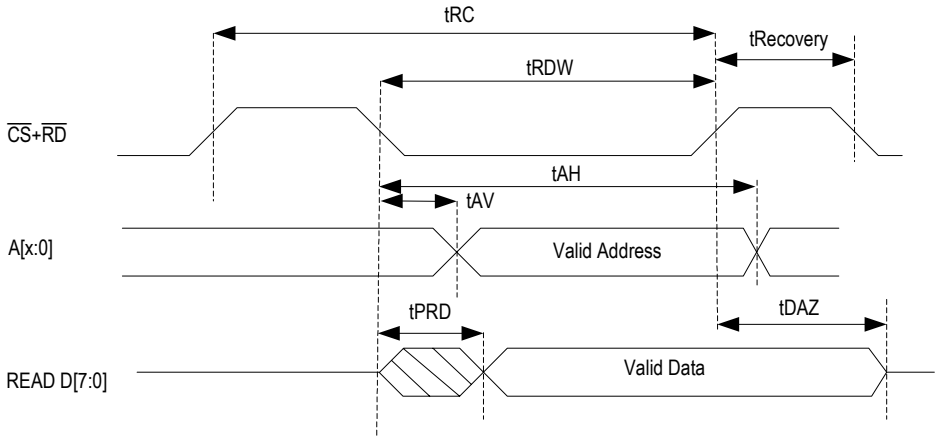


Figure-30 Non-Multiplexed Motorola Write Timing

Table-58 Non-Multiplexed Intel Read Timing Characteristics

Symbol	Parameter	Min	Max	Unit
tRC	Read Cycle Time	190		ns
tRDW	Valid $\overline{RD}$ Width	180		ns
tAV	Delay from $\overline{RD}$ to Valid Address		15	ns
tAH	Address to $\overline{RD}$ Hold Time	65		ns
tPRD	$\overline{RD}$ to Valid Read Data Propagation Delay		175	ns
tDAZ	Delay from $\overline{RD}$ inactive to data bus High Impedance	5	20	ns
tRecovery	Recovery Time from Read Cycle	5		ns

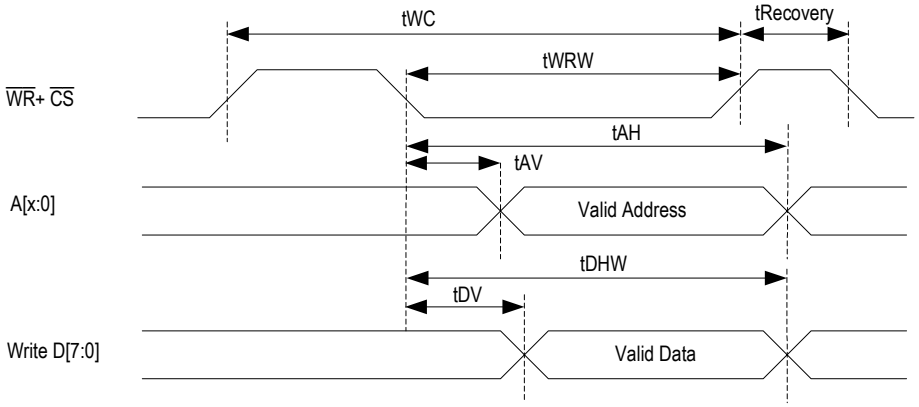


Note: $\overline{WR}$ should be tied to high

Figure-31 Non-Multiplexed Intel Read Timing

Table-59 Non-Multiplexed Intel Write Timing Characteristics

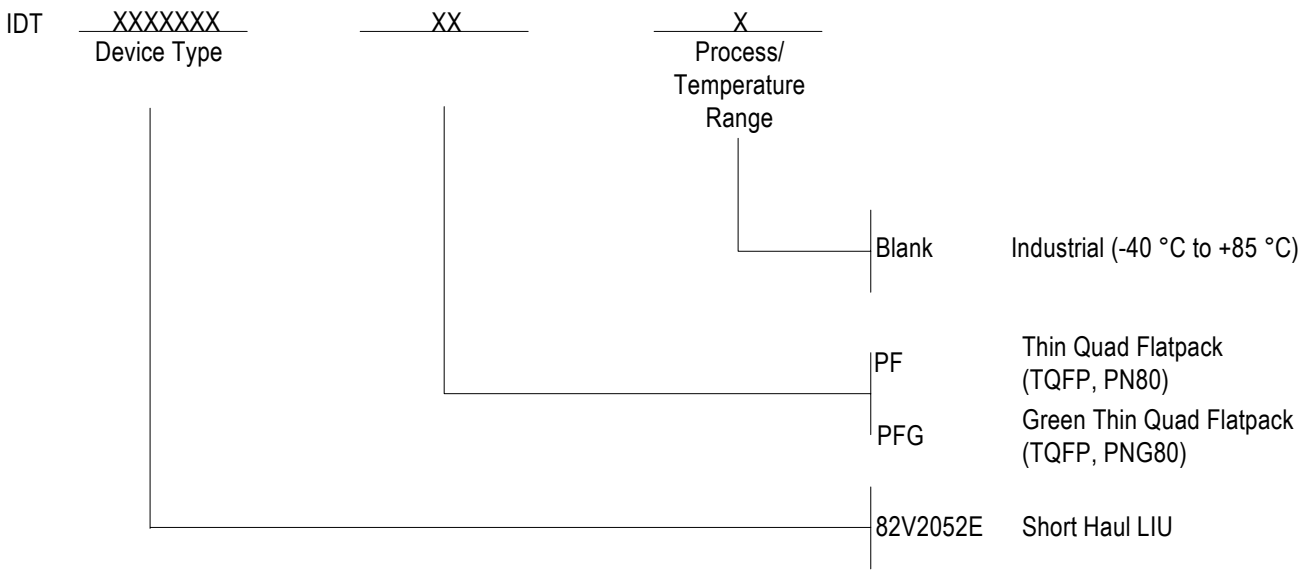
Symbol	Parameter	Min	Max	Unit
tWC	Write Cycle Time	120		ns
tWRW	Valid $\overline{WR}$ Width	100		ns
tAV	Delay from $\overline{WR}$ to Valid Address		15	ns
tAH	Address to $\overline{WR}$ Hold Time	65		ns
tDV	Delay from $\overline{WR}$ to Valid Write Data		15	ns
tDHW	Write Data to $\overline{WR}$ Hold Time	65		ns
tRecovery	Recovery Time from Write Cycle	5		ns



Note: $\overline{RD}$ should be tied to high

Figure-32 Non-Multiplexed Intel Write Timing

ORDERING INFORMATION



DATASHEET DOCUMENT HISTORY

12/12/2005 pgs. 1, 15, 21, 27, 35, 36, 43, 59, 70

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