HIGHLIGHTS

- Synchronization Management Unit (SMU) provides tools to manage physical layer and packet based synchronous clocks for IEEE 1588 / PTP Telecom Profile applications
- Supports independent IEEE 1588 and Synchronous Ethernet (SyncE) timing paths
- Combo mode provides SyncE physical layer frequency support for IEEE 1588 Telecom Boundary Clock (T-BC) and Telecom Time Slave Clocks (T-TSC) per G.8273.2
- Digital PLL 1 (DPLL1) and DPLL 2 can be configured as Digitally Controlled Oscillators (DCOs) for PTP clock synthesis
- DCO frequency resolution is [(77760 / 1638400) * 2^-48] or ~1.686305041e-10 ppm
- DPLL1 and DPLL2 generate G.8262 compliant SyncE clocks
- Two independent Time of Day (ToD) counters/time accumulators, one associated with each of DPLL1 and DPLL2, can be used to track differences between the two time domains and to time-stamp external events
- DPLL3 performs rate conversions to frequency synchronization interfaces or for other general purpose timing applications
- APLL generates clocks with jitter < 1 ps RMS (12 kHz to 20 MHz) for: 1000BASE-T and 1000BASE-X
- Fractional-N input dividers support a wide range of reference frequencies
- Locks to 1 Pulse Per Second (PPS) references
- It can be configured from an external EEPROM after reset

FEATURES

- Differential reference inputs (IN1 to IN4) accept clock frequencies between 1 PPS and 650 MHz
- Single ended inputs (IN5 to IN6) accept reference clock frequencies between 1 PPS and 162.5 MHz
- Loss of Signal (LOS) pins (LOS0 to LOS3) can be assigned to any clock reference input
- Reference monitors qualify/disqualify references depending on activity, frequency and LOS pins
- Automatic reference selection state machines select the active reference for each DPLL based on the reference monitors, priority tables, revertive and non-revertive settings and other programmable settings
- Fractional-N input dividers enable the DPLLs to lock to a wide range of reference clock frequencies including: 10/100/1000 Ethernet, 10G Ethernet, OTN, SONET/SDH, PDH, TDM, GSM, CPRI and GNSS frequencies
- Any reference input (IN1 to IN6) can be designated as external sync pulse inputs (1 PPS, 2 kHz, 4 kHz or 8 kHz) associated with a selectable reference clock input
- FRSYNC_8K_1PPS and MFRSYNC_2K_1PPS output sync pulses that are aligned with the selected external input sync pulse input and frequency locked to the associated reference clock input
- DPLL1 and DPLL2 can be configured with bandwidths between 0.09 mHz and 567 Hz
- DPLL1 and DPLL2 lock to input references with frequencies between 1 PPS and 650 MHz
- DPLL3 locks to input references with frequencies between 8 kHz and 650 MHz
- DPLL1 and DPLL2 comply with ITU-T G.8262 for Synchronous Ethernet Equipment Clock (EEC), and G.813 for Synchronous Equipment Clock (SEC); and Telcordia GR-253-CORE for Stratum 3 and SONET Minimum Clock (SMC)
- DPLL1 and DPLL2 generate clocks with PDH, TDM, GSM, CPRI/OBSAI, 10/100/1000 Ethernet and GNSS frequencies; these clocks are directly available on OUT1 and OUT5
- DPLL3 generates N x 8 kHz clocks up to 100 MHz that are output on OUT6 and OUT7
- DPLL1 and DPLL2 can be configured as DCOs to synthesize IEEE 1588 clocks
- APLL can be connected to DPLL1 or DPLL2
- APLL generates 10/100/1000 Ethernet, 10G Ethernet, or SONET/SDH frequencies
- Any of eight common TCXO/OCXO frequencies can be used for the System Clock: 10 MHz, 12.8 MHz, 13 MHz, 19.44 MHz, 20 MHz, 24.576 MHz, 25 MHz or 30.72 MHz
- The I2C slave, SPI or the UART interface can be used by a host processor to access the control and status registers
- The I2C master interface can automatically load a device configuration from an external EEPROM after reset
- Differential outputs OUT3 and OUT4 output clocks with frequencies between 1 PPS and 650 MHz
- Single ended outputs OUT1, OUT2 and OUT5 output clocks with frequencies between 1 PPS and 125 MHz
- DPLL1 and DPLL2 support independent programmable delays for each of IN1 to IN6; the delay for each input is programmable in steps of 0.61 ns with a range of ~±78 ns
- The input to output phase delay of DPLL1 and DPLL2 is programmable in steps of 0.0745 ps with a total range of ±20 μs
- The clock phase of each of the output dividers for OUT1 (from APLL) to OUT4 is individually programmable in steps of ~200 ps with a total range of +/-180°
- 1149.1 JTAG Boundary Scan
- 72-pin QFN green package

APPLICATIONS

- Access routers, edge routers, core routers
- Carrier Ethernet switches
- Multi-service access platforms
- Optical network terminal (ONT)
- Distribution point Unit (DPU)
- PON OLT
- LTE eNodeB
- IEEE 1588 / PTP Telecom Profile clock synthesizer
- ITU-T G.8273.2 Telecom Time Slave Clock (T-TSC)
- ITU-T G.8264 Synchronous Equipment Timing Source (SETS)
- ITU-T G.8263 Packet-based Equipment Clock (PEC)
- ITU-T G.8262 Synchronous Ethernet Equipment Clock (EEC)
- ITU-T G.813 Synchronous Equipment Clock (SEC)
- Telcordia GR-253-CORE Stratum 3 Clock (S3) and SONET Minimum Clock (SMC)

DESCRIPTION

The 82P33813 Synchronization Management Unit (SMU) provides tools to manage timing references, clock sources and timing paths for IEEE 1588 / Precision Time Protocol (PTP) and Synchronous Ethernet (SyncE) based clocks. The device supports up to three independent timing paths that control: PTP clock synthesis; SyncE clock generation; and general purpose frequency translation. The device supports physical layer timing with Digital PLLs (DPLLs) and it supports packet based timing with Digitally Controlled Oscillators (DCOs). Input-to- input, input-to-output and output-to-output phase skew can all be precisely managed. The device outputs low-jitter clocks that can directly synchronize lower-rate Ethernet interfaces; as well as CPRI/OBSAI, SONET/SDH and PDH interfaces and IEEE 1588 Time Stamp Units (TSUs).

The 82P33813 accepts four differential reference inputs and two single ended reference inputs that can operate at common GNSS, Ethernet, SONET/SDH and PDH frequencies that range in frequency from 1 Pulse Per Second (PPS) to 650 MHz. The references are continually monitored for loss of signal and for frequency offset per user programmed thresholds. All of the references are available to all three DPLLs. The active reference for each DPLL is determined by forced selection or by automatic selection based on user programmed priorities and locking allowances and based on the reference monitors and LOS inputs.

The 82P33813 can accept a clock reference and an associated phase locked sync signal as a pair. DPLL1 or DPLL2 can lock to the clock reference and align the frame sync and multi-frame sync outputs with the paired sync input. The device allows any of the differential or single ended reference inputs to be configured as sync inputs that can be associated with any of the other differential or single ended reference inputs. The input sync signals can have a frequency of 1 PPS, 2 kHz, 4 kHz or 8 kHz. This feature enables DPLL1 or DPLL2 to phase align its frame sync and multi-frame sync outputs with a sync input without the need use a low bandwidth setting to lock directly to the sync input.

DPLL1 and DPLL2 support four primary operating modes: Free-Run, Locked, Holdover and DCO. In Free-Run mode the DPLLs synthesize clocks based on the system clock alone. In Locked mode the DPLLs filter reference clock jitter with the selected bandwidth. In Locked mode, the long-term output frequency accuracy is the same as the long term frequency accuracy of the selected input reference. In Holdover mode, the DPLL uses frequency data acquired while in Locked mode to generate accurate frequencies when input references are not available. In DCO mode the DPLL control loop is opened and the DCO can be controlled by a PTP clock recovery servo running on an external processor to synthesize PTP clocks.

The 82P33813 requires a system clock for its reference monitors and other digital circuitry. The frequency accuracy of the system clock determines the frequency accuracy of the DPLLs in Free-Run mode. The frequency stability of the system clock determines the frequency stability of the DPLLs in Free-Run mode and in Holdover mode; and it affects the wander generation of the DPLLs in Locked and DCO modes.

When used with a suitable system clock, DPLL1 and DPLL2 meet the frequency accuracy, pull-in, hold-in, pull-out, noise generation, noise tolerance, transient response, and holdover performance requirements of the following applications: ITU-T G.8262/G.813 EEC/SEC options 1 and 2, ITU-T G.8263, ITU-T G.8273.2, Telcordia GR-1244 Stratum 3 (S3), Telcordia GR-253-CORE Stratum 3 (S3) and SONET Minimum Clock (SMC).

DPLL1 and DPLL2 can be configured with a range of selectable filtering bandwidths from 0.09 mHz to 567 Hz. The 17 mHz bandwidth can be used to lock the DPLL directly to a 1 PPS reference. The 69 mHz and the 92 mHz bandwidths can be used for G.8273.2. The 92 mHz bandwidth can be used for G.8262/G.813 Option 2 or Telcordia GR-253-CORE S3 or SMC applications. The bandwidths in the range 1.1 Hz to 8.9 Hz can be used for G.8262/G.813 Option 1 applications. Bandwidths above 10 Hz can be used in jitter attenuation and rate conversion applications.

DPLL1 and DPLL2 are each connected to Time of Day (ToD) counters or time accumulators; these ToD counters/time accumulators can be used to track differences between the two time domains and to time-stamp external events by using reference inputs as triggers.

DPLL3 supports three primary operation modes: Free-Run, Locked and Holdover. DPLL3 is a wideband (BW > 25Hz) frequency translator that can be used, for example, to convert a recovered line clock to a 1.544 MHz or 2.048 MHz synchronization interface clock.

In Telecom Boundary Clock (T-BC) and Telecom Time Slave Clock (T-TSC) applications per ITU-T G.8275.2, DPLL1 and DPLL2 are both used; one DPLL is configured as a DCO to synthesize PTP clocks and the other DPLL is configured as an EEC/SEC to generate physical layer clocks. Combo mode provides physical layer frequency support from the EEC/SEC to the PTP clock.

In Synchronous Equipment Timing Source (SETS) applications per ITU-T G.8264, DPLL1 or DPLL2 can be configured as an EEC/SEC to output clocks for the T0 reference point and DPLL3 can be used to output clocks for the T4 reference point.

Clocks generated by DPLL1 or DPLL2 can be passed through the APLL which are LC based jitter attenuating Analog PLL (APLL). The output clocks generated by the APLL are suitable for serial GbE and lower rate interfaces.

All 82P33813 control and status registers are accessed through an I2C slave, SPI or the UART microprocessor interface. For configuring the DPLLs and APLL, the I2C master interface can automatically load a configuration from an external EEPROM after reset.
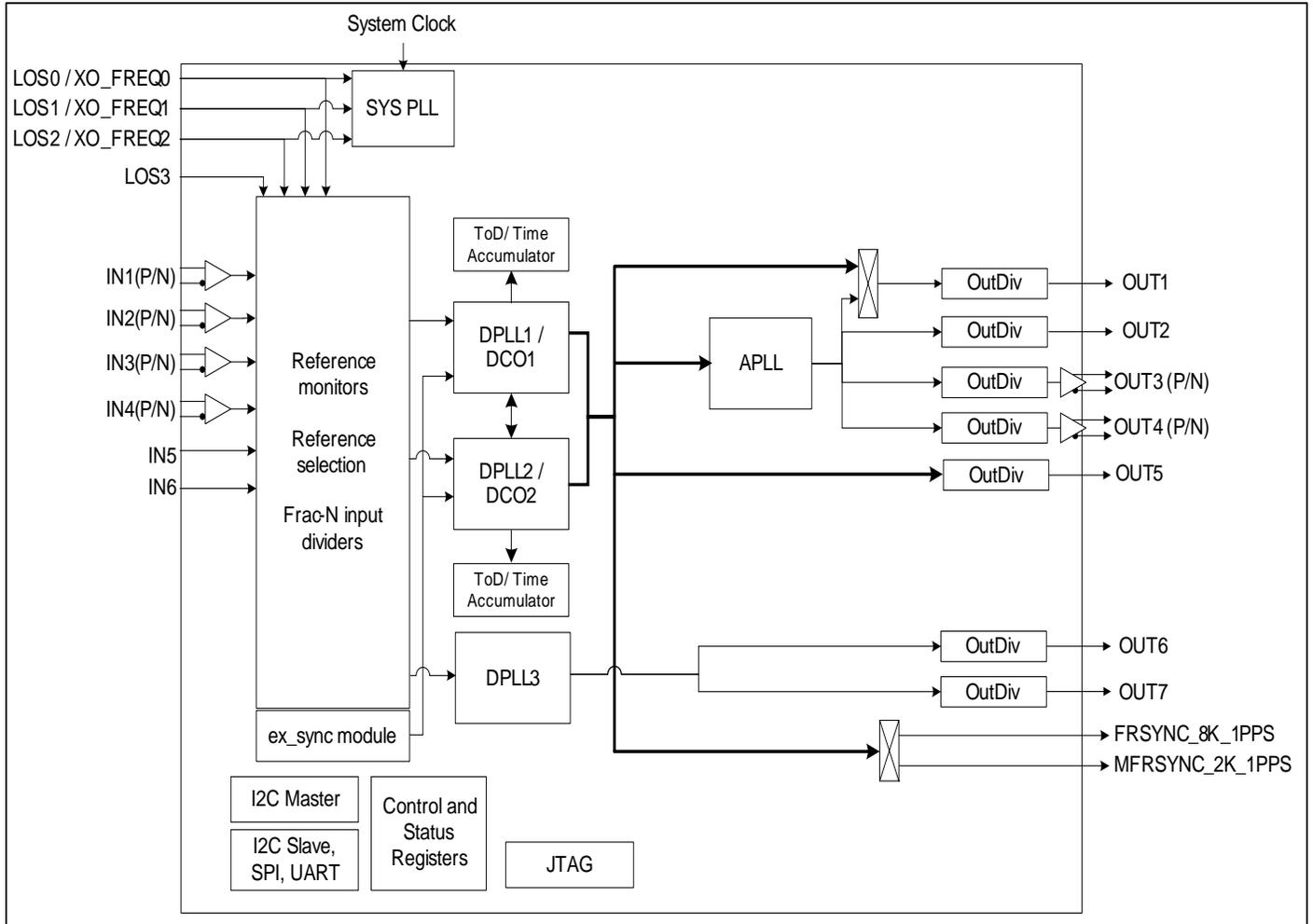
FUNCTIONAL BLOCK DIAGRAM

Figure 1. Functional Block Diagram

CONTENTS

1   PIN ASSIGNMENT

Figure 2. Pin Assignment (Top View)

2 PIN DESCRIPTION

Table 1: Pin Description

Pin No.	Name	I/O	Type	Description
				Global Control Signal
6	OSCI	I	CMOS	OSCI: Crystal Oscillator System Clock A clock provided by a crystal oscillator is input on this pin. It is the system clock for the device. The oscillator frequency is selected via pins XO_FREQ0 ~ XO_FREQ2
58	MS/SL	I pull-up	CMOS	MS/SL: Master / Slave Selection This pin, together with the MS_SL_CTRL bit, controls whether the device is configured as the Master or as the Slave. The signal level on this pin is reflected by the MASTER_SLAVE bit. MS_SL = 0: Slave MS_SL = 1: Master (default with internal pull-up)
59	SONET/SDH/ LOS3	I pull-down	CMOS	SONET/SDH: SONET / SDH Frequency Selection During reset, this pin determines the default value of the IN_SONET_SDH bit: High: The default value of the IN_SONET_SDH bit is '1' (SONET); Low: The default value of the IN_SONET_SDH bit is '0' (SDH). After reset, the value on this pin takes no effect. LOS3- This pin is used to disqualify input clocks. See input clocks section for more details.
52	RSTB	I pull-up	CMOS	RSTB: Reset Refer to section 2.2 reset operation for details.
7 8 9	XO_FREQ0/ LOS0 XO_FREQ1/ LOS1 XO_FREQ2/ LOS2	I pull-down	CMOS	XO_FREQ0 ~ XO_FREQ2: These pins set the oscillator frequency. XO_FREQ[2:0] Oscillator Frequency (MHz) 000 10.000 001 12.800 010 13.000 011 19.440 100 20.000 101 24.576 110 25.000 111 30.720 LOS0 ~ LOS2 - These pins are used to disqualify input clocks. See input clocks section for more details. After reset, this pin takes on the operation of LOS0-LOS2
				Input Clock and Frame Synchronization Input Signal
31 32	IN1_POS IN1_NEG	I	PECL/LVDS	IN1_POS / IN1_NEG: Positive / Negative Input Clock 1 A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
33 34	IN2_POS IN2_NEG	I	PECL/LVDS	IN2_POS / IN2_NEG: Positive / Negative Input Clock 1 A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
35 36	IN3_POS IN3_NEG	I	PECL/LVDS	IN3_POS / IN3_NEG: Positive / Negative Input Clock 3 A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
38 39	IN4_POS IN4_NEG	I	PECL/LVDS	IN4_POS / IN4_NEG: Positive / Negative Input Clock 4 A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
37	IN5	I pull-down	CMOS	IN5: Input Clock 5 A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.

Table 1: Pin Description (Continued)

Pin No.	Name	I/O	Type	Description
41	IN6	I pull-down	CMOS	IN6: Input Clock 6 A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
Output Frame Synchronization Signal				
43	FRSYNC _8K_1PPS	O	CMOS	FRSYNC_8K_1PPS: 8 kHz Frame Sync Output An 8 kHz signal or a 1PPS sync signal is output on this pin.
44	MFRSYNC _2K_1PPS	O	CMOS	MFRSYNC_2K_1PPS: 2 kHz Multiframe Sync Output A 2 kHz signal or a 1PPS sync signal is output on this pin.
Output Clock				
30 28	OUT1 OUT2	O	CMOS	OUT1 ~ OUT2: Output Clock 1 ~ 2
25 26	OUT3_POS OUT3_NEG	O	PECL/LVDS	OUT3_POS / OUT3_NEG: Positive / Negative Output Clock 3 This output is set to LVDS by default.
21 22	OUT4_POS OUT4_NEG	O	PECL/LVDS	OUT4_POS / OUT4_NEG: Positive / Negative Output Clock 4 This output is set to LVDS by default.
63	OUT5	O	CMOS	OUT5: Output Clock 5
61 60	OUT6 OUT7	O	CMOS	OUT6 ~ OUT7: Output Clock 6 ~ 7
Miscellaneous				
13	VC	O	Analog	VC: APLL VC Output An external RC filter (a resistor in series with a capacitor to ground, and another capacitor in parallel) should be connected to this pin.
Lock Signal				
55	DPLL_LOCK	O	CMOS	DPLL_LOCK This pin goes high when the DPLL is locked
Microprocessor Interface				
57	INT_REQ	O Tri-state	CMOS	INT_REQ: Interrupt Request This pin is used as an interrupt request.
46 45	MPU_MODE1/ I2CM_SCL MPU_MODE0/ I2CM_SDA	I/O pull-up	CMOS/ Open Drain	MPU_MODE[1:0]: Microprocessor Interface Mode Selection During reset, these pins determine the default value of the MPU_SEL_CNFG[1:0] bits as follows: 00: I2C mode 01: SPI mode 10: UART mode 11: I2C master (EEPROM) mode I2CM_SCL: Serial Clock Line In I2C master mode, the serial clock is output on this pin. I2CM_SDA: Serial Data Input for I2C Master Mode In I2C master mode, this pin is used as the for the serial data.
47	SDI/I2C_AD2/ UART_RX	I pull-down	CMOS	SDI: Serial Data Input In Serial mode, this pin is used as the serial data input. Address and data on this pin are serially clocked into the device on the rising edge of SCLK. I2C_AD2: Device Address Bit 2 In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface. UART_RX In UART mode, this pin is used as the receive data (UART Receive)

Table 1: Pin Description (Continued)

Pin No.	Name	I/O	Type	Description
48	CLKE/I2C_AD1	I pull-down	CMOS	CLKE: SCLK Active Edge Selection In Serial mode, this pin is an input, it selects the active edge of SCLK to update the SDO: High - The falling edge; Low - The rising edge. I2C_AD1: Device Address Bit 1 In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface.
49	CS/I2C_AD0	I pull-up	CMOS	CS: Chip Selection In Serial modes, this pin is an input.A transition from high to low must occur on this pin for each read or write operation and this pin should remain low until the operation is over. I2C_AD0: Device Address Bit 0 In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface.
50	SCLK/I2C_SCL	I pull-down	CMOS	SCLK: Shift Clock In Serial mode, a shift clock is input on this pin. Data on SDI is sampled by the device on the rising edge of SCLK. Data on SDO is updated on the active edge of SCLK. The active edge is determined by the CLKE. I2C_SCL: Serial Clock Line In I2C mode, the serial clock is input on this pin.
51	SDO/I2C_SDA/ UART_TX	I/O pull-up	CMOS/ Open Drain	SDO: Serial Data Output In Serial mode, this pin is used as the serial data output. Data on this pin is serially clocked out of the device on the active edge of SCLK. I2C_SDA: Serial Data Input/Output In I2C mode, this pin is used as the input/output for the serial data. UART_TX: In UART mode, this pin is used as the transmit data (UART Transmit)
JTAG (per IEEE 1149.1)				
14	TMS	I pull-up	CMOS	TMS: JTAG Test Mode Select The signal on this pin controls the JTAG test performance and is sampled on the rising edge of TCK.
15	TRSTB	I pull-up	CMOS	TRSTB: JTAG Test Reset (Active Low) A low signal on this pin resets the JTAG test port. This pin should be connected to ground when JTAG is not used.
16	TCK	I pull-down	CMOS	TCK: JTAG Test Clock The clock for the JTAG test is input on this pin. TDI and TMS are sampled on the rising edge of TCK and TDO is updated on the falling edge of TCK. If TCK is idle at a low level, all stored-state devices contained in the test logic will indefinitely retain their state.
17	TDI	I pull-up	CMOS	TDI: JTAG Test Data Input The test data are input on this pin. They are clocked into the device on the rising edge of TCK.
18	TDO	O tri-state	CMOS	TDO: JTAG Test Data Output The test data are output on this pin. They are clocked out of the device on the falling edge of TCK. TDO pin outputs a high impedance signal except during the process of data scanning.
Power & Ground				
2, 3, 4, 5, 10 11, 12	VDDA	Power	-	VDDA: Analog Core Power - +3.3V DC nominal
20, 24, 69, 72	VDDAO	Power		VDDAO: Analog Output Power - +3.3V DC nominal
27, 29, 64, 66	VDDDO	Power		VDDDO: Digital Output Power - +3.3V DC nominal

Table 1: Pin Description (Continued)

Pin No.	Name	I/O	Type	Description
40, 62	VDDD	Power		**VDDD**: Digital Core Power - +3.3V DC nominal
42, 53	VDDD_1_8	Power		**VDDD_1_8**: Digital Core Power - +1.8V DC nominal
19,23	VSSAO	Ground		**VSSAO**: Ground
73 (e_PAD)	VSS	Ground	-	**VSS**: Ground
Other				
1, 54, 56, 65, 67, 68, 70, 71	IC	-	-	**IC**: Internal Connection Internal Use. These pins must be left open for normal operation.

2.1 RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

2.1.1 INPUTS

Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Single-Ended Clock Inputs

For protection, unused single-ended clock inputs should be tied to ground.

Differential Clock Inputs

For applications not requiring the use of a differential input, both *_POS and *_NEG can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from _POS to ground.

2.1.2 OUTPUTS

Status Pins

For applications not requiring the use of a status pin, we recommend bringing out to a test point for debugging purposes.

Single-Ended Clock Outputs

All unused single-ended clock outputs can be left floating, or can be brought out to a test point for debugging purposes.

Differential Clock Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

2.2 RESET OPERATION

The device must be reset properly in order to ensure operations conform with specification.

To properly reset the device, the RSTB pin must be held at a low value for at least 50 usec. The device should be brought out of reset only at the time when power supplies are stabilized and the system clock is available on OSCi pin. The RSTB can be held low until this time, or pulsed low for at least 50us after this time.

The bootstrap pins (XO_FREQ[2:0], MPU_MODE[1:0], I2C_AD[2:0], MS/SL, SONET/SDH) need to be held at desired states for at least 2ms after de-assertion of RSTB pin to allow correct sampling. See Figure 3 for detail.

If loading from an EEPROM, the maximum time from RSTB de-assert to have stable clocks is 100ms. Note that if there is a bad EEPROM read sequence and the EEPROM loading is repeated once or twice (three times halts the device), then this time can be 2 or 3 times longer respectively. If not loading from EEPROM the maximum time from RSTB de-assert to have stable clocks is 10ms.

An on-board reset circuit or a commercially available voltage supervisory can be used to generate the reset signal. It is also feasible to use a standalone power-up RC reset circuit. When using a power-up RC reset circuit, careful consideration must be taken into account to fine tune the circuit properly based on each power supply's specification to ensure the power supply rise time is fast enough with respect to the RC time constant of the RC circuit.
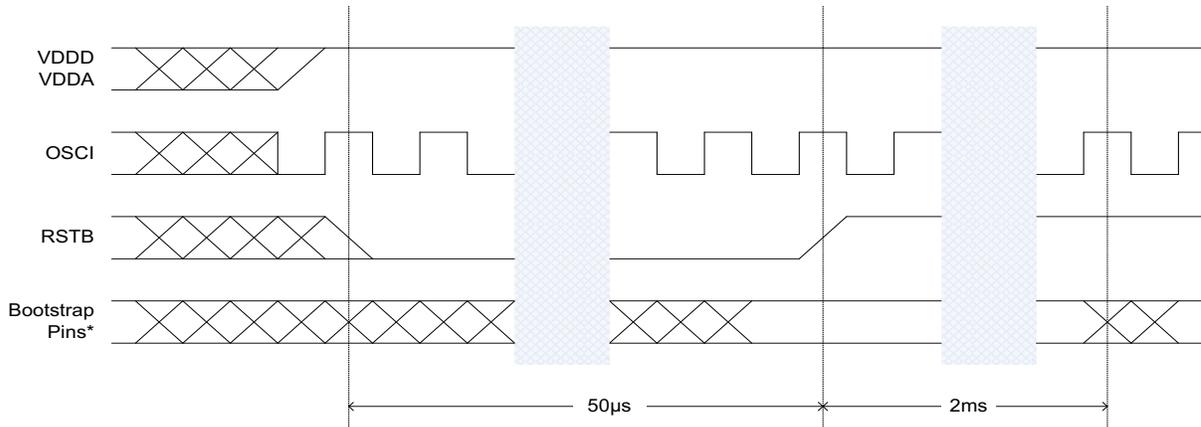
* Bootstrap pins are: XO_FREQ[2:0], MPU_MODE[1:0], I2C_AD[2:0], MS/SL, SONET/SDH

Figure 3. Reset timing diagram

2.3   MS/SL PIN USAGE

The MS/SL pin is used for timing card redundancy applications where there is a primary and secondary timing card in the system. For other applications, this pin should be left unconnected or connected to an external pull-up.

For more information, see AN-901, *How to Implement Master/Slave for SETS and SMU Devices on Timing Redundancy Designs.*

3 FUNCTIONAL DESCRIPTION

3.1 IEEE 1588 AND SYNCHRONOUS ETHERNET (SYNCE) SYSTEM ARCHITECTURES

ITU-T is working on key recommendations for the use of IEEE 1588 for Telecom. There are several recommendations that have been published for frequency applications, they are:

- ITU-T Recommendation G.8261, Timing and synchronization aspects in packet networks.
- ITU-T Recommendation G.8262, Timing characteristics of Synchronous Ethernet Equipment slave clock (EEC).
- ITU-T Recommendation G.8264, Distribution of timing through packet networks
- Recommendation ITU-T G.8261.1, Packet Delay Variation Network Limits applicable to Packet Based Methods (Frequency Synchronization).
- Recommendation ITU-T G.8263, Timing Characteristics of Packet based Equipment Clocks (PEC) and Packet based Service Clocks (PSC)
- ITU-T Recommendation G.8265), Architecture and requirements for packet based frequency delivery
- ITU-T Recommendation G.8265.1, Precision time protocol telecom profile for frequency sync
- ITU-T Recommendation G.8260, Definitions and terminology for synchronization in packet networks

For the phase and time applications ITU-T has consented the following recommendations:

- ITU-T Recommendation G.8271, Time and phase synchronization aspects of packet networks
- ITU-T Recommendation G.8272, Timing characteristics of Primary reference time clock
- ITU-T Recommendation G.8271.1, Network Limits for Time Synchronization in Packet Networks
- ITU-T Recommendation G.8273, Framework of phase and time clocks

- ITU-T Recommendation G.8273.2, Timing characteristics of telecom boundary clocks and telecom time slave clocks
- ITU-T Recommendation G.8275, Architecture and requirements for packet-based time and phase delivery
- ITU-T Recommendation G.8275.1, Precision time protocol telecom profile for phase/time synchronization with full timing support from the network

Another important ITU-T Recommendation that is used in synchronization networks is ITU-T Recommendation G.781, Synchronization Layer Functions.

82P33813 has a very flexible architecture to allow systems to support the current requirements defined by ITU-T. In addition to supporting the published ITU-T Recommendations, the device has the flexibility to support future ITU-T phase/time recommendations.

3.1.1 IEEE1588 AND SYNCE SINGLE BLADE ARCHITECTURE

Figure 4 shows the single blade architecture, note that only the blocks relevant to synchronization have been drawn. In this application all the synchronization functions are centralized in one card, for example in a pizza box type of system. In Figure 4, the timestamps are done at the Ethernet PHY, but there are solutions that deploys a host processor that integrates the time stamp unit. The host processor terminates the transport layer protocol and the IEEE 1588 protocol. The timestamps are processed (servo or clock recovery algorithm) by the host processor. Based on the clock recovery algorithm the host processor will control the 82P33813 internal DCO to generate clocks that are locked to an IEEE 1588 master in the network.

In the case of a slave node that has the frequency locked to synchronous Ethernet (SyncE), the 82P33813 has a combo mode that allows the frequency to be used from SyncE and the phase be controlled by IEEE 1588 (see section 3.3.2.3 Combo Mode on page 23 for more details on combo mode).
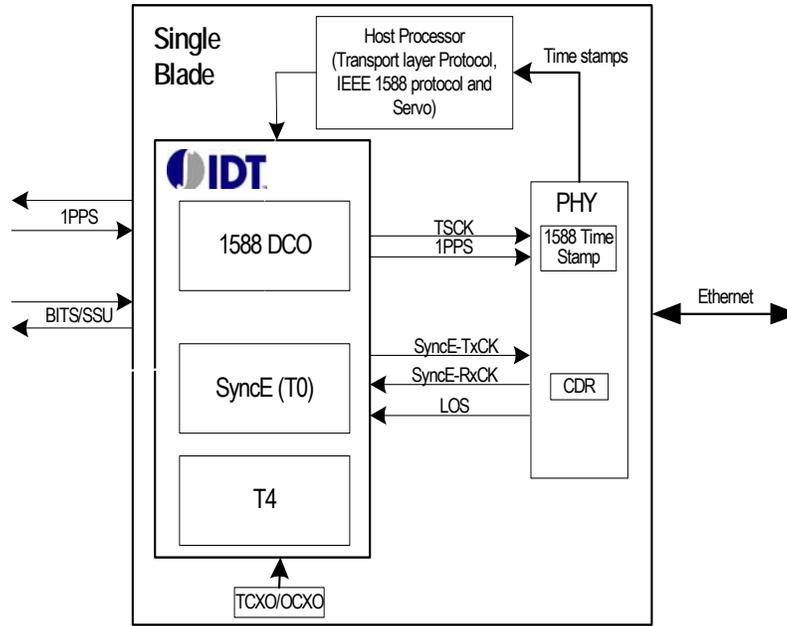
Figure 4. Single Blade Architecture

3.1.2 DISTRIBUTED ARCHITECTURE FOR T-BC AND T-TSC, IEEE 1588 IN THE TIMING CARD

Figure 5 shows a distributed architecture that can represent a Telecom Boundary clock (T-BC) or telecom time slave clocks (T-TSC) implementation where the IEEE 1588 is handled in the timing card. In this architecture IEEE 1588 protocol is terminated in the timing card. The local host processor will run the clock recovery algorithm (servo) and run the alternate Best Master Clock Algorithm (BMCA) according to ITU-T G.8275.1. The alternate BMCA determines which Telecom Grand Master (T-GM) to be used as the source of time. In Figure 5, one of the packet data port will be a slave port and the others will be master ports of the T-BC. The first revision of G.8275.1 assumes that the frequency is transported by synchronous Ethernet (SyncE) and the phase is controlled by IEEE 1588. G.8271.1 shows a model for Telecom Boundary Clock (T-BC) with SyncE assistance. 82P33813 has a combo mode that allows the implementation of the T-BC and T-TSC with SyncE assistance. It is very important to control the IEEE 1588 clocks independently of the SyncE clocks. It maybe also important to be able to suppress phase transients on the SyncE clocks to not affect the IEEE 1588 clocks. See Chapter 3.3.2.3 for mode details on the combo mode.

ITU-T G.8273.2 has two classes of T-BC and T-TSC clocks. Class A must meet 50ns of phase alignment inside an equipment. Class B must meet 20ns of phase alignment inside an equipment, this will allow an Operator to deploy longer chains of T-BCs. To be able to meet such tight requirements, it is very important to control the delays between the timing card and the line cards. 82P33813 has individual phase adjustments to allow very fine control of the phase of the clocks inside the equipment. See Chapter 3.3.7.1, Chapter 3.3.7.2, and Chapter 3.3.7.3 for details on the phase adjustment control modes.

The architecture depicted in Figure 5 can also be used for a phase and time application using G.8275.2 and frequency application using G.8265.1 (see Chapter 3.1.4.1). The key difference in this case is that the T-BC, T-TSC or a packet slave clock will experience Packet Delay Variation (PDV) due to the network that does not have IEEE 1588 full timing support (T-BC is not deployed in every node of the network). An algorithm to filter PDV must be implemented in this case.

Also for the architecture shown in Figure 5, there is an active timing card and a redundant timing card. This is done in equipment that are designed to have a redundant timing card in case of failure of the primary timing card. The redundant timing card mimics the output of the active timing card, so in case of failure the system will still provide proper synchronization.
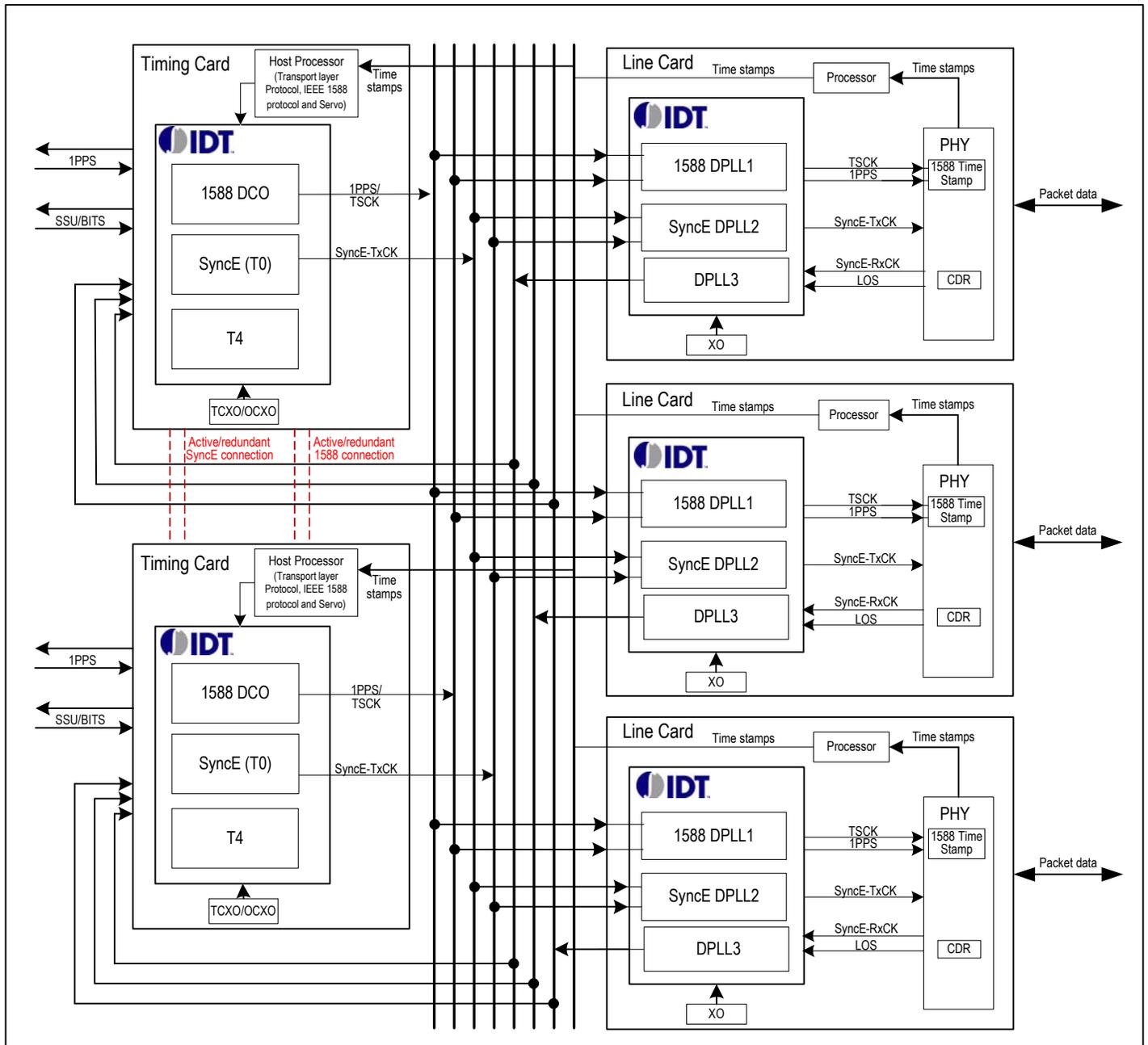
Figure 5. Distributed Architecture, IEEE 1588 in the Timing Card

3.1.3　T-BC AND T-TSC - IEEE 1588 IN THE LINE CARD

Figure 6 shows a distributed architecture that can represent a T-BC or a T-TSC implementation where the IEEE 1588 is handled in the line cards. In this architecture IEEE 1588 protocol is terminated in the line cards. The local host processor will run the clock recovery algorithm (servo) and run the alternate Best Master Clock Algorithm (BMCA) according to ITU-T G.8275.1. The alternate BMCA determines which Telecom Grand Master (T-GM) to be used as the source of time. In Figure 6, one of the packet data port will be a slave port and the others will be master ports of the T-BC.

The 82P33813 disciplined DCO mode is very important for this architecture as it allows the use of a simple crystal (e.g. 20ppm) at the line card, as the SyncE clock coming from the timing card will be used at the line card to implement the T-BC with SyncE assistance. Also in this architecture it is very important to control the IEEE 1588 clocks independently of the SyncE clocks. It is also important to be able to suppress phase transients on the SyncE clocks to not affect the IEEE 1588 clocks. See Chapter 3.3.2.2 for mode details on the disciplined DCO mode.

To be able to meet the ITU-T G.8273.2 tight requirements described in the previous architecture, it is very important to control the delays between the clocks from the line card that is behaving as the slave port of the T-BC with line cards that are behaving as master ports. 82P33813 has individual phase adjustments to allow very fine control of the phase of the clocks inside the equipment. See Chapter 3.3.7.3 for mode details on the phase adjustment control.

The architecture depicted in Figure 5 can also be used for a phase and time application using G.8275.2 and frequency application using G.8265.1 (see Chapter 3.1.4.2). The key difference in this case is that the T-BC, T-TSC or a packet slave clock will experience Packet Delay Variation (PDV) due to the network that does not support IEEE 1588. An algorithm to filter PDV must be implemented in this case.
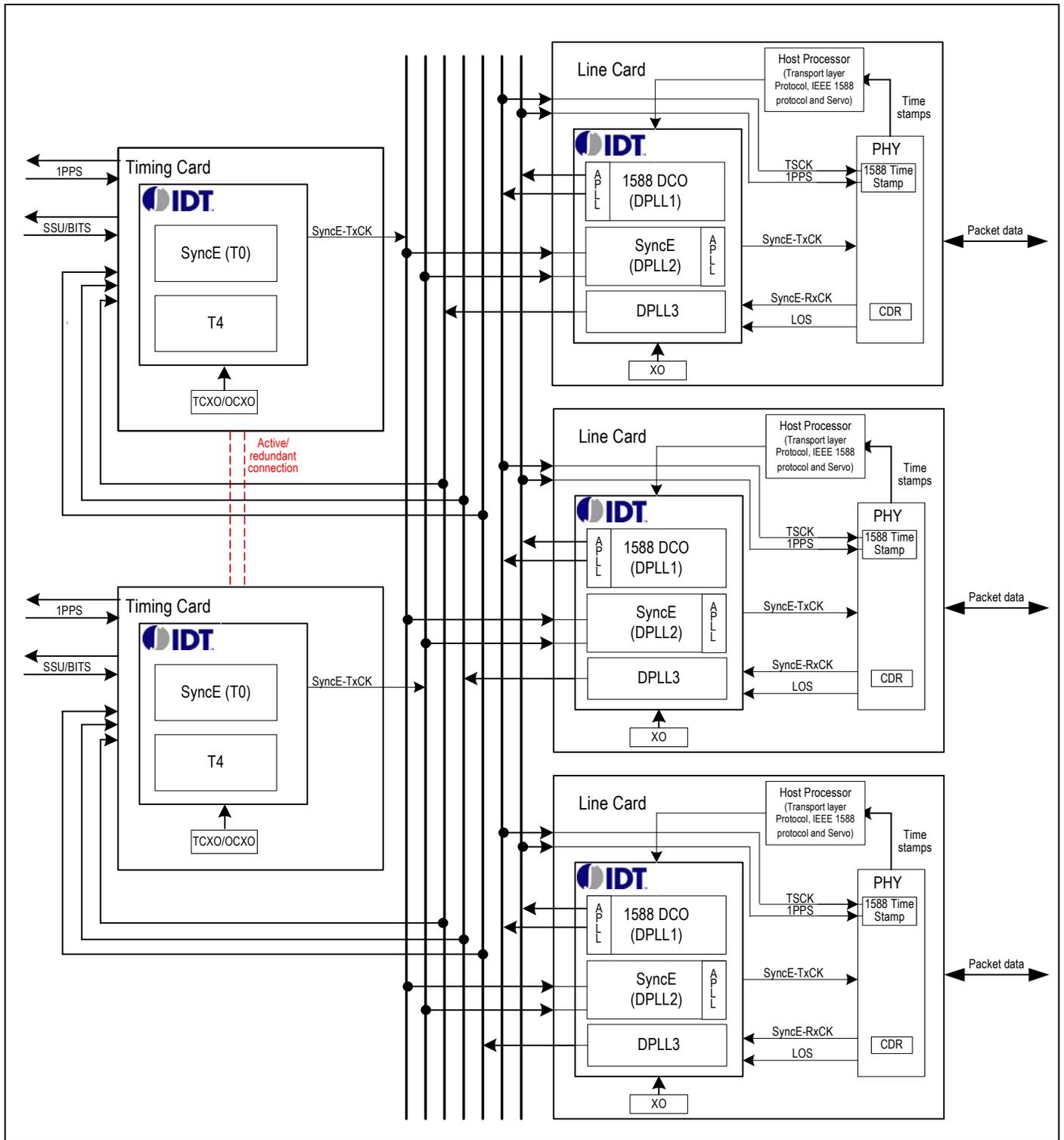
Figure 6. Distributed Architecture, IEEE 1588 in the Line Card

3.1.4 DISTRIBUTED ARCHITECTURE FOR TELECOM SLAVE CLOCK

3.1.4.1 Telecom Slave Clock - IEEE 1588 in the Timing Card

Figure 5 can also represent a distributed architecture for a Telecom slave clock implementation where the IEEE 1588 is handled in the timing card. In this architecture IEEE 1588 protocol is terminated in the timing card. The local host processor will run the clock recovery algorithm (servo) and run the alternate Best Master Clock Algorithm (BMCA) according to ITU-T G.8275.1 if the slave is part of a time/phase profile, or it will run the BMCA according to G.8265.1 if the slave is part of a frequency profile.

If this architecture represents a Slave Only Ordinary Clock (SOOC) as defined in G.8265.1, then the packet data ports in the line cards can be receiving timing packets from different T-GMs.The alternate BMCA

determines which T-GM to be used as a source of frequency and/or time.

If the slave clock has access to synchronous Ethernet then the combo mode in 82P33813 can be used. In this architecture it is also very important to control the IEEE 1588 clocks independently of the SyncE clocks. It is also important to be able to suppress phase transients on the SyncE clocks to not affect the IEEE 1588 clocks. See Chapter 3.3.2.3 for mode details on the combo mode.

If the Telecom slave clock is being used in a frequency profile, then it is important to meet the requirements defined for the Telecom Slave Clock defined in G.8265.1. Figure 7 shows how the IDT solution maps into the 1588 functional block diagram for SOOC shown in Figure 3/ G.8265.1.
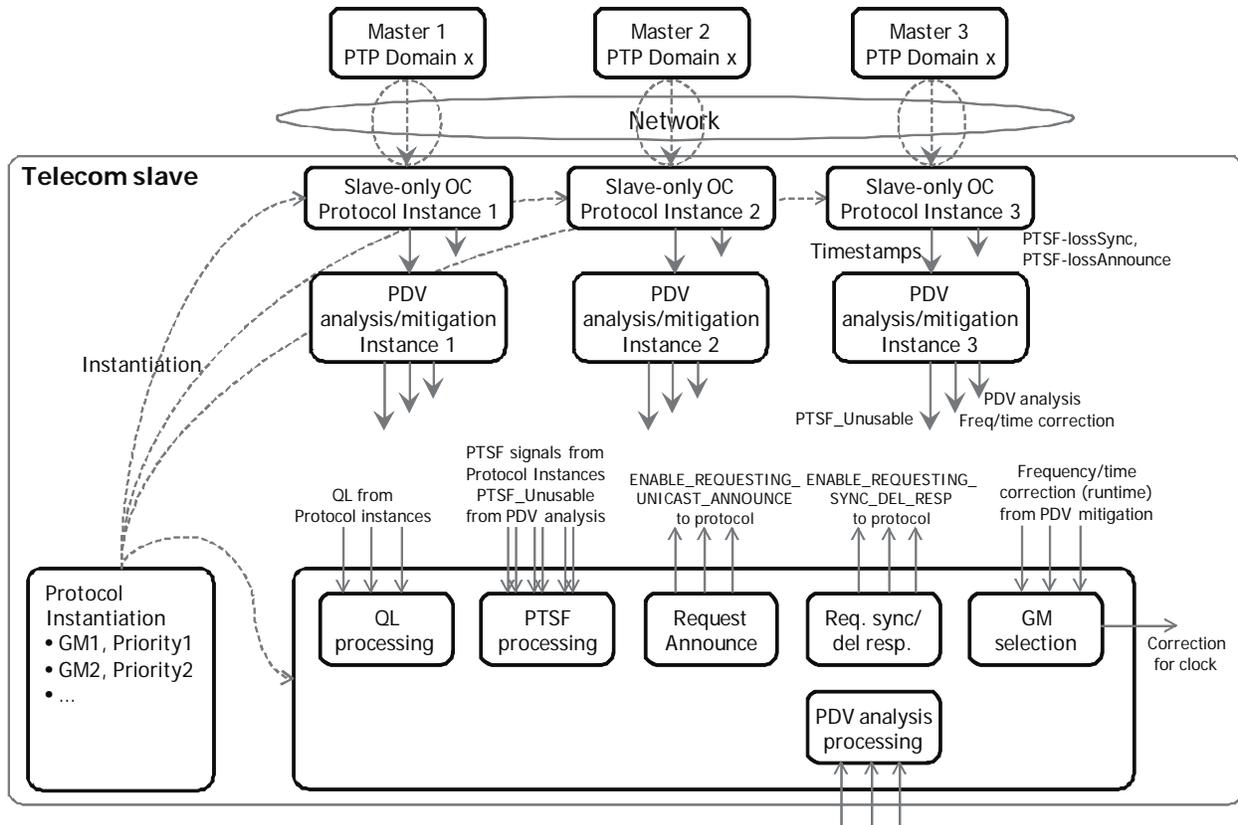

Figure 7. Telecom slave clock functional model

3.1.4.2 Telecom Slave Clock - IEEE 1588 in the Line Card

Figure 6 can also represent a distributed architecture for a Telecom slave clock implementation where the IEEE 1588 is handled in the line cards. In this architecture IEEE 1588 protocol is terminated at the line cards.

The local host processor will run the clock recovery algorithm (servo) and run the alternate Best Master Clock Algorithm (BMCA) according to ITU-T G.8275.1 and G.8275.2 if the slave is part of a time/phase profile, or it will run the BMCA according to G.8265.1 if the slave is part of a frequency profile.

If this architecture represents a Slave Only Ordinary Clock (SOOC) then the packet data ports in the line cards can be receiving timing packets from different T-GMs.The alternate BMCA determines which T-GM to be used as a source of frequency and/or time.

The 82P33813 disciplined DCO mode is very important for this architecture as it allows the use of a simple crystal (e.g. 20ppm) at the line cards, as the SyncE clock coming from the timing card will be used at the line card to be used as the local frequency. Also in this architecture it is very important to control the IEEE 1588 clocks independently of the SyncE clocks. It is also important to be able to suppress phase transients on the SyncE clocks to not affect the IEEE 1588 clocks. See Chapter 3.3.2.2 for mode details on the disciplined DCO mode.

3.2 SYNCHRONOUS ETHERNET, SONET AND SDH ARCHITECTURE

82P33813 integrates key features that allows the device to be used in Synchronous Ethernet, SONET and SDH applications. There are several key synchronization standards that are important to meet for such a system, they are:

- ITU-T Recommendation G.8262, Timing characteristics of Synchronous Ethernet Equipment slave clock (EEC)

- ITU-T Recommendation G.8264, Distribution of timing through packet networks
- ITU-T Recommendation G.812, Timing requirements of slave clocks suitable for use as node clocks in synchronization networks.
- ITU-T Recommendation G.813, Timing characteristics of SDH equipment slave clocks (SEC).
- GR-253-CORE - Telcordia Technologies Generic Requirements - Issue 5, October 2009
- GR-1244-CORE - Telcordia Technologies Generic Requirements - Issue 4, October 2009
- ATIS-0900101.2006 - T1.101 - Synchronization Interface Standard

Figure 8 shows a single blade architecture that it is usually used in simple equipment.

Figure 8.
SyncE/SONET/SDH single blade application

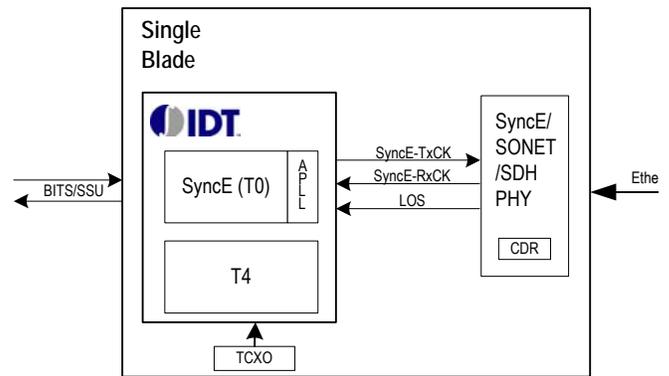Figure 9 shows an active/redundant architecture, as described before it is usually used in Telecom equipment that are designed to have a redundant timing card in case of primary timing card failure. The redundant timing card mimics the output of the active timing card, so in case of failure the system will still provide proper synchronization.
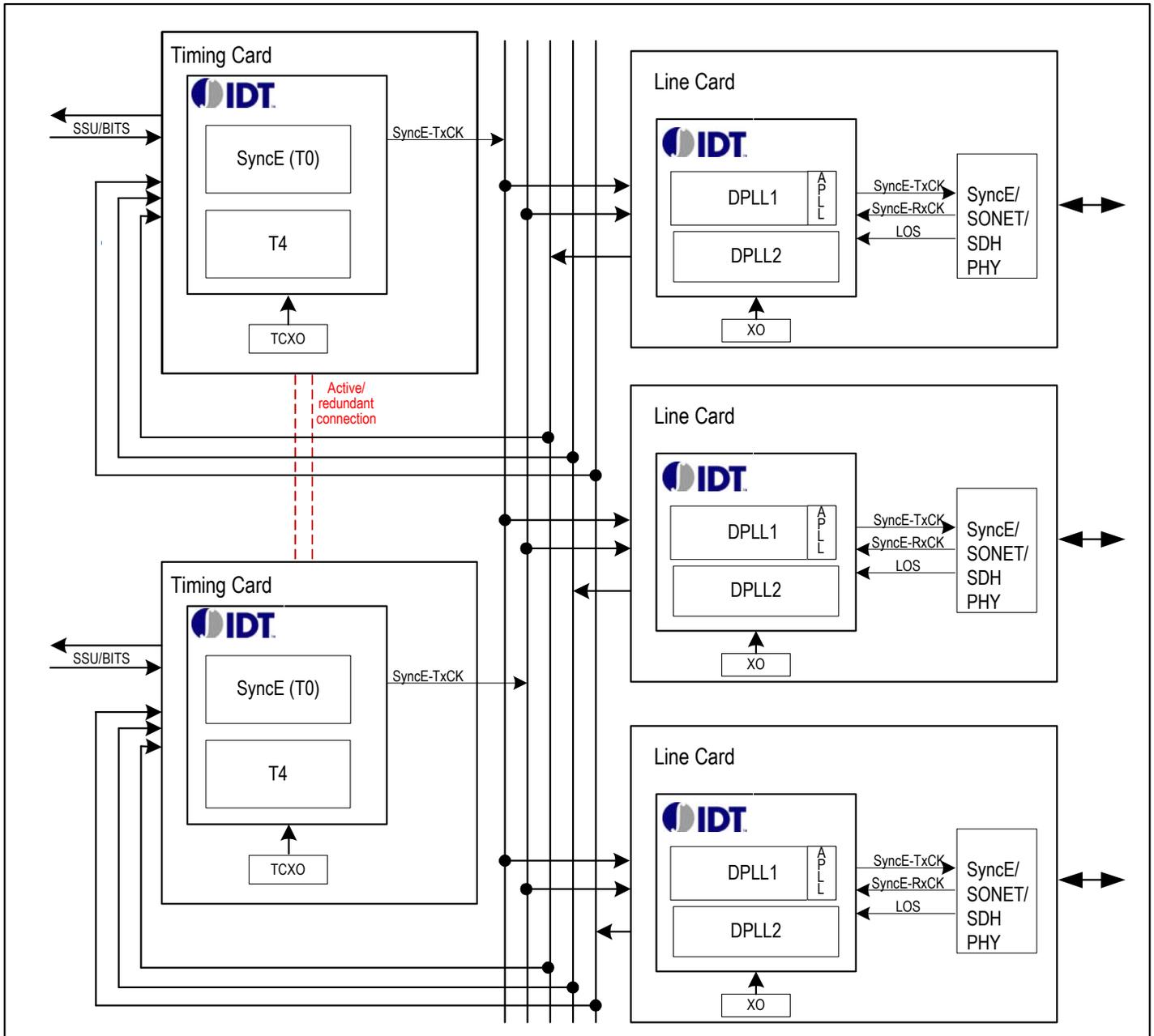
Figure 9. SyncE/SONET/SDH active/redundant application

3.3 HARDWARE FUNCTIONAL DESCRIPTION

3.3.1 SYSTEM CLOCK

A crystal oscillator should be used as an input on the OSCI pin. This clock is provided for the device as a system clock. The system clock is used as a reference clock for all the internal circuits. The active edge of the system clock can be selected by the OSC_EDGE bit in xo_freq_cnfg register.

Eight common oscillator frequencies can be used for the stable System Clock. The oscillator frequency can be set by pins or by xo_freq_cnfg register as shown in Table 2.

Table 2: Oscillator Frequencies

xo_freq[2:0] pins xo_freq_cnfg[2:0] bits	Oscillator Frequency (MHz)
000	10.000
001	12.800
010	13.000
011	19.440
100	20.000
101	24.576
110	25.000
111	30.720

An offset from the nominal frequency may be compensated by setting the NOMINAL_FREQ_VALUE[23:0] bits. The calibration range is within ±741 ppm.

The crystal oscillator should be chosen accordingly to meet different applications and standard requirements. (See AN-807 Recommended Crystal Oscillators for NetSynchro WAN PLL).

3.3.2 MODES OF OPERATION

3.3.2.1 DCO control modes

Figure 10 and Figure 11 show a high level diagram of the DCO control architecture, it shows the DCO in DPLL2 being controlled, but both DPLL1 and DPLL2 have the same capabilities, they are identical. The DCO is a phase accumulator running at an internal clock. The DCO is controlled by a digital word that can represent phase offset or frequency offset. In the case of an IEEE 1588 application, the external processor will run the clock recovery servo algorithm and it will generate a phase offset word or a frequency offset word to control the DCO.

The DCO control modes can be set by registers DPLL1_operating_mode_cnfg and DPLL2_operating_mode_cnfg for DPLL1 and DPLL2 respectively.

Figure 10 shows the DCO being controlled by writing a frequency offset word into the DCO, then by changing temporarily the DCO's frequency, the phase of the clock (or 1PPS) being generated by the DCO will also change. The output phase change is the product of the frequency change times the duration for which the frequency change is applied for. Because the DCO's frequency word has a very fine resolution, the output phase can be adjusted in very fine steps. In this case the clock recovery servo algorithm controls the bandwidth and phase slope limiting. The frequency offset word can be written into DPLL1_holdover_freq_cnfg[39:0] bits of frequency configuration registers for DPLL1, and into DPLL2_holdover_freq_cnfg[39:0] bits of frequency configuration registers for DPLL2. This value is 2's complement signed number. Total range is +/-92 ppm, and the DCO programming resolution is [(77760 / 1638400) * 2^-48] or ~1.686305041e-10 ppm. The DCO resolution is affected by the offset applied into the DCO, so when writing into the DCO, the programming resolution is [(77760/1638400) * 2^-48] * (1 + offset-in-ppm / 1e6).

Controlling the DCO's frequency for smaller fine resolution phase changes is a good method, but for bigger phase changes it is better to use the snap-alignment method. The snap phase alignment is fast but only provides coarse adjustment. The 82P33813 allows for both the fine phase adjustment by controlling the frequency of the DCO and the coarse phase adjustment by snap-align the output clock (or 1PPS), for details, see section 3.3.7.3 Output Phase control on page 39.

Figure 11 shows the DCO being controlled by writing a phase offset word into the DCO, then the clock recovery servo algorithm directly controls the DPLL phase, which in turn controls DCO phase with hardware controlled bandwidth (e.g. 0.1Hz per G.8273.2) and phase slope limiting. This method allows a better control of the bandwidth of the clock as the bandwidth is controlled in hardware, so it makes it easier to meet G.8273.2 (G.8273.2 specifies the T-BC bandwidth to be between 0.05Hz and 0.1Hz). The phase offset word can be written into DPLL1_phase_offset_cnfg[28:0] of phase configuration registers for DPLL1, and into DPLL2_ phase_offset_cnfg[28:0] of phase configuration registers for DPLL2. The update rate needs to be at least 60 times of the loop filter bandwidth, as an example, for 0.1Hz, the update should be >6Hz.

This value is 2's complement number, phase programming resolution is 0.0745ps and the total range is +/-20us This mode is enabled by writing the ph_offset_en in those registers.
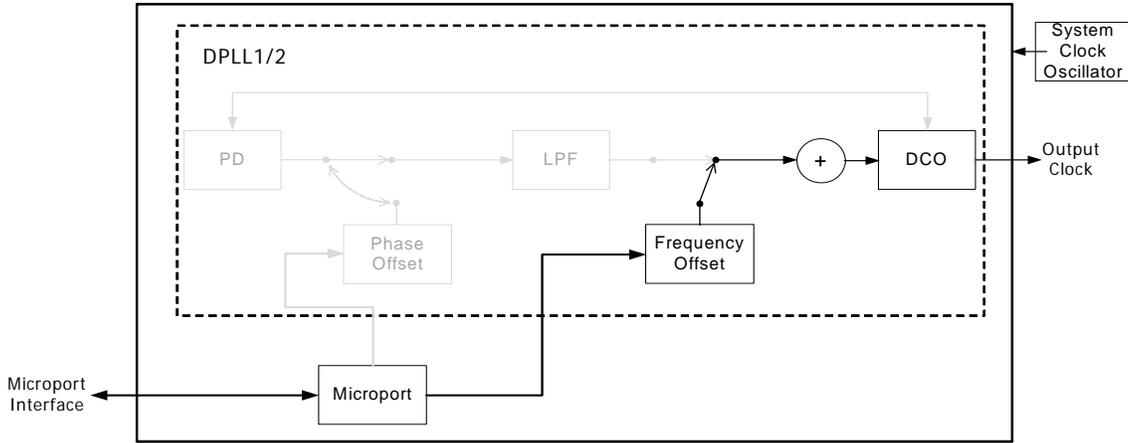
Figure 10. DCO frequency offset Control functional block diagram
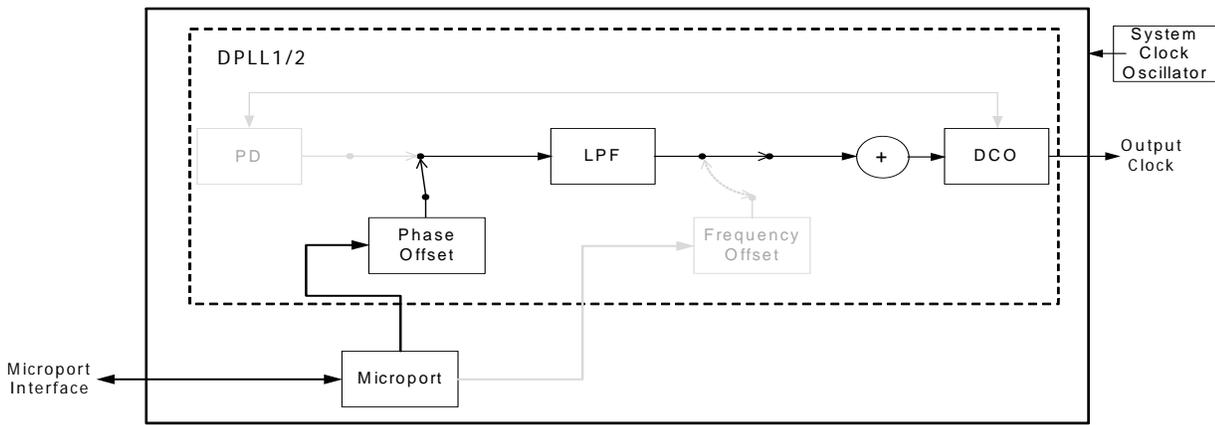
Figure 11. DCO phase offset Control functional block diagram

3.3.2.2 Disciplined DCO

Figure 12 shows a high level diagram of the Disciplined Digital Controlled Oscillator (DCO) mode. The 82P33813 uses a SyncE reference (or any other physical layer reference, e.g. SONET/SDH) to stabilize the local oscillator and create a disciplined DCO. The long term stability of the disciplined DCO is the same as the SyncE (SONET/SDH) reference.

In this mode, two PLL cores are used. DPLL1 (or DPLL2) will be locked to the physical layer clock and its output clock will be used as the local oscillator for the DCO, so the DCO will be disciplined by the SyncE clock. This is done all inside the device, no need to route the clocks externally. It is also important to be able to control phase transients in the SyncE clock. This can be done by either using an internal filter that will filter the SyncE transients, or by suppressing the SyncE based on SSM clock quality level.

The disciplined DCO mode is very useful for applications as depicted in Figure 6 where the IEEE 1588 is terminated in the line card. In this case, by using the disciplined DCO, a simple lower stability local clock oscillator can be used in the line cards instead of a TCXO or an OCXO.
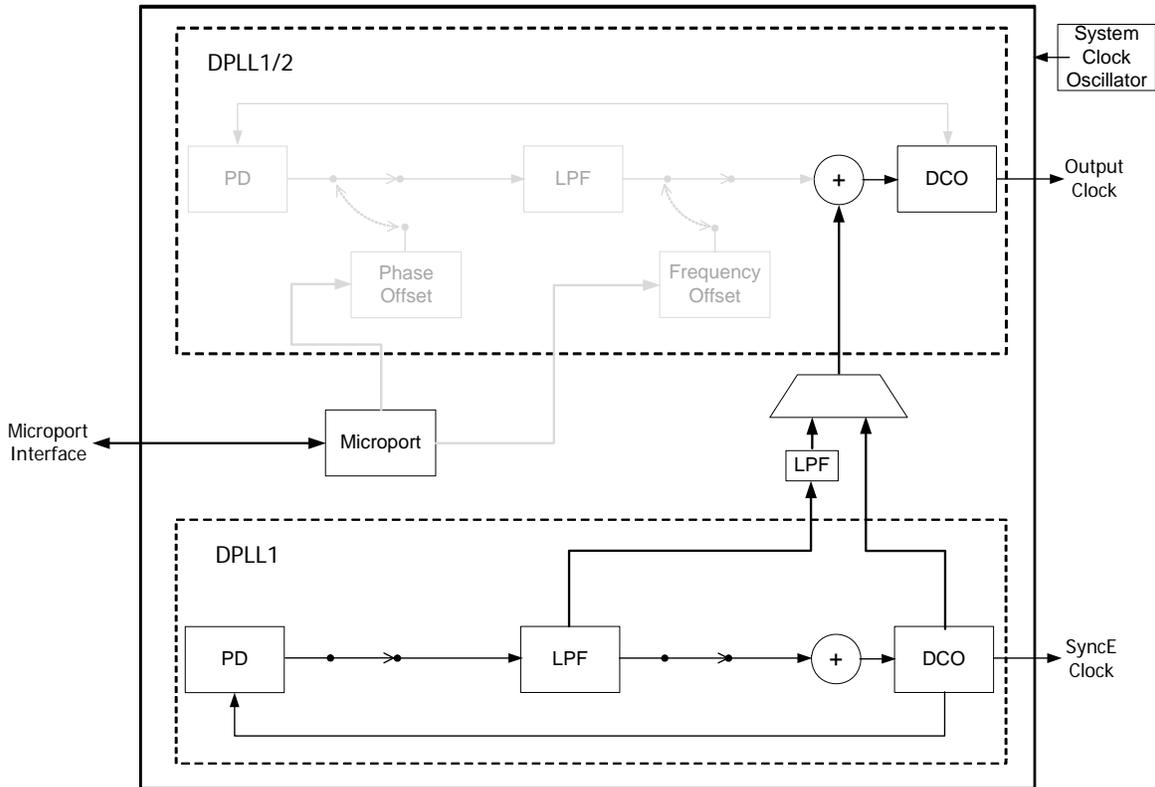

Figure 12. Disciplined DCO mode

3.3.2.3 Combo Mode

Figure 13 shows a high level diagram of the Combo mode using frequency control and Figure 14 shows a high level diagram of the Combo mode using phase control. The 82P33813 uses the disciplined DCO to provide a stable time base for the IEEE 1588 clock recovery servo algorithm.

In this mode, two PLL cores are used. DPLL1 (or DPLL2) will be locked to the physical layer clock the second DCO will be controlled by IEEE 1588 clock recovery servo algorithm. The IEEE 1588 timestamps are used to calculate the phase offset between the IEEE 1588 master's 1 PPS pulse and the IEEE 1588 slave's 1 PPS pulse and then align the two pulses by moving the slave's 1 PPS pulse in phase. The slave must be able to move the 1 PPS pulse by +/- 0.5 s, and the 82P33813 provides this capability.

The combo mode is very useful for implementations of T-BC per ITU-T Recommendations. ITU-T Recommendation G.8271.1defines congruent and non-congruent scenarios. Congruent scenario is defined when both the physical layer frequency and phase/time follow the same synchronization path, and non-congruent scenario is defined when both the physical layer frequency and phase/time do not follow the same synchronization path. As it is stated in G.8271.1, the non-congruent scenario represents a worst-case for the combination of PTP and SDH/SyncE.

The combo mode was designed to deal with the worst case scenario when the physical layer clock and the IEEE 1588 clock are not traceable to the same primary reference (e.g. the physical layer clock is traceable to the Primary Reference Clock (PRC) and the IEEE 1588 clock is traceable to the Primary Reference Time Clock (PRTC)). In this scenario the Telecom Slave clock will have to track 2 different frequencies: the physical layer frequency and the IEEE 1588 frequency. An alternative way of combining SyncE and IEEE 1588 is to initially frequency lock to a SyncE clock as the input reference, then the slave switches to the IEEE 1588 packet stream as the timing reference. This method will only work if the SyncE clock and the IEEE 1588 timing are traceable to the same PRTC. It is recommended to use the Combo mode as it will work in both cases: when the physical layer clock and the IEEE 1588 clock are not traceable to the same primary reference, and also when they are traceable to the same primary reference.

The advantage of the combo mode is that the physical layer clock and the IEEE 1588 timing can be traceable to two separate and independent timing paths. There can be a significant frequency offset between the two without causing any problems in the slave clock. Both the physical layer clock and the IEEE 1588 clock can be recovered and filtered independently for wander and jitter by the slave clock

This is done all inside the device, no need to route the clocks externally. It is also important to be able to control phase transients in the SyncE clock. This can be done by either using an internal filter that will filter the SyncE transients, or by suppressing the SyncE transients based on SSM clock quality level.
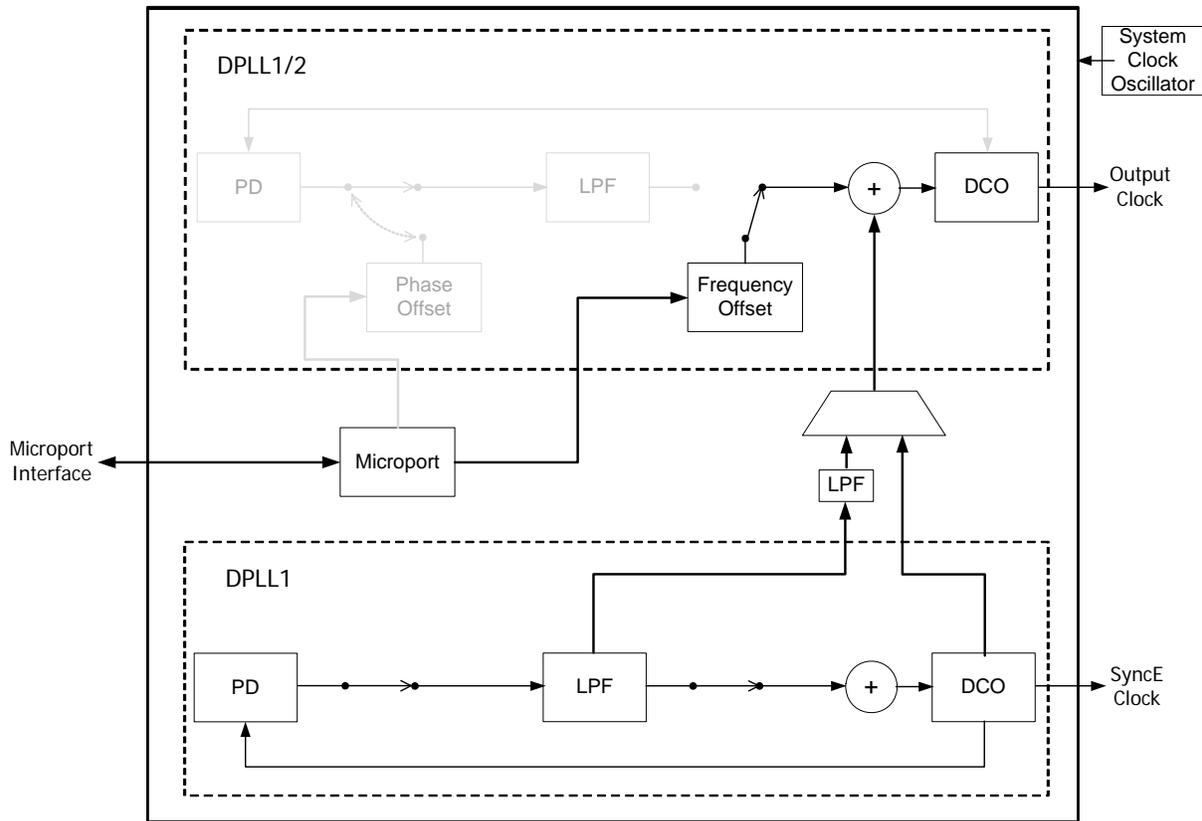
Figure 13. Combo mode using frequency control
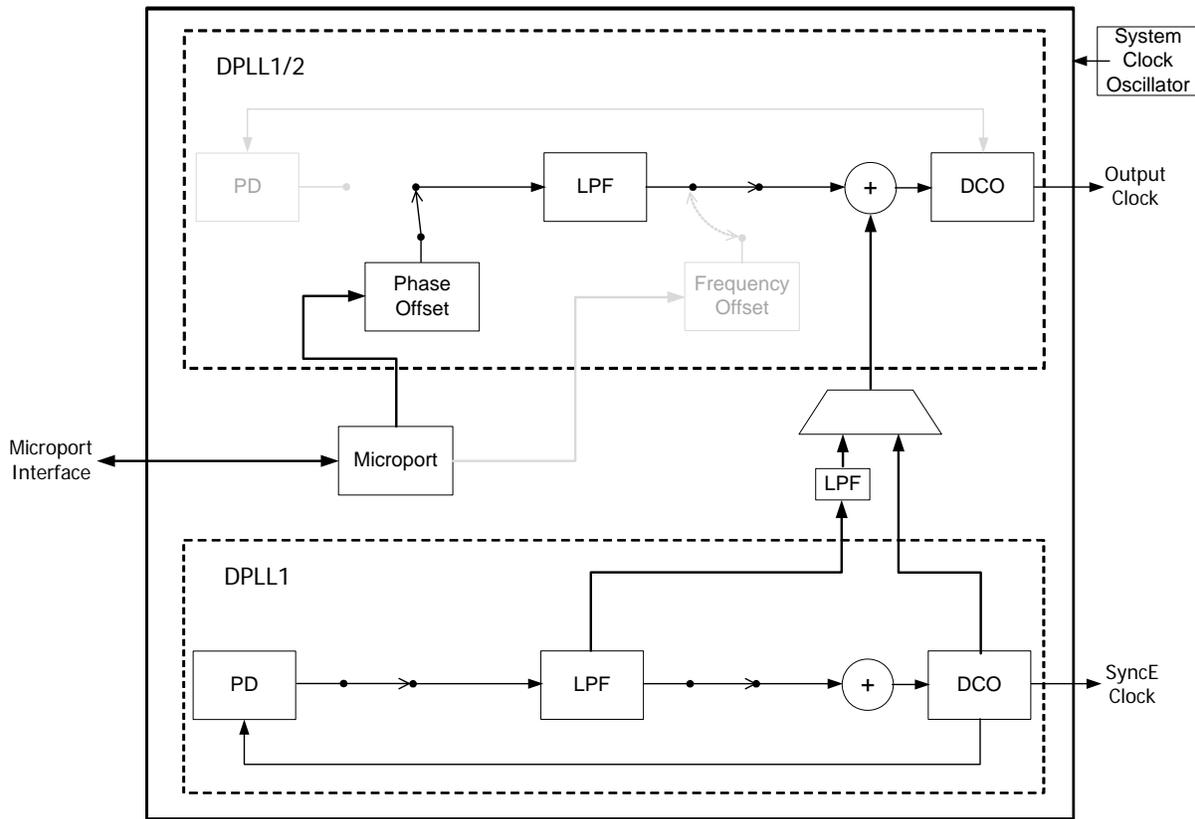
Figure 14. Combo mode using phase control

3.3.2.4 DPLL1 and DPLL2 Operating Mode

The DPLL1 and DPLL2 can operate in several different modes as shown in Table 3.

The DPLL1 and DPLL2 operating mode is controlled by the DPLL1_OPERATING_MODE[4:0] bits and DPLL2_OPERATING_- MODE[4:0] bits respectively.

When the operating mode is switched automatically, the operation of the internal state machine is shown in Figure 15.

Whether the operating mode is under external control or is switched automatically, the current operating mode is always indicated by the DPLL1/2_DPLL_OPERATING_STS[4:0] bits. When the operating mode switches, the DPLL1/2_OPERATING_STS bit will be set. If the DPLL1/2_OPERATING_STS bit is '1', an interrupt will be generated if the corresponding mask bit is set to "1", the mask bit is set to "0" by default.

Table 3: DPLL1/2 Operating Mode Control

DPLL1/2_OPERATING_MODE[4:0]	DPLL1/2 Operating Mode
00000	Automatic
00001	Forced - Free-Run
00010	Forced - Holdover
00011	Reserved
00100	Forced - Locked
00101	Forced - Pre-Locked2
00110	Forced - Pre-Locked
00111	Forced - Lost-Phase
01000-01001	Reserved
01010	DCO write frequency see Chapter 3.3.2.1)
10010	DCO write phase (see Chapter 3.3.2.1)
10011-11111	Reserved

Figure 15. DPLL Automatic Operating Mode

Notes to Figure 15:

1. Reset.

2. An input clock is selected.

*3. The DPLL selected input clock is disqualified **AND** No qualified input clock is available.*

4. The DPLL selected input clock is switched to another one.

5. The DPLL selected input clock is locked (the DPLL_LOCK bit is '1').

*6. The DPLL selected input clock is disqualified **AND** No qualified input clock is available.*

7. The DPLL selected input clock is unlocked (the DPLL_LOCK bit is '0').

8. The DPLL selected input clock is locked again (the DPLL_LOCK bit is '1').

9. The DPLL selected input clock is switched to another one.

10. The DPLL selected input clock is locked (the DPLL_LOCK bit is '1').

*11. The DPLL selected input clock is disqualified **AND** No qualified input clock is available.*

12. The DPLL selected input clock is switched to another one.

*13. The DPLL selected input clock is disqualified **AND** No qualified input clock is available.*

14. An input clock is selected.

15. The DPLL selected input clock is switched to another one.

The causes of Item 4, 9, 12, 15 - 'the *DPLL* selected input clock is switched to another one' - are: (The *DPLL* selected input clock is disqualified AND Another input clock is switched to) OR (In Revertive switching, a qualified input clock with a higher priority is switched to) OR (The DPLL selected input clock is switched to another one Forced selection).

3.3.2.4.1 Free-Run Mode

In Free-Run mode, the DPLL1/2 output refers to the system clock and is not affected by any input clock. The accuracy of the DPLL1/2 output is equal to that of the system clock.

3.3.2.4.2 Pre-Locked Mode

In Pre-Locked mode, the DPLL1/2 output attempts to track the selected input clock.

The Pre-Locked mode is a secondary, temporary mode.

3.3.2.4.3 Locked Mode

In Locked mode, the DPLL1/2 is locked to the input clock. The phase and frequency offset of the DPLL1/2 output track those of the DPLL1/2 selected input clock.

For a closed loop, different bandwidths and damping factors can be used depending on DPLL locking stages: starting, acquisition and locked.

In the first two seconds when the DPLL1/2 attempts to lock to the selected input clock, the starting bandwidth and damping factor are used. They are set by the DPLL1/2_START_BW[4:0] bits and the DPLL1/2_START_DAMPING[2:0] bits respectively.

During the acquisition, the acquisition bandwidth and damping factor are used. They are set by the DPLL1/2_ACQ_BW[4:0] bits and the DPLL1/2_ACQ_DAMPING[2:0] bits respectively.

When the DPLL1/2 is locked, the locked bandwidth and damping factor are used. They are set by the DPLL1/2_LOCKED_BW[4:0] bits and the DPLL1/2_LOCKED_DAMPING[2:0] bits respectively.

The corresponding bandwidth and damping factor are used when the DPLL1/2 operates in different locking stages: starting, acquisition and locked, as controlled by the device automatically.

The locked bandwidth is selectable can be set as shown in Table 4.

Table 4: DPLL1/2 Locked Bandwidth

DPLL1/2_LOCKED_BW[4:0]	BW	Application
00000	0.090 mHz	
00001	0.27 mHz	
00010	0.90 mHz	stratum 3E, BW<1mHz
00011	2.9 mHz	G.812 Type I, BW< 3mHz
00100	4.3 mHz	
00101	8.7 mHz	
00110	17 mHz	
00111	35 mHz	
01000	69 mHz	
01001	92 mHz	GR-253 stratum 3, SMC and EEC-option, 2, BW $\leq$ 0.1Hz
01010	277 mHz	
01011	554 mHz	
01100	1.1 Hz	EEC-option 1, 1$\leq$ BW $\leq$10 GR-1244 stratum 3, BW$\leq$3Hz
01101	2.2 Hz	EEC-option 1, 1$\leq$ BW $\leq$10 GR-1244 stratum 3, BW$\leq$3Hz
01110	4.4 Hz	EEC-option 1, 1$\leq$ BW $\leq$10
01111	8.9 Hz	EEC-option 1, 1$\leq$ BW $\leq$10
10000	18 Hz	
10001	35 Hz	
10010	71 Hz	
10011	142 Hz	
10100	283 Hz	
10101	567 Hz	
10110-11111	Reserved	

3.3.2.4.4 Pre-Locked2 Mode

In Pre-Locked2 mode, the DPLL1/2 output attempts to track the selected input clock.

The Pre-Locked2 mode is a secondary, temporary mode.

3.3.2.4.5 Lost-Phase Mode

In Lost-Phase mode, the DPLL1/2 output attempts to track the selected input clock.

The Lost-Phase mode is a secondary, temporary mode.

3.3.2.4.6 Holdover Mode

In Holdover mode, the DPLL1/2 resorts to the stored frequency data acquired in Locked mode to control its output. The DPLL1/2 output is not phase locked to any input clock. The frequency offset acquiring method is selected by the man_holdover bit, auto_avg bit, the hist_mode [1:0] bits, and the avg_mode[1:0] bits in DPLL1/2_holdover_mode_cnfg registers as shown in Table 5.

Table 5: Frequency Offset Control in Holdover Mode

man_hold over	auto_avg	hist_mode [1:0]		avg_mode[1:0]		Frequency Offset Acquiring Method
0	0	don't-care		don't-care		Averaged
	1	0	0	0	0	Current averaged value with holdover filter BW of ~0.18mHz
				0	1	Current averaged value with holdover filter BW of ~1.5mHz
				1	0	Current averaged value with holdover filter BW of ~12mHz
				1	1	Current averaged value with holdover filter BW of ~0.15Hz
		0	0	0	0	Averaged value 1 second before with holdover filter BW of ~0.18mHz
				0	1	Averaged value 1 second before with holdover filter BW of ~1.5mHz
				1	0	Averaged value 1 second before with holdover filter BW of ~12mHz
				1	1	Averaged value 1 second before with holdover filter BW of ~0.15Hz
		0	1	0	0	Averaged value 8 seconds before with holdover filter BW of ~0.18mHz
				0	1	Averaged value 8 seconds before with holdover filter BW of ~1.5mHz
				1	0	Averaged value 8 seconds before with holdover filter BW of ~12mHz
				1	1	Averaged value 8 seconds before with holdover filter BW of ~0.15Hz
		1	0	0	0	Averaged value 64 seconds before with holdover filter BW of ~0.18mHz
				0	1	Averaged value 64 seconds before with holdover filter BW of ~1.5mHz
				1	0	Averaged value 64 seconds before with holdover filter BW of ~12mHz
				1	1	Averaged value 64 seconds before with holdover filter BW of ~0.15Hz
1	don't-care					Manual - values is set by DPLL1/2_holdover_freq_cnfg register

The default value for holdover mode is set to current averaged value with holdover filter BW of ~1.5mHz. In this mode the initial frequency offset is better than 1.1e-5ppm assuming that there is no in-band jitter/wander at the input just before entering holdover state. The default mode is used for Telcordia GR-1244, Telcordia GR-253, ITU-T G.8262 and ITU-T G.813 to meet holdover requirements.

In Manual Mode, the frequency offset is set by the DPLL1/2_holdover_freq_cnfg[39:0] bits. The accuracy is 1.686305041e-10 ppm, however the resolution is affected by the frequency offset applied, so when writing the frequency offset, the programming resolution is $[(77760/1638400) * 2^{-48}] * (1 + \text{offset-in-ppm} / 1e6)$.

The offset value, which is acquired by the modes shown in Table 5, can be read from the holdover_freq_cnfg[39:0] bits by setting the read_avg bit to "1". If read_avg bit is set to "0" then the value in holdover_freq_cnfg[39:0] bits is the value written into it. The value is 2's complement signed number, and the total range is +/- 92 ppm.

The holdover frequency resolution is calculated as follows:

Holdover Frequency resolution: $HO\_freq\_res = (77760/1638400) * 2^{-48}$

The Holdover value read from register bits holdover_freq_cnfg[[39:0] must be converted to decimal:

$HO\_value\_dec = holdover\_freq\_cnfg[39:0]$ value in decimal

The frequency offset in ppm is calculated as follows:

Holdover Frequency Offset (ppm) = $(HO\_freq\_res * HO\_value\_dec)/(1-((HO\_freq\_res * HO\_value\_dec)/1e6))$

3.3.2.4.7 Hitless Reference Switching

Bit hitless_switch_en in DPLL1/2_mon_sw_pbo_cnfg register can be used to set hitless reference switching. When a Hitless Switching (HS) event is triggered, the phase offset of the selected input clock with respect to the DPLL1/2 output is measured. The device then automatically accounts for the measured phase offset and compensates for the appropriate phase offset into the DPLL output so that the phase transients on the DPLL1/2 output are minimized. The input frequencies should be set to frequencies equal to 8kHz or higher.

If hitless_switch_en is set to "1", a HS event is triggered if any one of the following conditions occurs:
- DPLL1/2 selected input clock switches to a different reference
- DPLL1/2 exits from Holdover mode or Free-Run mode

For the two conditions, the phase transients on the DPLL1/2 output are minimized to be no more than 0.61 ns with HS. The HS can also be frozen at the current phase offset by setting the hitless_switch_freeze bit in DPLL1/2_mon_sw_pbo_cnfg register. When the HS is frozen, the device will ignore any further HS events triggered by the above two conditions, and maintain the current phase offset.

When the HS is disabled, there may be a phase shift on the DPLL1/2 output, as the DPLL1/2 output tracks back to 0 degree phase offset with respect to the DPLL1/2 selected input clock. This phase shift can be limited; see section 3.3.2.4.8 Phase Slope Limit.

3.3.2.4.8   Phase Slope Limit

To meet the phase slope requirements of Telcordia and new ITU-T standards, both DPLL1 and DPLL2 provide a phase slope limiting feature to limit the rate of output phase movement. The limit level is selectable via DPLL1/2_ph_limit[2:0] bits in DPLL1/2_bw_overshoot_cnfg register. The options are shown in Table 6.

Table 6: DPLL1/2 Phase Slope Limit

DPLL1/2_ph_limit[2:0]	Phase Slope Limit
000	61µs/s (GR-1244 ST3)
001	885ns/s (GR-1244-CORE ST2 and 3E, GR-253-CORE ST3 and G.8262 EEC option 2)
010	7.5 µs/s (G.813 opt1, G.8262 EEC-option 1)
011	unlimited / 1.4 ms/s (default)
100	1 ns/s
101	5 ns/s
110	10 ns/s
111	programmable (default)*
*Note: The default phase slope limiting is set to programmable with a default value set to 0 ns/s, therefore the phase slope limiting must be set to the proper value to meet different standards according to this table.	

The programmable phase slope limiting can be set by writing into registers DPLL1/2_prog_ph_limit_cnfg[23:0]. The range of the programmable limit is 1484.3614 us/s.

3.3.2.4.9   Frequency Offset Limit

The DPLL1/2 output is limited to be within the programmed DPLL hard limit (refer to Chapter 3.3.4.3).

3.3.2.5   DPLL3 Operating Mode

The DPLL3 operating mode is controlled by the DPLL3_OPERATING_MODE[2:0] bits, as shown in Table 7. DPLL3 is disabled by default, write "0" to bit DPLL3_dpll_pdn in pdn_conf register to enable it.

Table 7: DPLL3 Operating Mode Control

DPLL3_OPERATING_MODE[2:0]	DPLL3 Operating Mode
000	Automatic
001	Forced - Free-Run
010	Forced - Holdover
100	Forced - Locked

When the operating mode is switched automatically, the operation of the internal state machine is shown in Figure 16:
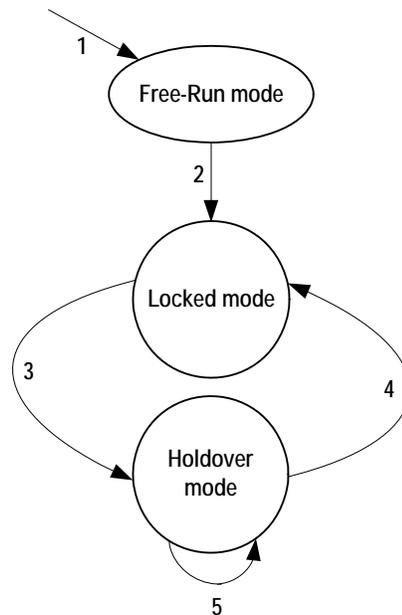
Figure 16. DPLL3 Automatic Operating Mode

Notes to Figure 16:
1. Reset.
2. An input clock is selected.
3. (The DPLL3 selected input clock is disqualified) OR (A qualified input clock with a higher priority is switched to) OR (The DPLL3 selected input clock is switched to another one by Forced selection).
4. An input clock is selected.
5. No input clock is selected.

3.3.2.5.1   Free-Run Mode

In Free-Run mode, the DPLL3 output refers to the system clock and is not affected by any input clock. The accuracy of the DPLL3 output is equal to that of the system clock.

3.3.2.5.2   Locked Mode

In Locked mode, the DPLL3 is locked to the input clock. The phase and frequency offset of the DPLL3 output track those of the DPLL3 selected input clock.

DPLL3 is a wide BW DPLL, with loop bandwidth higher than 25Hz.

3.3.2.5.3   Holdover Mode

In Holdover mode, the DPLL3 has 2 modes of operation for the holdover set by DPLL3_auto_avg bit in DPLL3_holdover_mode_cnfg register.

DPLL3_auto_avg = 0: holdover frequency is the instantaneous value of integral path just before entering holdover. If the DPLL3 was locked to an input clock reference that has no in-band jitter/wander and was then

manually set to go into holdover, the initial frequency accuracy is 4.4X10-8 ppm.

DPLL3_auto_avg = 1: averaged frequency value is used as holdover frequency. The holdover average bandwidth is about 1.5mHz. In this mode the initial frequency offset is 1.1e-5ppm assuming that there is no in-band jitter/wander at the input just before entering holdover state.

3.3.2.5.4   Frequency Offset Limit

The DPLL3 output is limited to be within the DPLL hard limit (refer to Chapter 3.3.4.3).

3.3.3   INPUT CLOCKS AND FRAME SYNC

The 82P33813 has 6 input clocks that can also be used for frame sync pulses.

The 82P33813 supports Telecom and Ethernet frequencies from 1PPS up to 650 MHz.

Any of the input clocks can be used as a frame pulse or sync signal. The SYNC_sel[3:0] bits in IN*n*_los_sync_cnfg (1 ≤ *n* ≤ 6) registers sets which pin is used as frame pulse or sync signal.

IN1 to IN6 can be used for 2 kHz, 4 kHz or 8 kHz frame pulses or 1PPS sync signal.The input frequency should match the setting in the sync_freq[1:0] bits in DPLL1/2_input_mode_cnfg register.

3.3.3.1   Input Clock Pre-divider

Each input clock is assigned an internal Pre-divider. The Pre-divider can be used to divide the clock frequency down to a convenient frequency, such as 8 kHz for the internal DPLL1 and DPLL2. Note that T1 and E1 references can exhibit substantial jitter with frequencies above 4 kHz. These references should be applied to DPLL1 or DPLL2 without being divided down to 8 kHz.

For IN1 ~ IN6, the DPLL required frequency is set by the corresponding IN_FREQ[3:0] bits.

Table 8: IN_FREQ[3:0] DPLL Frequency

IN_FREQ[3:0] Bits	DPLL Frequency
0000	8 kHz
0001	1.544 MHz / 2.048 MHz (depends on SONET/ SDH bit)
0010	6.48 MHz
0011–1000	Reserved
1001	2 kHz
1010	4 kHz
1011	1 PPS
1100	6.25 MHz
1101–1111	Reserved

Each Pre-divider consists of an FEC divider and a DivN divider,. IN1~IN4 also include an HF (High Frequency) divider. Figure 17 shows a block diagram of the pre-dividers for an input clock.

For 1 PPS, 2 kHz, 4 kHz or 8 kHz input clock frequency only, the Pre-divider should be bypassed by setting INn_DIV[1:0] bits = "0" (1 ≤ n ≤ 4), DIRECT_DIV bit = "0", and LOCK_8K bit = "0". The corresponding IN_-FREQ[3:0] bits should be set to match the input frequency.

The HF divider, which is available for IN1 ~ IN4, should be used when the input clock is higher than (>) 162.5 MHz. The input clock can be divided by 4, 5 or can bypass the HF divider, as determined by the INn_DIV[1:0] bits (1 ≤ n ≤ 4).

The DivN divider can be bypassed, as determined by the DIRECT_DIV bit and the LOCK_8K bit. When DivN divider is bypassed, the corresponding IN_FREQ[3:0] bits should be set to match the input

frequency. DIVN must be bypassed on a reference clock input that is also associated with another reference input used as SYNC.

When the DivN divider is used for INn (1 ≤ n ≤ 6), the division factor setting should observe the following order:
1. *Write the lower eight bits of the division factor to the PRE_DIVN_VALUE[7:0] bits;*
2. *Write the higher eight bits of the division factor to the PRE_DIVN_VALUE[14:8] bits.*

The division factor is calculated as follows:
Division Factor = (the frequency of the clock input to the DivN divider ÷ the frequency of the DPLL required clock set by the IN_-FREQ[3:0] bits) - 1

The Pre-divider configuration and the division factor setting depend on the input clock on one of the IN1 ~ IN6 pins and the DPLL required clock.

For the fractional input divider, the FEC divider, each input clock has a 16-bit (fec_divp_cnfg[15:0]) that represents the value of the numerator and a 16-bit (fec_divq_cnfg[15:0]) that represents the value of the denominator of FEC divider. The FEC division factor is calculated as follows:

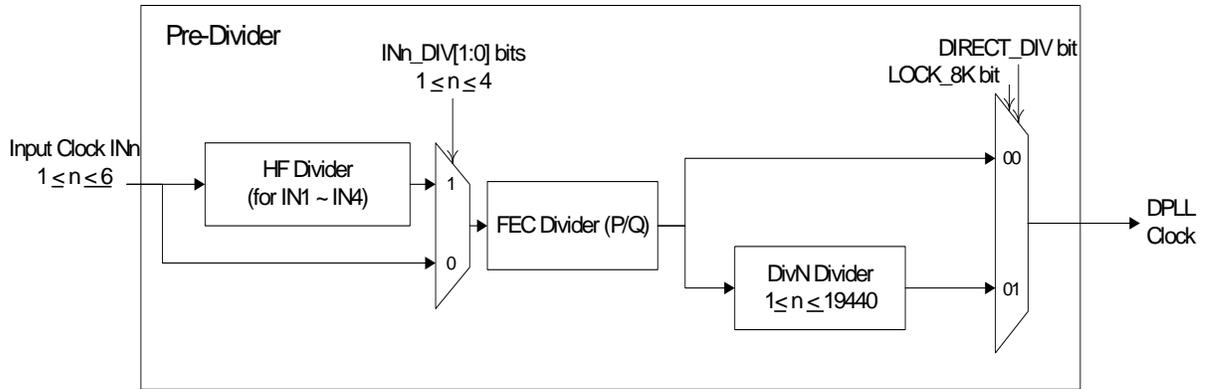*FEC Division Factor = (fec_divp_cnfg[15:0]) ÷ (fec_divq_cnfg[15:0])*

Figure 17. Pre-divider for an input clock

3.3.3.2 Input Clock Quality Monitoring

The qualities of all the input clocks are always monitored in the following aspects:

- Activity
- Frequency

Activity and frequency monitoring are conducted on all the input clocks.

The qualified clocks are available for selection for all 3 DPLLs.

3.3.3.2.1 Activity Monitoring

Activity is monitored by using an internal leaky bucket accumulator, as shown in Figure 18.

Each input clock is assigned an internal leaky bucket accumulator. The input clock is monitored for each period of 128 ms, the internal leaky bucket accumulator is increased by 1 when an event is detected; and it is decreased by 1 when no event is detected within the period set by the decay rate. The event is that an input clock drifts outside (>) ±500 ppm with respect to the system clock within a 128 ms period.

There are four configurations (0 - 3) for a leaky bucket accumulator. The leaky bucket configuration for an input clock is selected by the cor-responding BUCKET_SEL[1:0] bits. Each leaky bucket configuration consists of four elements: upper threshold, lower threshold, bucket size and decay rate.

The bucket size is the capability of the accumulator. If the number of the accumulated events reach the bucket size, the accumulator will stop increasing even if further events are detected. The upper threshold is a point above which a no-activity alarm is raised. The lower threshold is a point below which the no-activity alarm is cleared. The decay rate is a certain period during which the accumulator decreases by 1 if no event is detected.

The leaky bucket configuration is programmed by one of four groups of register bits: the BUCKET_SIZE_n_DATA[7:0] bits, the UPPER_THRESHOLD_n_DATA[7:0] bits, the LOWER_THRESHOLD_n_DATA[7:0] bits and the DECAY_RATE_n_DATA[1:0] bits respectively; 'n' is 0 ~ 3.

The no-activity alarm status of the input clock is indicated by the INn_NO_ACTIVITY_ALARM bit ($6 \geq n \geq 1$).

The input clock with a no-activity alarm is disqualified for clock selection for the DPLLs.
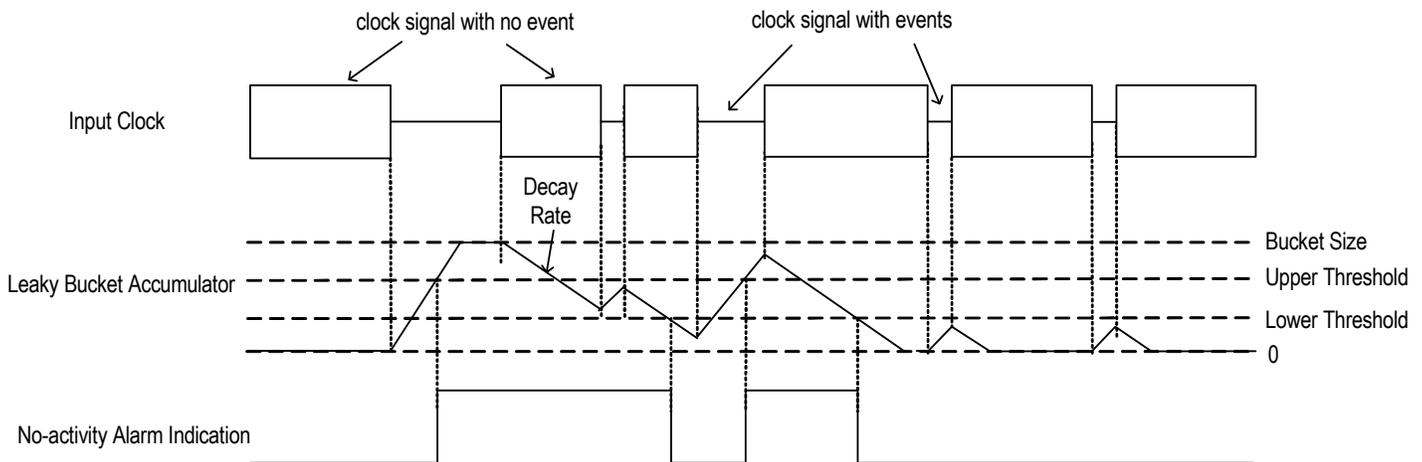
Figure 18. Input Clock Activity Monitoring

3.3.3.2.2 Frequency Monitoring

Frequency is monitored by comparing the input clock with a reference clock. The reference clock can be derived from the system clock or the output of DPLL1, as determined by the FREQ_MON_CLK bit.

Each reference clock has a hard frequency monitor and a soft frequency monitor. Both monitors have two thresholds, rejecting threshold and accepting threshold, which are set in HARD_FREQ_MON_-THRESHOLD[7:0] and SOFT_FREQ_MON_THRESHOLD[7:0]. So four frequency alarm thresholds are set for frequency monitoring: Hard Alarm Accepting Threshold, Hard Alarm Rejecting Threshold, Soft Alarm Accepting Threshold and Soft Alarm Rejecting Threshold.

The frequency hard alarm accepting threshold can be calculated as follows:

Frequency Hard Alarm Accepting Threshold (ppm) = (HARD_FRE-Q_MON_THRESHOLD[7:4] + 1) X FREQ_MON_FACTOR[3:0] (b3~0, FREQ_MON_FACTOR_CNFG)

The frequency hard alarm rejecting threshold can be calculated as follows:

Frequency Hard Alarm Rejecting Threshold (ppm) = (HARD_FRE-Q_MON_THRESHOLD[3:0] + 1) X FREQ_MON_FACTOR[3:0] (b3~0, FREQ_MON_FACTOR_CNFG)

When the input clock frequency rises to above the hard alarm rejecting threshold, the INn_FREQ_HARD_ALARM bit (6 ≥ n ≥ 1) will alarm and indicate '1'. The alarm will remain until the frequency is down to below the hard alarm accepting threshold, then the INn_FRE-Q_HARD_ALARM bit will return to '0'. There is a hysteresis between frequency monitoring, refer to Figure 19.

The soft alarm is indicated by the INn_FREQ_SOFT_ALARM bit (6 ≥ n ≥ 1) in the same way as hard alarm.

The input clock with a frequency hard alarm is disqualified for clock selection for the DPLLs, but the soft alarm doesn't affect the clock selection for the DPLLs.

The frequency of each input clock with respect to the reference clock can be read by doing the following step:

1. *Read the value in the IN_FREQ_VALUE[7:0] bits and calculate as follows:*

   *Input Clock Frequency (ppm) = IN_FREQ_VALUE[7:0] * FRE-Q_MON_FACTOR[3:0]*

Note that the value set by the FREQ_MON_FACTOR[3:0] bits depends on the application.
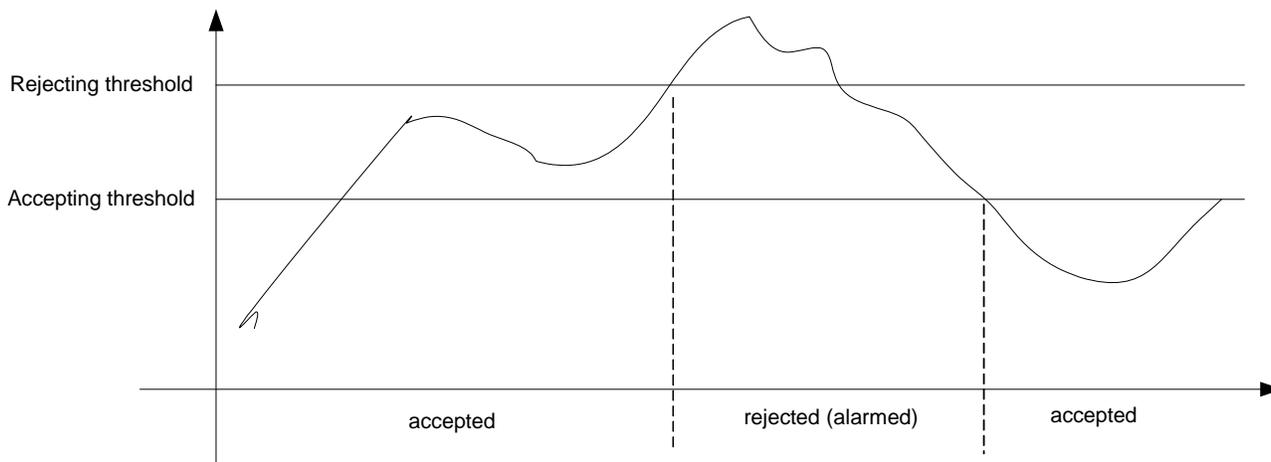
Figure 19. Hysteresis Frequency Monitoring

3.3.3.3   Input Clock Selection

For DPLL1, DPLL2 and DPLL3, the DPLL1/2/3_INPUT_SEL[3:0] bits (register DPLL1/2/3_input_sel_cnfg) determine the input clock selection, as shown in Table 9:

Table 9: Input Clock Selection for DPLL1, DPLL2 and DPLL3

DPLL1/2/3 _INPUT_SEL[3:0]	Input Clock Selection
0000	Automatic selection
0001 ~ 0010	Reserved
0011 ~ 0110	Forced selection (IN1 ~ IN4)
0111 ~ 1000	Reserved
1001 ~ 1010	Forced selection (IN5 ~ IN6)
1011 ~ 1111	Reserved

3.3.3.3.1   Forced Selection

In Forced selection, the selected input clock is set by the DPLL1_IN-PUT_SEL[3:0], DPLL2_INPUT_SEL[3:0], and DPLL3_INPUT_SEL[4:0] bits. The results of input clocks quality monitoring do not affect the input clock selection if Forced selection is used.

3.3.3.3.2 Automatic Selection

In Automatic selection, the input clock selection is determined by input clock being valid, priority and input clock configuration. The input clock is declared valid depending on the results of input clock quality monitoring (refer to Chapter 3.3.3.2). The input clock can be configured to be valid and therefore be allowed to participate in the locking process by setting to "0" the corresponding INn_VALID bit ($6 \geq n \geq 1$) in DPLL_remote_input_valid_cnfg register, by default all the inputs are not valid, and therefore the user must set the corresponding bit to "0" in order to allow the DPLL to lock to a particular input clock. Within all the qualified input clocks, the one with the highest priority is selected. The priority is set by the corresponding INn_SEL_PRIORITY[3:0] bits in DPLL_INn_sel_priority_cnfg ($6 \geq n \geq 1$). If more than one qualified input clock INn is available, then it is important to set appropriate priorities to the input clocks, two input clocks must not have the same priority. This process is shown in Figure 20.
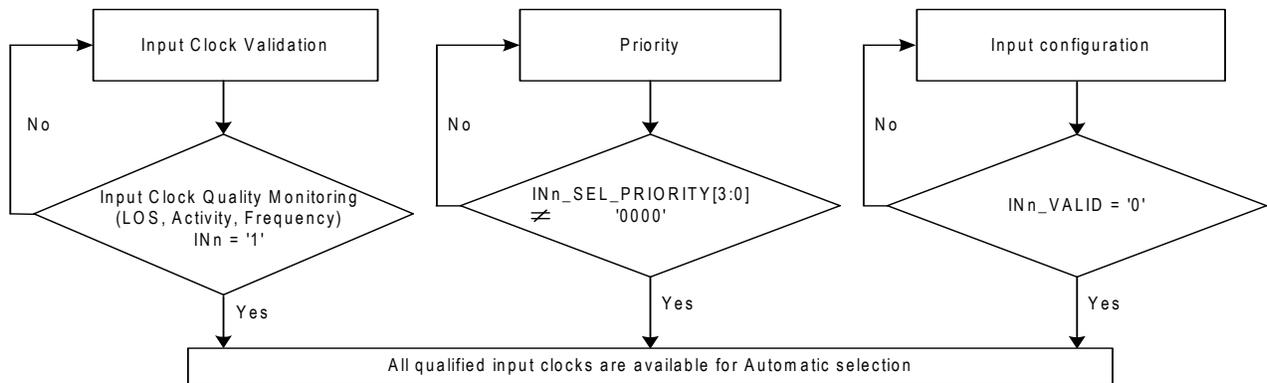
Figure 20. Qualified Input Clocks for Automatic Selection

3.3.3.3.2.1 Input Clock Validation

For all the input clocks, the input is declared valid depending on the results of input clock quality monitoring (refer to Chapter 3.3.3.2). The IN_NOISE_WINDOW bit should be set to '1' if any of INn_FREQ[3:0] is set for frequencies ≤ 8 kHz, by default it is set to '0'.

For DPLL1 and DPLL2, the following conditions must be satisfied for the input clock to be valid; otherwise, it is invalid.
- No no-activity alarm (the INn_NO_ACTIVITY_ALARM bit is '0');
- No frequency hard alarm (the INn_FREQ_HARD_ALARM bit is '0');
- No phase lock alarm, i.e., the INn_PH_LOCK_ALARM bit is '0';
- If the ULTR_FAST_SW bit is '1', the DPLL selected input clock misses less than (<) 2 consecutive clock cycles; if the ULTR_FAST_SW bit is '0', this condition is ignored;
- LOS[3:0] are not set to disqualify the input clock

For DPLL3, the following conditions must be satisfied for the input clock to be valid; otherwise, it is invalid.
- No no-activity alarm (the INn_NO_ACTIVITY_ALARM bit is '0');
- No frequency hard alarm (the INn_FREQ_HARD_ALARM bit is '0');
- LOS[3:0] are not set to disqualify the input clock

The INn bit ($6 \geq n \geq 1$) indicates whether or not the clock is valid. When the input clock changes from 'valid' to 'invalid', or from 'invalid' to 'valid), the INn bit will be set. If the INn bit is '1', an interrupt will be generated.

When the DPLL selected input clock has failed, i.e., the selected input clock changes from 'valid' to 'invalid', the DPLL_MAIN_REF_- FAILED bit will be set. If the DPLL_MAIN_REF_FAILED bit is '1', an interrupt will be generated.

3.3.3.3.2.2 Revertive and Non-Revertive Switching

For DPLL1 and DPLL2, Revertive and Non-Revertive switchings are supported, as selected by the REVERTIVE_MODE bit.

For DPLL3, only Revertive switching is supported.

GR-1244 defines Revertive and Non-Revertive Reference switching. In Non-Revertive switching, a switch to an alternate reference is maintained even after the original reference has recovered from the failure that caused the switch. In Revertive switching, the clock switches back to the original reference after that reference recovers from the failure, independent of the condition of the alternate reference. In Non-Revertive switching, input clock switch is minimized.

In Revertive switching, the selected input clock is switched when another qualified input clock with a higher priority than the current selected input clock is available. Therefore, if REVERTIVE_MODE bit is set to "1", then the selected input clock is switched if any of the following is satisfied:
- the selected input clock is disqualified;
- another qualified input clock with a higher priority than the selected input clock is available.

A qualified input clock with the highest priority is selected by revertive switching. If more than one qualified input clock INn is available, then it is important to set appropriate priorities to the input clocks, two input clocks must not have the same priority.

In Non-Revertive switching, the DPLL1/2 selected input clock is not switched when another qualified input clock with a higher priority than the current selected input clock becomes available. In this case, the selected input clock is switched and a qualified input clock with the highest priority is selected only when the DPLL1/2 selected input clock is disqualified. If more than one qualified input clock INn is available, then it is important to set appropriate priorities to the input clocks, two input clocks must not have the same priority.

3.3.3.3.3 Selected / Qualified Input Clocks Indication

The selected input clock is indicated by the CURRENTLY_SELECTED_INPUT[3:0] bits.

When the device is configured in Automatic selection and Revertive switching is enabled, the input clock indicated by the CURRENTLY_SELECTED_INPUT[3:0] bits is the same as the one indicated by the HIGHEST_PRIORITY_VALIDATED[3:0] bits.

3.3.3.3.4 Input Clock Loss of Signal

There are 4 LOS input pins (LOS[3:0]) that can be used to disqualify the input clock. If they are set high, then the associated input clock is disqualified to be used as an input clock, and therefore the DPLLs will not lock to that particular input clock.

The 4 LOS pins can be associated with any input clock by setting bits LOS_EN in INn_LOS_SYNC_CNFG (1 ≤ n ≤ 6) register. By default, the LOS pins are not associated with any input.

3.3.4 DPLL LOCKING PROCESS

The following events are always monitored for the DPLLs locking process:
- Fast Loss;
- Fine Phase Loss;
- Hard Limit Exceeding.

For proper operation, COARSE_PH_LOS_LIMT_EN must be set to 0.

3.3.4.1 Fast Loss

A fast loss is triggered when the selected input clock misses 3 consecutive clock cycles. It is cleared once an active clock edge is detected.

For all DPLL1 and DPLL2 the occurrence of the fast loss will result in the DPLL to unlock if the FAST_LOS_SW bit is '1'. For DPLL3, the occurrence of the fast loss will result in the DPLL to unlock regardless of the FAST_LOS_SW bit.

3.3.4.2 Fine Phase Loss

The DPLL compares the selected input clock with the feedback signal. If the phase-compared result exceeds the fine phase limit programmed by the PH_LOS_FINE_LIMT[2:0] bits, a fine phase loss is triggered. It is cleared once the phase-compared result is within the fine phase limit.

For greatest jitter and wander tolerance, set the PH_LOS_FINE_LIMT[2:0] to the largest value..

The occurrence of the fine phase loss will result in DPLL to unlock if the FINE_PH_LOS_LIMT_EN bit is '1'.

3.3.4.3 Hard Limit Exceeding

Two limits are available for this monitoring. They are DPLL soft limit and DPLL hard limit. When the frequency of the DPLL output with respect to the system clock exceeds the DPLL soft / hard limit, a DPLL soft / hard alarm will be raised; the alarm is cleared once the frequency is within the corresponding limit. The occurrence of the DPLL soft alarm does not affect the DPLL locking status. The DPLL soft alarm is indicated by the corresponding DPLL_SOFT_FREQ_ALARM bit. The occurrence of the DPLL hard alarm will result in the DPLL to unlock if the FREQ_LIMT_PH_LOS bit is '1'.

The DPLL soft limit is set by the DPLL_FREQ_SOFT_LIMT[6:0] bits and can be calculated as follows:

$$DPLL\ Soft\ Limit\ (ppm) = DPLL\_FREQ\_SOFT\_LIMT[6:0]\ X\ 0.724$$

The DPLL hard limit is set by the DPLL_FREQ_HARD_LIMT[15:0] bits and can be calculated as follows:

$$DPLL\ Hard\ Limit\ (ppm) = DPLL\_FREQ\_HARD\_LIMT[15:0]\ X\ 0.0014$$

3.3.4.4 Locking Status

The DPLL locking status depends on the locking monitoring results. The DPLL is in locked state if none of the following events is triggered during 2 seconds; otherwise, the DPLL is unlocked.

- Fast Loss (the FAST_LOS_SW bit is '1');
- Fine Phase Loss (the FINE_PH_LOS_LIMT_EN bit is '1');
- DPLL Hard Alarm (the FREQ_LIMT_PH_LOS bit is '1').

If the FAST_LOS_SW bit, the COARSE_PH_LOS_LIMT_EN bit, the FINE_PH_LOS_LIMT_EN bit or the FREQ_LIMT_PH_LOS bit is '0', the DPLL locking status will not be affected even if the corresponding event is triggered. If all these bits are '0', the DPLL will be in locked state in 2 seconds.

The DPLL locking status is indicated by the corresponding DPLL_LOCK bits and by the DPLL_LOCK pins.

3.3.4.5 Phase Lock Alarm

DPLL1 and DPLL2 have a phase lock alarm that will be raised when the selected input clock can not be locked in DPLL1/2 within a certain period. This period can be calculated as follows:

$$Period\ (sec.) = TIME\_OUT\_VALUE[5:0]\ X\ MULTI\_FACTOR[1:0]$$

The phase lock alarm is indicated by the corresponding INn_PH_LOCK_ALARM bit ($6 \geq n \geq 1$).

The phase lock alarm can be cleared, as selected by the PH_ALARM_TIMEOUT bit:

- It is cleared when a '1' is written to the corresponding INn_PH_LOCK_ALARM bit;
- It is cleared after the period ($= TIME\_OUT\_VALUE[5:0]\ X\ MULTI\_FACTOR[1:0]\ in\ second$) starting from the time the alarm is raised.

The selected input clock with a phase lock alarm is disqualified for the DPLL1 and DPLL2 to lock.

Note that phase lock alarm is not available for DPLL3.

3.3.5 APLL

APLL is provided for a better jitter and wander performance of the device output clocks. The bandwidth for the APLL is internally set to 22 kHz (typical).

The input of the APLL can be derived from one of the DPLL1 or DPLL2 outputs, as selected by the apll_path_freq_cnfg[2:0] bits respectively as shown in Table 10.

Table 10: APLL input selection

apll_path_freq_cnfg[2:0]	APLL Input Selection
000	622.08 MHz from DPLL1
001	625 MHz from DPLL1
010	644.53125 MHz from DPLL1
011	Reserved
100	622.08 MHz from DPLL2
101	625 MHz from DPLL2
110	644.53125 MHz from DPLL2
1111	Reserved

The following steps should be followed to set the APLL output to Ethernet LAN PHY frequencies.

To initialize the device, write into the following registers:

1. Write 0x04F4F0 to bits apll_divn_frac_cnfg[20:0] of the APLL-fractional feedback divider configuration register to set the fractional part of feedback divider for the APLL.
2. Write 0x0051 to bits apll_divn_den_cnfg[15:0] of the APLL divisor denominator configuration register to set the denominator part of feedback divider for the APLL.
3. Write 0x0010 to bits apll_divisor_num_cnfg[15:0] of the APLL divisor numerator configuration register to set the numerator part of feedback divider for the APLL.
4. Write 0x21 to bits apll_divisor_int_cnfg[5:0] of the APLL divisor integer configuration register to set the integer part of feedback divider for the APLL.
5. Write 0x13356218 to bits apll_fr_ratio_cnfg[28:0] of the APLL feedback divider configuration register to set the feedback divider for the APLL.

After the device has been initialized according to the steps above, follow the following steps when setting the APLL path to 644.53125 MHz:

- Write 1'b1 to dsm_cnfg_en bit to enable the preset programmable feedback divider of the APLL configuration register
- Write the corresponding value in the apll_path_freq_cnfg[2:0] bits according to Table 10.

After the device has been initialized according to the steps 1 to 5 above, follow the following steps when setting the APLL path to 625MHz: or 622.08MHz

- Write 1'b0 to dsm_cnfg_en bit to disable the preset programmable feedback divider of the APLL configuration register
- Write the corresponding value in the apll_path_freq_cnfg[2:0] bits according to Table 10.

3.3.5.1   EXTERNAL FILTER

It is recommended to use external filter component for better noise suppression. The filter components are connected to VC pin. Choosing the correct external components and having a printed circuit board (PCB) layout is a key task for quality operation of the APLL external filter option. Figure 21 shows the APLL external filter components, and Table 11 shows the recommended values for Rs, Cs and Cp. The device has been characterized using these parameters. The external loop filter components should be kept as close as possible to the device. Loop filter traces should be kept short. Other signal traces should be kept separated and not run underneath the device, and loop filter components.

Table 11: APLL filter components

VC Filter Pin	Rs (Ω)	Cs (uF)	Cp (pF)
External component	220	1	470
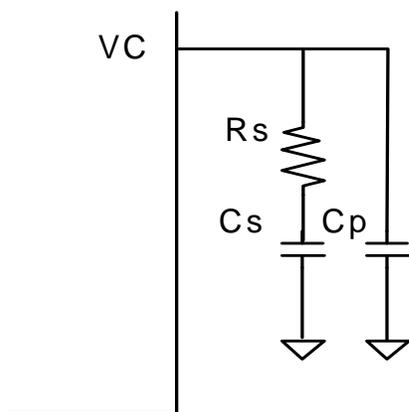
Figure 21. APLL External Filter

3.3.6   OUTPUT CLOCKS & FRAME SYNC SIGNALS

The device supports 7 output clocks and 2 frame sync output signals.

3.3.6.1   Output Clocks

OUT1 can be derived either from DPLL1, DPLL2, or from the APLL selected by out1_mux_cnfg[3:0].

OUT2 ~ OUT4 can be derived from APLL.

OUT5 can be derived either from DPLL1 or DPLL2.

OUT1 to OUT5 have an output divider associated with each output. The divider is composed by 2 cascaded dividers, the first divider can be programmed by writing into OUTn_DIV1_CNFG[4:0], the second divider can be programmed by writing into OUTn_DIV2_CNFG[26:0].

Figure 22 shows the diagram for OUT1 and OUT5 output dividers and relevant register bits.
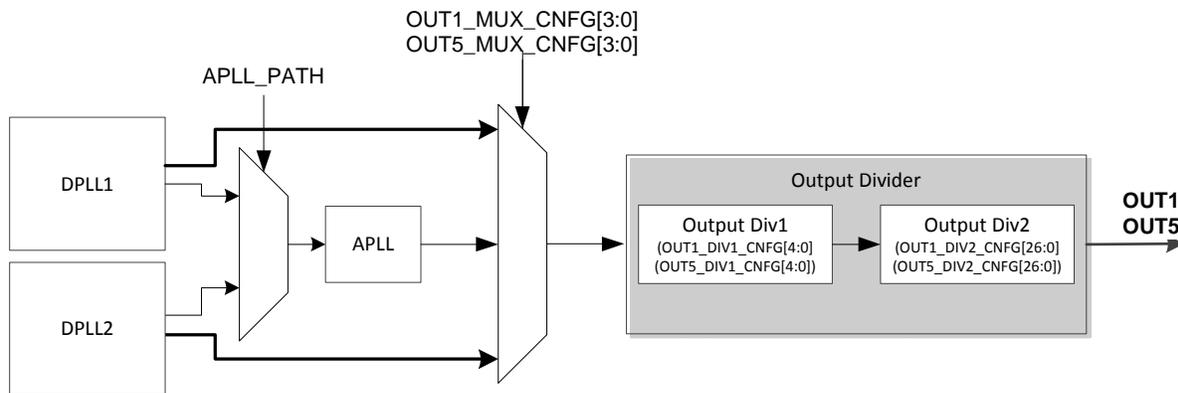
Figure 22. OUT1 and OUT5 output dividers

Figure 23 shows the diagram for OUT2 to OUT4 output dividers and relevant register bits.
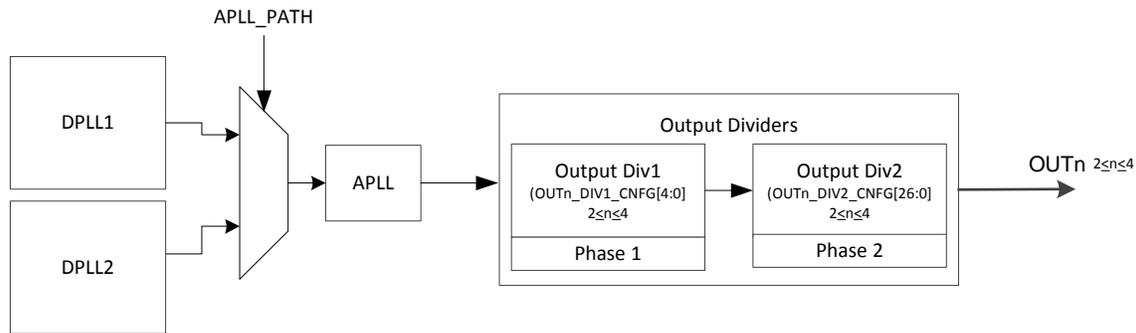
Figure 23. OUT2 to OUT4 output dividers

OUT6 and OUT7 are derived from DPLL3, there is an output divider associated with it. A GUI (Time Commander) can be used to set the following bis in the respective register that are associated with the DPLL3 dividers.

- To set the feedback divider, program dpll3_fb_div_cnfg[13:0] bits of DPLL3 feedback divider register
- To set the fractional divider, program dpll3_divn_frac_cnfg[23:0] of DPLL3 fractional divider register
- To set the denominator of the fractional divider, program dpll3_divn_den_cnfg[15:0] bits of DPLL3 fractional divider denominator register
- To set the numerator of the fractional divider, program dpll3_divn_num_cnfg[15:0] bits of DPLL3 fractional divider numerator register
- To set the integer divider, program dpll3_int_cnfg[7:0]bits of DPLL3 integer divider register

OUT1 to OUT7 output clocks can be inverted by setting OUTn_IN-VERT bit (0: output not inverted, 1: output inverted) in OUTn_MUX-_CNFG register for (1 $\leq$ n $\leq$ 5), and in OUT6_CNFG and OUT7_CNFG registers for OUT6 and OUT7 respectively.

The output clocks can be squelched by setting OUTn_SQUELCH[1:0] bits (0x: no squelch, 10: squelch to '0', 11: squelch to '1') in OUTn_MUX_CNFG register for (1 $\leq$ n $\leq$ 5), and in OUT6_CNFG and OUT7_CNFG registers for OUT1 to OUT5, and OUT6 and OUT7 respectively.

OUT1 to OUT5 output clocks can be individually powered down by setting OUTn_PDN bit to '1' in OUTn_MUX_CNFG register for (1 < n < 5)

82P33813 provides a variety of output frequencies from 1Hz to 650MHz.

The APLL is always enabled and the default frequency for OUT1, OUT2, and OUT3 is respectively 25 MHz, 125 MHz, and 156.25MHz.

By default, OUT 4 and OUT5 are squelched. Set the proper registers to set desired frequency values for OUT 3 and OUT5.

DPLL3 is disabled by default, and if it is enabled, then the default frequency for OUT6 and OUT7 is respectively 16.384 MHz and 2.048 MHz.

The APLL and the DPLLs can be configured from an external EEPROM after reset. It can be used to set specific start up frequency values as needed by the application.

3.3.6.2   Frame Sync Signals

Either an 8 kHz or a 2 kHz frame sync, or a 1PPS sync signal are output on the FRSYNC_8K_1PPS and MFRSYNC_2K_1PPS pins if enabled by the 8K_1PPS_EN and 2K_1PPS EN bits respectively. They are CMOS outputs.

The output sync frequencies are independent of the input sync frequency. The output FRSYNC_8K_1PPS and MFRSYNC_2K_1PPS frequencies are selected through the dpll1/2_fr_mfr_sync_cnfg registers.

Any supported clock frequency at the clock input can be associated with the sync signals.

The frame sync output signals are derived from the DPLL1 and DPLL2 output and are aligned with the output clock. They are synchronized to the frame sync input signal. In DCO control modes (section 3.3.2.1), the output FRSYNC_8K_1PPS and MFRSYNC_2K_1PPS must not be used, a 1PPS output sync signal can be generated in any of the output clocks connected to the DCO being used.

The frame/sync output signals align to the first edge of the associated reference clock that occurs after the edge of the frame/sync input signal. The frequency of the associated reference clock must be lower or equal to the frequencies of the output clocks that requires to be aligned with the frame/sync pulse signal.

If the frame sync input signal with respect to the DPLL1/2 selected input clock is above a limit set by the SYNC_MON_LIMT[2:0] bits, an external sync alarm will be raised and the frame/sync input signal is disabled to synchronize the frame/sync output signals. The external sync alarm is cleared once the frame/sync input signal with respect to the DPLL selected input clock is within the limit. If it is within the limit, whether frame/sync input signal is enabled to synchronize the frame sync output signal is determined by the AUTO_EXT_SYNC_EN bit and the EXT_SYNC_EN bit.

When the frame/sync input signal is enabled to synchronize the frame/sync output signal, it is adjusted to align itself with the DPLL selected input clock. The selected input reference divider should be set

to 1, so the FRSYNC and MFRSYNC will be aligned to the first clock input edge following the SYNC/frame signal input.

By default, the falling edge of the frame/sync input signal is aligned with the rising edge of the DPLL1/2 selected input clock. The rising edge of frame/sync input signal can be set to be aligned with the rising edge of the DPLL1/2 selected input clock by setting sync_edge bit to "1" in DPLL1/2_sync_edge_cnfg register.

The EX_SYNC_ALARM_MON bit indicates whether frame/sync input signal is in external sync alarm status. The external sync alarm is indicated by the EX_SYNC_ALARM bit. If the EX_SYNC_ALARM bit is '1', the occurrence of the external sync alarm will trigger an interrupt.

The 8 kHz frame pulse, the 2 kHz frame pulse, and the 1PPS sync signal can be inverted by setting the 8K_1PPS_INV and 2K_1PPS_INV bits of Frame Sync and Multiframe Sync Output Configuration Register.

The 8 kHz and the 2 kHz frame sync outputs can be 50:50 duty cycle or pulsed, as determined by the 8K_PUL and 2K_PUL bits respectively. When they are pulsed, the pulse width derived from DPLL1 is defined by the period of OUT1, and the pulse width derived from DPLL2 is defined by the period of OUT5. They are pulsed on the position of the falling or rising edge of the standard 50:50 duty cycle, as selected by the 2K_8K_PUL_POSITION bit of Frame Sync and Multiframe Sync Output Configuration Register.

3.3.7 INPUT AND OUTPUT PHASE CONTROL

The device has several features to allow a tight control of the phase on the input and output clocks.

3.3.7.1 DPLL1 and DPLL2 Phase offset control

The phase offset of the DPLL1/2 selected input clock with respect to the DPLL1/2 output can be adjusted. If the device is configured as the active PLL in a redundancy system, then the PH_OFFSET_EN bit determines whether the input-to-output phase offset is enabled. If the device is configured as the inactive PLL in a redundancy system, then the input-to-output phase offset is always enabled. If enabled, the input-to-output phase offset can be adjusted by setting the PH_OFFSET_CNFG[28:0] bits in DPLL1/2 phase offset configuration register. The register value is a 2's complement phase offset with a resolution of 0.0745ps and a total range of [20us, - 20us].

The input-to-output phase offset can be calculated as follows:
Phase Offset (ps) = PH_OFFSET[28:0] X 0.0745

3.3.7.2 Input Phase control

All the inputs phase can be controlled individually. They can be programmed with a resolution of 0.61 ns and a range of [77.5 ns,-78.1ns] by setting INn_PHASE_OFFSET_CNFG[7:0] bits ($1 \leq n \leq 6$) in the input phase offset configuration register. The register value is a 2's complement phase offset, the default is zero. The programmed offset is automatically applied to the DPLL1 and DPLL2 when a particular input is

selected. If the manual DPLL1 and DPLL2 phase offset control is used then the per-input phase offset is not applied.

3.3.7.3 Output Phase control

The output phase can be controlled individually for outputs OUT1 to OUT5. There is the coarse phase control that allows the output phase to be adjusted as low as 1.6ns. There is a fine phase adjustment that allows the output phase to be adjusted as low as 187.27 ps. The total range is +/-180°.

There are two registers associated with the coarse phase adjustment, the OUTn_PH1_CNFG ($1 \leq n \leq 5$) and the OUTn_PH2_CNFG ($1 \leq n \leq 5$) registers. The OUTn_PH1_CNFG register is associated with output divider 1 as shown in Figure 22 and Figure 23, the phase can be adjusted by a step size that is equal to the period of the input of clock of the output Div1, the number set in the OUTn_PH1_CNFG register should not be larger than the number set in OUTn_DIV1_CNFG register. The OUTn_PH2_CNFG register is associated with output divider 2 as shown in Figure 22 and Figure 23, the phase can be adjusted by a step size that is equal to the period of the input of clock of the output Div2, the number set in the OUTn_PH2_CNFG register should not be larger than the number set in OUTn_DIV2_CNFG register.

There is a register that is associated with the fine phase adjustment, the OUTn_FINE_CNFG ($1 \leq n \leq 4$). For the fine phase adjustment, the output clocks must be output from the APLL, The phase can be adjusted by a step size that is equal to the 1/2 of the period of the VCO. For Ethernet clocks the VCO frequency is 2.5GHz, for Ethernet LAN PHY the VCO frequency is 2.578125 GHz, and for SONET/SDH clocks the VCO frequency is 2.48832 GHz. OUT1 can be output from the DPLLs, and in that case the fine phase adjustment is not available, it is only available if the clocks are output from the APLL.

The output phase adjustments are not available for OUT6 and OUT7.

3.3.8 TIME OF DAY COUNTER

The device has 2 time accumulators that keeps track of the local Time of Day (ToD). The time accumulators are associated with DPLL1 and DPLL2. The time accumulator runs on the 77.76 MHz clock that is generated by the DCO1/2. By using the DCO clock, the Time of Day tracks the input clock or packet stream that the DPLL is locked to and is also synchronized to the output clocks and the output 1 PPS signal generated from the same DPLL.

In order to synchronize the device Time of Day with the Time of Day in the IEEE 1588 server, the device has several triggers available. These can be used to select on which trigger the time accumulator can be synchronized to a pre-programmed value. An internal timer allows to update and sample the Time of Day at fixed intervals timed on the local oscillator.

The time accumulator records the Time of Day in PTP format: 48-bit seconds, and 32-bit ns.

4 POWER SUPPLY FILTERING TECHNIQUES

To achieve optimum jitter performance, power supply filtering is required to minimize supply noise modulation of the output clocks. The common sources of power supply noise are switch power supplies and the high switching noise from the outputs to the internal PLL. The 82P33813 provides separate VDDA and VDDAO power pins for the internal analog PLL, it also provides VDDD and VDDDO pins for the core logic as well as I/O driver circuits.

The suggested power decoupling scheme is shown in Figure 24.

VCC3V3   40, 42   VDDD
0.1uF   0.1uF   10uF   0.1uF
                                                         VSS
                                                ePAD
One 0.1uF
per pin

VCC1V8   42, 53   VDDD_1P8
0.1uF   0.1uF   10uF   0.1uF
                                                         VSS
                                                ePAD
One 0.1uF
per pin

VCC3V3   27, 29, 64, 66   VDDDO
0.1uF   0.1uF   10uF   0.1uF
                                                         VSS
                                                ePAD
One 0.1uF
per pin

VCC3V3   2, 3, 4, 5, 10 11, 12 VDDA
0.1uF   0.1uF   10uF   0.1uF
                                                         VSS
                                                ePAD
One 0.1uF
per pin

VCC3V3   20, 24, 69, 72   VDDAO
0.1uF   0.1uF   10uF   0.1uF
                                                         VSSAO
                                            19, 23, ePAD
One 0.1uF
per pin
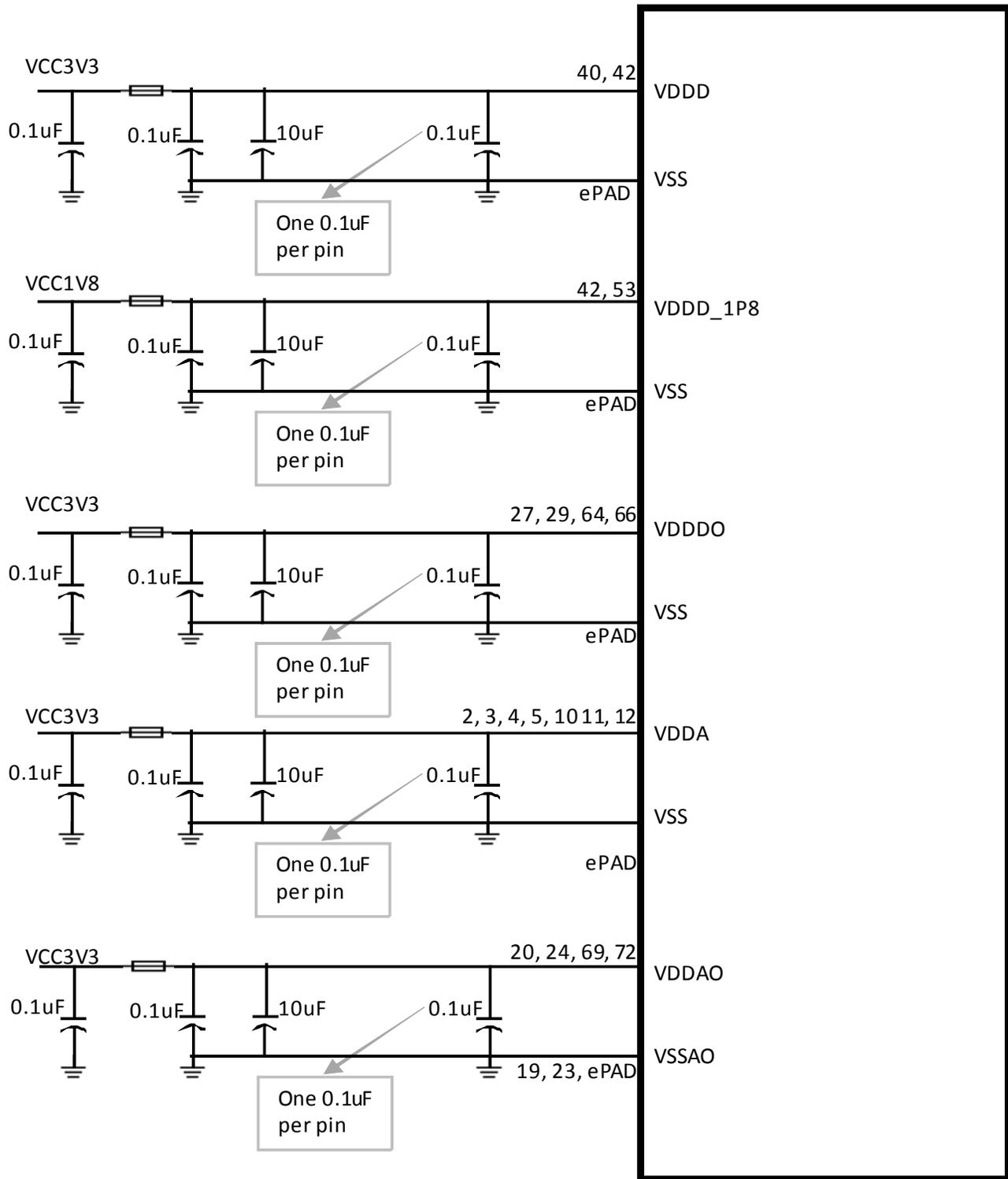
Figure 24. 82P33813 Power Decoupling Scheme

5 MICROPROCESSOR INTERFACE

The microprocessor interface provides access to read and write the registers in the device. The microprocessor interface supports I2C.

5.1 I2C SLAVE MODE

5.1.1 I2C DEVICE ADDRESS

The default value for the higher 4-bit address is 4'b1010, the 3-bit address is set by pins I2C_AD2, I2C_AD1, and I2C_AD0.

5.1.2 I2C BUS TIMING

Figure 25 shows the definition of I2C bus timing.

Figure 25. Definition of I2C Bus Timing

Table 12: Timing Definition for Standard Mode and Fast Mode[1]

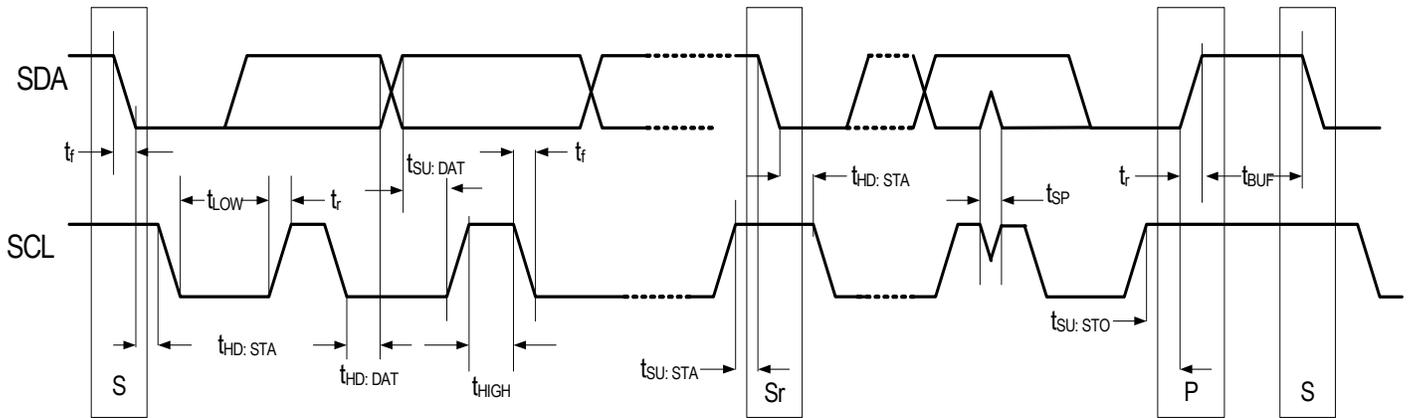| Symbol	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
SCL	Serial clock frequency	0	100	0	400	kHz
$t_{HD; STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	-	0.5	-	µs
t_{LOW}	LOW period of the SCL clock	4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock	4.0	-	0.6	-	µs
$t_{SU; STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	µs
$t_{HD; DAT}$	Data hold time: for CBUS compatible masters for I^{2}C-bus devices	5.0 0[2]	- 3.45[3]	- 0[2]	- 0.9[3]	µs
$t_{SU; DAT}$	Data set-up time	250	-	100[4]	-	ns
t_r	Rise time of both SDA and SCL signals	-	1000	20 + 0.1Cb[5]	300	ns
t_f	Fall time of both SDA and SCL signals	-	300	20 + 0.1Cb[5]	300	ns
$t_{SU; STO}$	Set-up time for STOP condition	4.0	-	0.6	-	µs
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF
V_{nL}	Noise margin at the LOW level for each connected device (Including hysteresis)	0.1VDD	-	0.1VDD	-	V
V_{nH}	Noise margin at the HIGH level for each connected device (Including hysteresis)	0.2VDD	-	0.2VDD	-	V
t_{sp}	Pulse width of spikes which must be suppressed by the input filter	0	50	0	50	ns

Note:
1. All values referred to V_{IHmin} and V_{ILmax} levels (see Table 23)
2. A device must Internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum $t_{HD; DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. A Fast-mode I^{2}C-bus device can be used in a Standard-mode I^{2}C-bus system, but the requirement $t_{SU; DAT} \geqslant$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU; DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^{2}C-bus specification) before the SCL line is released.
5. C_b = total capacitance of one bus line in pF. If mixed with Hs-mode device, faster fall-times according to Table 24 allowed.
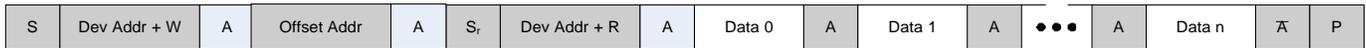n/a = not applicable

5.1.3 SUPPORTED TRANSACTIONS

The supported types of transactions are shown below.

Figure 26. I2C Slave Interface Supported Transactions

Table 13: Description of I2C Slave Interface Supported Transactions

Operation	Description
Current Read	Reads a burst of data from an internal determined starting address, this starting address is equal to the last address accessed during the last read or write operation, incremented by one. If the address exceeds the address space, it will start from 0 again.
Sequential Read	Reads a burst of data from a specified address space. The starting address of the space is specified as offset address.
Sequential Write	Writes a burst of data to a specified address space, the starting address of the space is specified as offset address.

The registers are divided up into pages of 128 bytes with each byte having a separate address. Multi-byte registers need to be accessed in multiple read/write cycles. Address 0x7F is reserved for the page index pointer.

All register accesses are done as 8 bit I2C cycles. The 8-bit address refers to the register offset within the active page. If access to a different page is needed then a separate I2C write must be performed to the page register (0x7F). This makes the new page active and then 8 bit reads and writes can be performed anywhere within that page.

Note that accesses to multi-byte registers should not be interrupted by accesses to other addresses, because that may cause the data to be corrupted. The access of the multi-byte registers is different from the single-byte registers. Take the DPLL1 priority table registers (00H and 01H in page 2) as an example, the write operation for the multi-byte registers follows a fixed sequence. The register (00H) is configured first and the register (01H) is configured last. The two registers are configured continuously and should not be interrupted by any operation. The DPLL1 priority table configuration will take effect after all the two registers are configured. During read operation, the register (00H) is read first and the register (01H) is read last. The priority table configuration register reading should be continuous and not be interrupted by any operation.

5.2 I2C MASTER MODE

The 82P33813 has the capability to read from an external I2C EEPROM upon exit from reset. This reduces the start-up load on the microprocessor by programming the registers in the device-address space 101_0xxx. This mode uses the MPU_MODE1/I2CM_SCL and the MPU_MODE0/I2CM_SDA pins as the serial clock and the serial data respectively, it requires that both these pins be pulled high through resistors (these resistor values are dependent on the bus capacitance and I2C speed of the application). Access to the 82P33813 registers through the microprocessor interface I2C serial port is not available until the EEPROM reading process is completed.

As an I^2C bus master, the 82P33813 will support the following:
- 8 kbit (1023 x 8) I2C EEPROM with device address 1010000 (for the base block)
- Sequential read (block read) of the entire memory-map for device, from byte-address 0x000 to 0x39E
- 7-bit device address mode
- Validation of the EEPROM read data via CCITT-8 CRC check against value stored in memory-map address 0x39E
- Support for 100kHz and 400kHz operation with speed programmability. If bit 7 is set at memory-map address 0x001, the 82P33813 will shift from 100kHz operation to 400kHz operation.
- 2-byte word-addressing (1-byte word addressing is supported by offsetting the memory-map upwards 1 address in the EEPROM)
- Read will abort with an alarm (RD_EEPROM_ERR interrupt status set) if any of the following conditions occur: Slave NACK, CRC failure, Slave Response time-out

As the 82P33813 I2C master bus is meant only to read from a single EEPROM, it has the following restrictions:

- No support for Multi-master
- No support for Slave clock stretching
- No support for I2C Start Byte protocol
- No support for EEPROM Chaining
- No support for Writing to external I2C devices including the EEPROM used for booting

5.2.1 I2C BOOT-UP INITIALIZATION MODE

EEPROM mode is enabled via setting the MPU_MODE[1:0] pins high (through two separate pull-up resistors). Once the RSTB input has been asserted (low) and then de-asserted (high) and the device internal calibration has been completed, the 82P33813 will perform a short block read at 100 kHz to program the EEPROM read speed (100 kHz or 400 kHz). The 82P33813 will then perform a block read to program all the device configuration registers, and check the CRC of the EEPROM data. During the boot-up EEPROM-reading process, the 82P33813 will not respond to microprocessor serial control port accesses. Once the initialization process is completed, the contents of any of the device configuration registers can be further altered by the microprocessor, if desired.

The 82P33813 can work with EEPROMs supporting 2-byte word-addresses or 1-byte word-addresses by using 2-byte word addressing for both. This works in the usual manner for EEPROMs supporting 2-byte word addresses, and gives an address-to-address match between EEPROM and memory-map. For EEPROMs supporting only 1-byte word addresses, the second address byte will cause an addition increment of the address counter, and the memory-map will be read at the next highest EEPROM address,.i.e memory-map (CSR) address 0x00 will be read from EEPROM address 0x01, and memory map address 0x39E will be read from EEPROM address 0x39F.

If a NACK is received to any of the read cycles performed by the 82P33813 during the initialization process, or if the CRC does not match the one stored in memory-map address 0x39E, the boot process will be restarted. This restart can happen up to three times before an abort is declared and the RD_EEPROM_ERR interrupt status bit is set. Also on RD_EEPROM_ERR the MPU_MODE1/ I2CM_SCL and MPU_MODE0/ I2CM_SDA pins are both held low until the interrupt status bit is cleared or the device is reset. The suggested method for dealing with RD_EE-PROM_ERR is to externally set the MPU_MODE[1:0] pins to 00 and then reset the 82P33813 so that it will boot into I2C serial port mode.

After a successful EEPROM boot, the 82P33813 will stop toggling the MPU_MODE1/ I2CM_SCL and MPU_MODE0/I2CM_SDA pins, returning them to static high values, and the RD_EEPROM_DONE interrupt status bit will be set. The I2C serial port will now respond to microprocessor reads and writes to the appropriate I2C device address.

5.2.2 EEPROM MEMORY MAP NOTES

The EEPROM memory-map is the same as the control and status register (CSR) map with the following additions and constraints:

1. For EEPROMs supporting 2-byte word-address, the memory-map addresses are the same as the EPPROM addresses; for EEPROMs supporting 1-byte word-address, the memory-map addresses will by mapped to the next address in the EEPROM, i.e. memory-map address 0x00 will be read from EEPROM address 0x01, and memory-map address 0x39E will be read from EEPROM address 0x39F.

2. Memory-map address 0x001, bit 7 is the EEPROM read speed (0 for 100 kps, 1 for 400 kbps)

3. Memory-map address 0x39E is the CRC-8 of the memory-map from 0x000 to 0x39D (the standard CCITT CRC-8 with the data width and result width being 8; the polynomial is (0, 1, 2, 8) or "0x07"). NB: all memory-map addresses from 0x000 to 0x39d are included in the sequential calculation of CRC, including those not used in the CSR - it is recommend that data at unused addresses be set to 0x00.

4. Memory-map addresses 0x392 to 0x39D must be set to the default values shown in the CSR documentation.

5. The device address at memory-map address 0x00f must match the address set by the board.

6. Each memory-map address that is a multiple of 0x7F must contain the pointer to the next page of the CSR i.e

0x07f	0x01
0x0ff	0x02
0x17f	0x03
0x1ff	0x04
0x27f	0x05
0x2ff	0x06
0x37f	0x07

5.3 SERIAL MODE

In a read operation, the active edge of SCLK is selected by CLKE. When CLKE is asserted low, data on SDO will be clocked out on the ris-ing edge of SCLK. When CLKE is asserted high, data on SDO will be clocked out on the falling edge of SCLK.

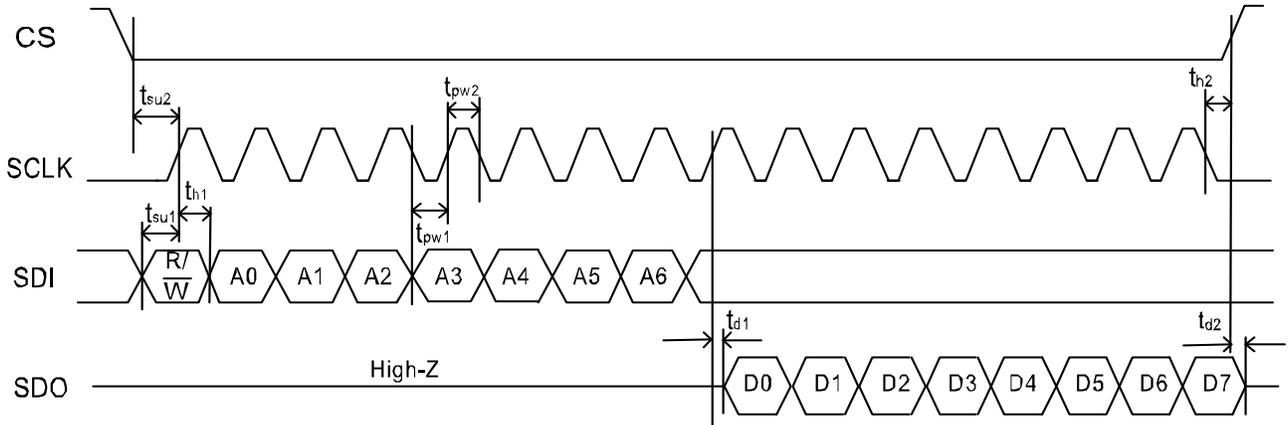In a write operation, data on SDI will be clocked in on the rising edge of SCLK.

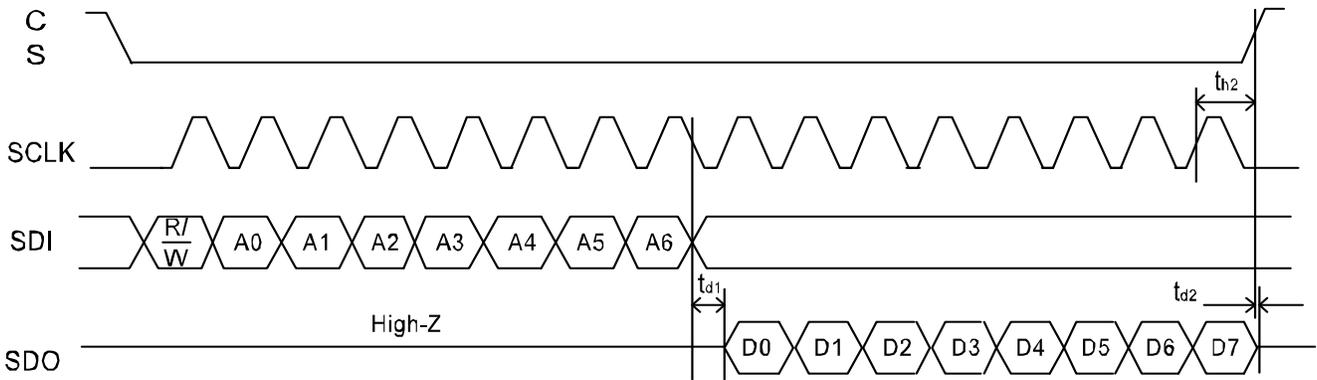**Figure 27. Serial Read Timing Diagram (CLKE Asserted Low)**

Figure 28. Serial Read Timing Diagram (CLKE Asserted High)

Table 14: Read Timing Characteristics in Serial Mode

Symbol	Parameter	Min	Typ	Max	Unit
T	One cycle time of the master clock		12.86		ns
t_{in}	Delay of input pad		5		ns
t_{out}	Delay of output pad		5		ns
t_{su1}	Valid SDI to valid SCLK setup time	4			ns
t_{su2}	Valid CS to valid SCLK setup time	14			ns
t_{d1}	Valid SCLK to valid data delay time		10		ns
t_{d2}	CS rising edge to SDO high impedance delay time		10		ns
t_{pw1}	SCLK pulse width low	5T+10			ns
t_{pw2}	SCLK pulse width high	5T+10			ns
t_{h1}	Valid SDI after valid SCLK hold time	6			ns
t_{h2}	Valid CS after valid SCLK hold time (CLKE = 0/1)	5			ns
t_{TI}	Time between consecutive Read-Read or Read-Write accesses (CS rising edge to CS falling edge)	10			ns
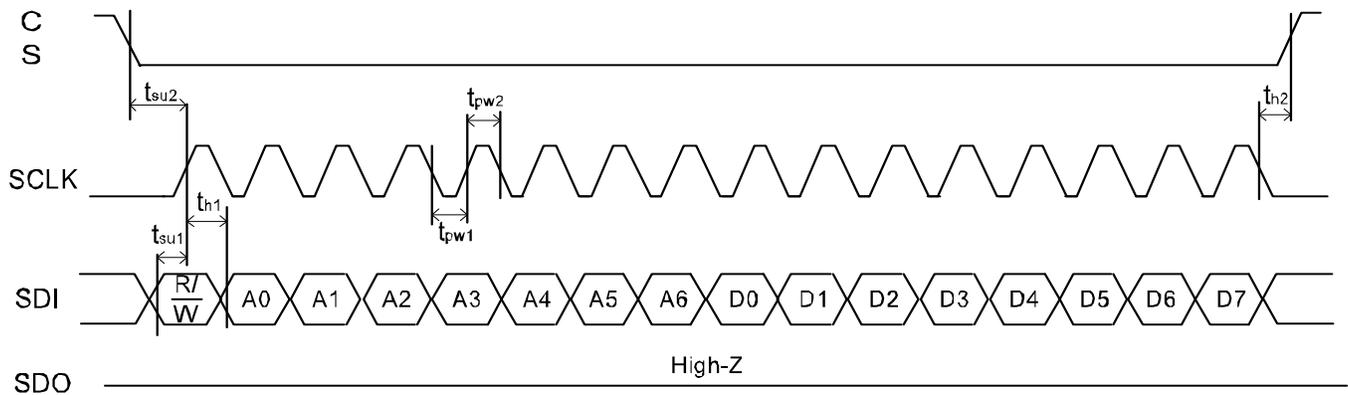
Figure 29. Serial Write Timing Diagram

Table 15: Write Timing Characteristics in Serial Mode

Symbol	Parameter	Min	Typ	Max	Unit
T	One cycle time of the master clock		12.86		ns
t_{in}	Delay of input pad		5		ns
t_{out}	Delay of output pad		5		ns
t_{su1}	Valid SDI to valid SCLK setup time	4			ns
t_{su2}	Valid CS to valid SCLK setup time	14			ns
t_{pw1}	SCLK pulse width low	5T+10			ns
t_{pw2}	SCLK pulse width high	5T+10			ns
t_{h1}	Valid SDI after valid SCLK hold time	6			ns
t_{h2}	Valid CS after valid SCLK hold time	5			ns
t_{TI}	Time between consecutive Write-Write or Write-Read accesses (CS rising edge to CS falling edge)	10			ns

5.4 UART MODE

When the 82P33813 comes out of reset with the MPU_MODE[1:0] pins set to 'b10, or when the boot-up EEPROM sets the mpu_sel_cnfg[1:0] bits to 'b10, the device will set its serial port mode to support simple 2-pin UART (Universal Asynchronous Receiver / Transmitter) communications. The UART_RX pin is used as the receive data, (data into the device), and the UART_TX pin is used as the transmit data, (data out of the device). The supported byte-protocol is 1 Start bit, 8 data bits, and 1 Stop bits, with no parity. Figure 30 shows the UART data frame.
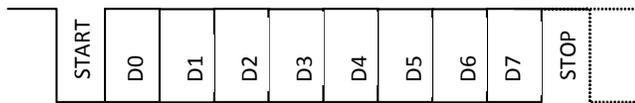

Figure 30. UART Data Frame

The falling edge of the Start bit is used to synchronize the UART receiver with the transmitter of the micro-controller; each bit is sampled at the expected midpoint as determined by this falling edge and the programmed baud rate.

The baud rate is programmed using the two control registers: baud_rate_cnfg, and baud_limit_cnfg. These registers set up an M/N divider from the 82P33813 system clock rate (77.76 MHz) down to the desired sample-clock rate, which must be 16 times the desired baud rate. The baud_freq_cnfg register is programmed with the M value, and the baud_limit_cnfg register is programmed with the value (N - M). These registers may be programmed by the boot-up EEPROM, or over the serial UART link. The new values take effect as soon as the UART goes idle, so it is recommended that all 4 bytes be written in one burst.

Example Baud rates:

9600 baud (default)
- Sample Clock Rate = 16 * 9600 = 153 600 Hz
- Sample Clock Rate = 77.76 MHz * 4/2025 = 153 600 Hz
- baud_freq_cnfg = 4 = x004
- baud_limit_cnfg = 2025 - 4 = 2021 = x07E5

115 200 baud
- Sample Clock Rate = 16 * 115 200 = 1 843 200 Hz
- Sample Clock Rate = 77.76 MHz * 16/675 = 1 843 200 Hz
- baud_freq_cnfg = 16 = x010
- baud_limit_cnfg = 675 - 16 = 659 = x293

Reads and writes of the 82P33813 control and status registers are performed through a multi-frame/byte binary protocol, which is more efficient than a character-oriented (hyper-terminal) protocol. The UART will auto-increment the internal address to support burst reads and writes for even higher efficiency.

5.4.1 PROTOCOL

Reads and writes are initiated by the micro-controller sending a command to the 82P33813. All commands start with a zero byte, followed by a command byte, 2 address bytes, and a length byte, which specifies the number of bytes to be written or read. Write commands then have a number of data bytes as given by the length byte. Commands are optionally acknowledged on completion.

Byte 1	Zero byte
Byte 2	Command byte
Byte 3	High Address byte (always zero)
Byte 4	Low Address byte
Byte 5	Length byte
Byte 6 to 5+Length	Write data bytes (if a write command)

The format of the command byte is given in Figure 16.

Table 16: UART Command byte Structure

Bit Number	Description
[7:6]	Not Used
[5:4]	Command: 2'b00 = NOP (sends ACK if requested) 2'b01 = Read 2'b10 = Write
[3:2]	Not Used
1	Address Auto-Increment: Set to 0 to enable address auto increment. Set to 1 to disable address auto increment.
0	Send ACK Flag: Set to 1 to send ACK byte at command completion.

Note that bursts cannot exceed the boundary of one register page (128 bytes), also the Address + Length should not reach the page register at the top of the register page (address 127 / x3F).

When the micro-controller sends a read command, or requests an acknowledge byte, the 82P33813 will transmit one of more bytes as follows:

Byte 1 to Length	Read Data bytes
Byte 'Length	'ACK byte (0x5A, if bit[0] of the Command byte was set]

Although the UART command contains a two-byte address, the 82P33813 will only use the Low Address byte. The UART can be set to expect a single byte address by clearing the uart_double_address bit in the baud_freq_cnfg[11:8] register. The command protocol can then leave out the High Address byte.

6 82P33813JTAG

This device is compliant with the IEEE 1149.1 Boundary Scan standard except the following:

- The output boundary scan cells do not capture data from the core and the device does not support EXTEST instruction;

The JTAG interface timing diagram is shown in Figure 31.
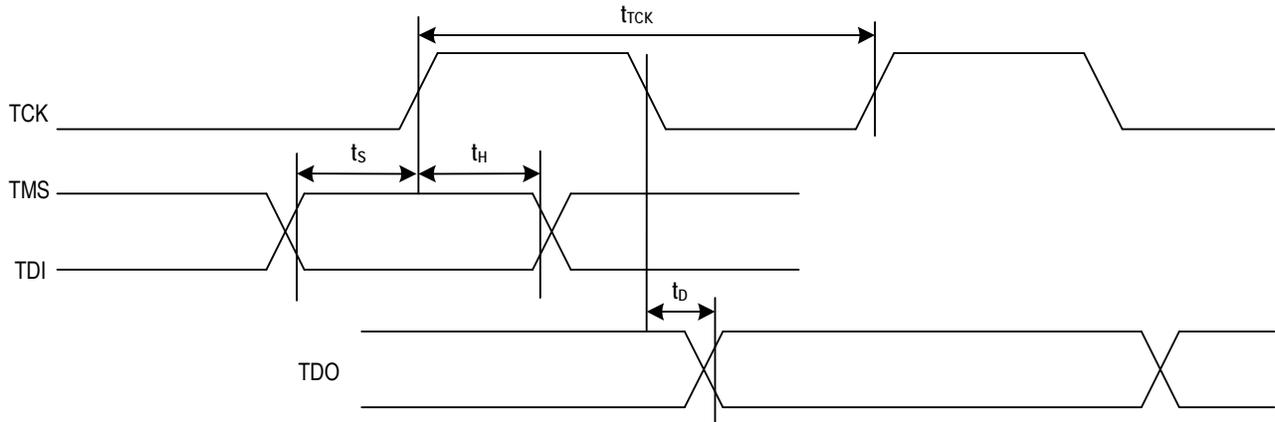
Figure 31. JTAG Interface Timing Diagram

Table 17: JTAG Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{TCK}	TCK period	100			ns
t_S	TMS / TDI to TCK setup time	25			ns
t_H	TCK to TMS / TDI Hold Time	25			ns
t_D	TCK to TDO delay time			50	ns

7 THERMAL MANAGEMENT

The device operates over the industry temperature range -40°C ~ +85°C. To ensure the functionality and reliability of the device, the maximum junction temperature T_{jmax} should not exceed 125°C. In some applications, the device will consume more power and a thermal solution should be provided to ensure the junction temperature T_j does not exceed the T_{jmax}.

7.1 JUNCTION TEMPERATURE

Junction temperature T_j is the temperature of package typically at the geographical center of the chip where the device's electrical circuits are. It can be calculated as follows:

Equation 1: $T_j = T_A + P \times \theta_{JA}$

Where:

θ_{JA} = Junction-to-Ambient Thermal Resistance of the Package

T_j = Junction Temperature

T_A = Ambient Temperature

P = Device Power Consumption

In order to calculate junction temperature, an appropriate θ_{JA} must be used. The θ_{JA} is shown in Table 18:

Table 18 has the thermal results based on JEDEC standard conditions. It is industry practice and IDT practice to publish these results.

If the PCB design differs from the JEDEC standard conditions, then the thermal results will be different.

7.2 THERMAL RELEASE PATH

In order to maximize both the removal of heat from the package, electrical grounding from the package to the board can be done through thermal vias to effectively conduct from the surface of the PCB to the ground plane(s). The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. These recommendations are to be used as a guideline only.

Table 18: Thermal Data

Parameter	Symbol	CONDITIONS	PKG	Typ Values (^{o}C/W)	Notes
Thermal Resistance	θ_{JC}	Junction to Case	QFN/NLG72	11.2	JEDEC PCB (7x7 matrix)
	θ_{JB}	Junction to Base		0.42	
	θ_{JA1}	Junction to Air, still air		20.75	
	θ_{JA2}	Junction to Air, 1 m/s air flow		17.05	
	θ_{JA3}	Junction to Air, 2 m/s air flow		15.66	
	θ_{JA4}	Junction to Air, 3 m/s air flow		14.96	

8 ELECTRICAL SPECIFICATIONS

8.1 ABSOLUTE MAXIMUM RATING

Table 19: Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit
V_{DDA}, V_{DDAO}, V_{DDDO}, V_{DDD}	Supply Voltage V_{DDA}, V_{DDAO}, V_{DDDO}, V_{DDD}	-0.5	3.6	V
$V_{DDD\_1\_8}$	Supply Voltage $V_{DDD\_1\_8}$	-0.5	1.98	V
V_{INCMOS}	Input Voltage (CMOS and Open drain pins)	-0.5	5.5	V
V_{INDIFF}	Input Voltage (Differential pins)	-0.5	V_{DDD}+ 0.5	V
V_{INAN}	Input Voltage (Analog pins)	-0.5	2.2	V
$I_{OUTCONT}$	Output Current (Continuous current)		50	mA
$I_{OUTSURGE}$	Output Current (Surge current)		100	mA
T_A	Ambient Operating Temperature Range	-40	85	°C
T_{STOR}	Storage Temperature	-50	150	°C
Note: CDM Classification - Class III (JESD22 - C101) HBM Classification - Class 2 (JS-001-2010)				

8.2 RECOMMENDED OPERATION CONDITIONS

Table 20: Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DDA}, V_{DDAO}, V_{DDDO}, V_{DDD}	Power Supply (DC voltage)	3.135	3.3	3.465	V	
$V_{DDD\_1\_8}$	Power Supply (DC voltage) $V_{DDD\_1\_8}$	1.71	1.8	1.89	V	
T_A	Ambient Temperature Range	-40		85	°C	
I_{DDA}	Analog Supply Current		327.75	361.90	mA	
I_{DDD}	Digital Supply Current (V_{DDD})		24.66	27.98	mA	
$I_{DDD\_1\_8}$	Digital Supply Current ($V_{DDD\_1\_8}$)		81.46	94.55	mA	
I_{DDDO}	Digital Output Supply Current		38.92	42.47	mA	All outputs enabled
I_{DDAO}	Analog Output Supply Current		152.13	170.93	mA	All outputs enabled, unloaded
	Analog Output Supply Current (loaded)		205.33	229.47	mA	All outputs enabled, 4 LVPECL outputs loaded with 150Ω to GND
P_{TOT}	Total Power Dissipation		1.94	2.28	W	All outputs enabled, excluding the loading
Note: 1. For lower power SMU configuration example, refer to Application Note AN-927.						

8.3 I/O SPECIFICATIONS

8.3.1 CMOS INPUT / OUTPUT PORT

Table 21: CMOS Input Port Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{IH}	Input Voltage High	2			V	
V_{IL}	Input Voltage Low			0.8	V	
I_{IN}	Input Current			±10	µA	

Table 22: CMOS Input Port with Internal Pull-Up Resistor Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{IH}	Input Voltage High	2			V	
V_{IL}	Input Voltage Low			0.8	V	
P_U	Pull-Up Resistor		50		KΩ	
I_{IN}	Input Current			±150	µA	

Table 23: CMOS Input Port with Internal Pull-Down Resistor Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{IH}	Input Voltage High	2			V	
V_{IL}	Input Voltage Low			0.8	V	
P_D	Pull-Down Resistor		50		KΩ	
I_{IN}	Input Current			±150	µA	

Table 24: CMOS Output Port Electrical Characteristics

Application Pin	Parameter	Description	Min	Typ	Max	Unit	Test Condition
Output Clock	V_{OH}	Output Voltage High	2.4		VDD	V	I_{OH} = -4 mA
	V_{OL}	Output Voltage Low			0.4	V	I_{OL} = 4 mA
	t_R	Rise time		2.2		ns	C_{LOAD} = 15 pF
	t_F	Fall time		2.2		ns	C_{LOAD} = 15 pF
Other Output	V_{OH}	Output Voltage High	2.4			V	I_{OH} = -2 mA
	V_{OL}	Output Voltage Low			0.4	V	I_{OL} = 2 mA
	t_R	Rise Time		7	20	ns	C_{LOAD} = 50 pF
	t_F	Fall Time		7	20	ns	C_{LOAD} = 50 pF

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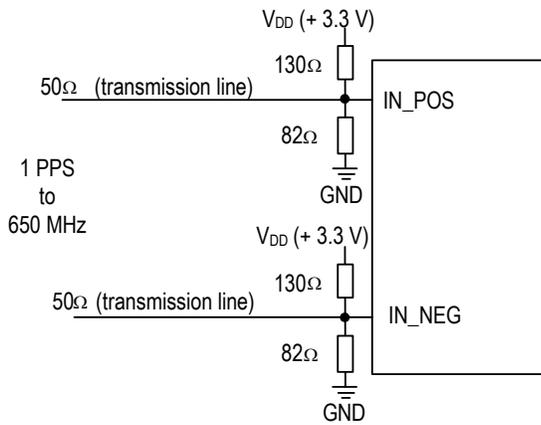### 8.3.2 LVPECL / LVDS INPUT / OUTPUT PORT

8.3.2.1 PECL Input Port

Figure 32. Recommended PECL Input Port Line Termination

Table 25: LVPECL Input Port Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{IL}	Input Low Voltage, Differential Inputs	VDD - 2.5	VDD - 1.5	VDD - 0.5	V	
V_{IH}	Input High Voltage, Differential Inputs	VDD - 2.4	VDD - 1.4	VDD - 0.4	V	
V_{ID}	Input Differential Voltage	0.1	0.7	1.4	V	
V_{IL_S}	Input Low Voltage, Single-ended Input	VSS	VDD - 1.95	VDD - 1.5	V	
V_{IH_S}	Input High Voltage, Single-ended Input	VDD - 1.3	VDD - 0.9	VDD	V	
I_{IH}	Input High Current, Input Differential Voltage V_{ID} = 1.4 V			10	μA	
I_{IL}	Input Low Current, Input Differential Voltage V_{ID} = 1.4 V	-10			μA	
Note: 1. Assuming a differential input voltage of at least 100 mV. 2. Unused differential input terminated to VDD-1.4 V.						

8.3.2.2   LVPECL Output Port

8.3.2.2.1   LVPECL Termination for 3.3 V

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figure 33 and Figure 34 show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.
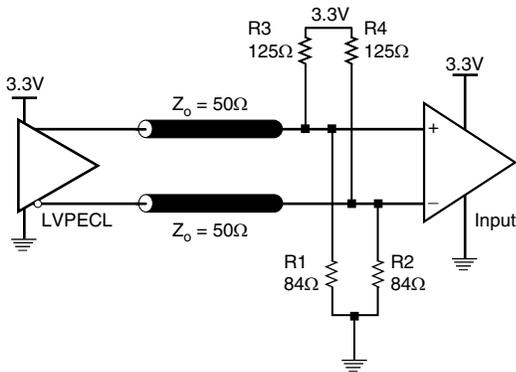

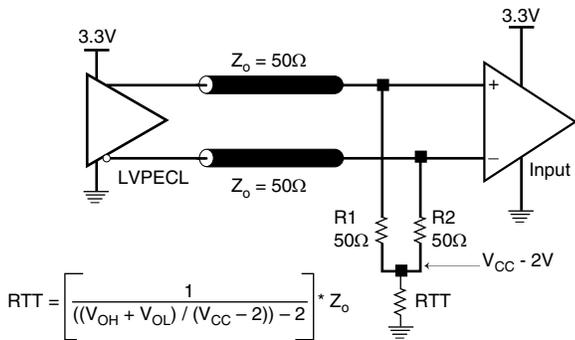**Figure 35. 2.5V LVPECL Output Termination**

Figure 33. 3.3V LVPECL Output Termination

Figure 36. 2.5V LVPECL Output Termination

$$RTT = \left[\frac{1}{((V_{OH} + V_{OL}) / (V_{CC} - 2)) - 2}\right] * Z_o$$

Figure 34. 3.3V LVPECL Output Termination

8.3.2.2.2   LVPECL Termination for 2.5 V

Figure 35 and Figure 36 show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to VCCO – 2V. For VCCO = 2.5V, the VCCO – 2V is very close to ground level. The R3 in Figure 36 can be eliminated and the termination is shown in Figure 37.
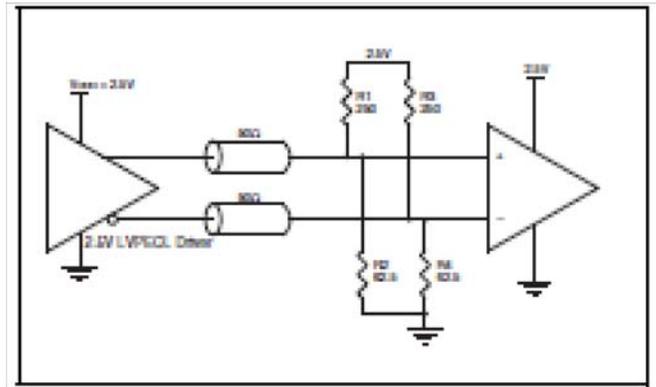

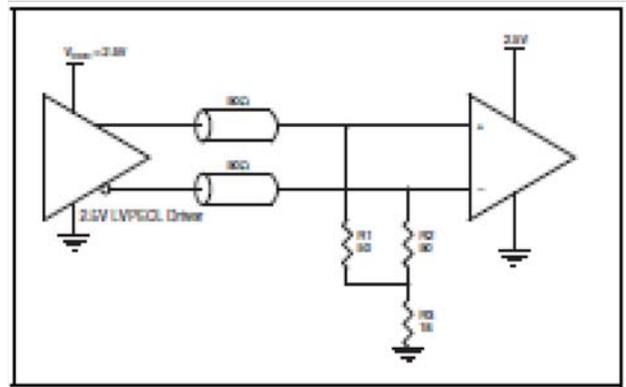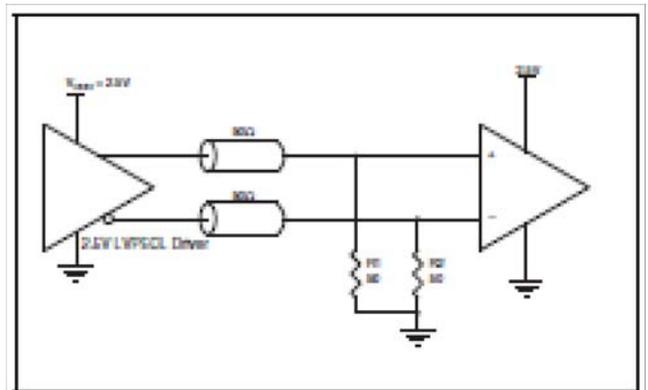**Figure 37. 2.5V LVPECL Output Termination**

Table 26: LVPECL Output Port Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{OH}	Output High Voltage; NOTE 1	$V_{CCO} - 1.3$		$V_{CCO} - 0.7$	V	
V_{OL}	Output Low Voltage; NOTE 1	$V_{CCO} - 2.0$		$V_{CCO} - 1.5$	V	
V_{SWING}	Peak-to-Peak Output Voltage Swing	0.6		1.0	V	
t_{RISE}/t_{FALL}	Output Rise/Fall time	80		400	ps	20% to 80%
NOTE 1: Outputs terminated with 50Ω to $V_{CCO} - 2V$						

8.3.3 LVDS INPUT / OUTPUT PORT

8.3.3.1 LVDS INPUT PORT

Figure 38. Recommended LVDS Input Port Line Termination

Table 27: LVDS Input Port Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{CM}	Input Common-mode Voltage Range	200	1200	2200	mV	
V_{DIFF}	Input Peak Differential Voltage	100	350	900	mV	
V_{IDTH}	Input Differential Threshold	-100		100	mV	
R_{TERM}	External Differential Termination Impedance		100		Ω	

8.3.3.2 LVDS Output Port

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (ZT) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage

source. The standard termination schematic as shown at the top part of Figure 39 can be used with either type of output structure. The termination schematic shown at the bottom part of Figure 39, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.
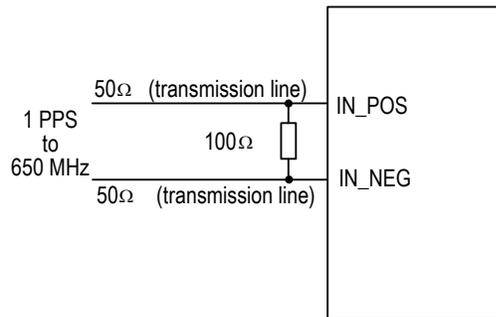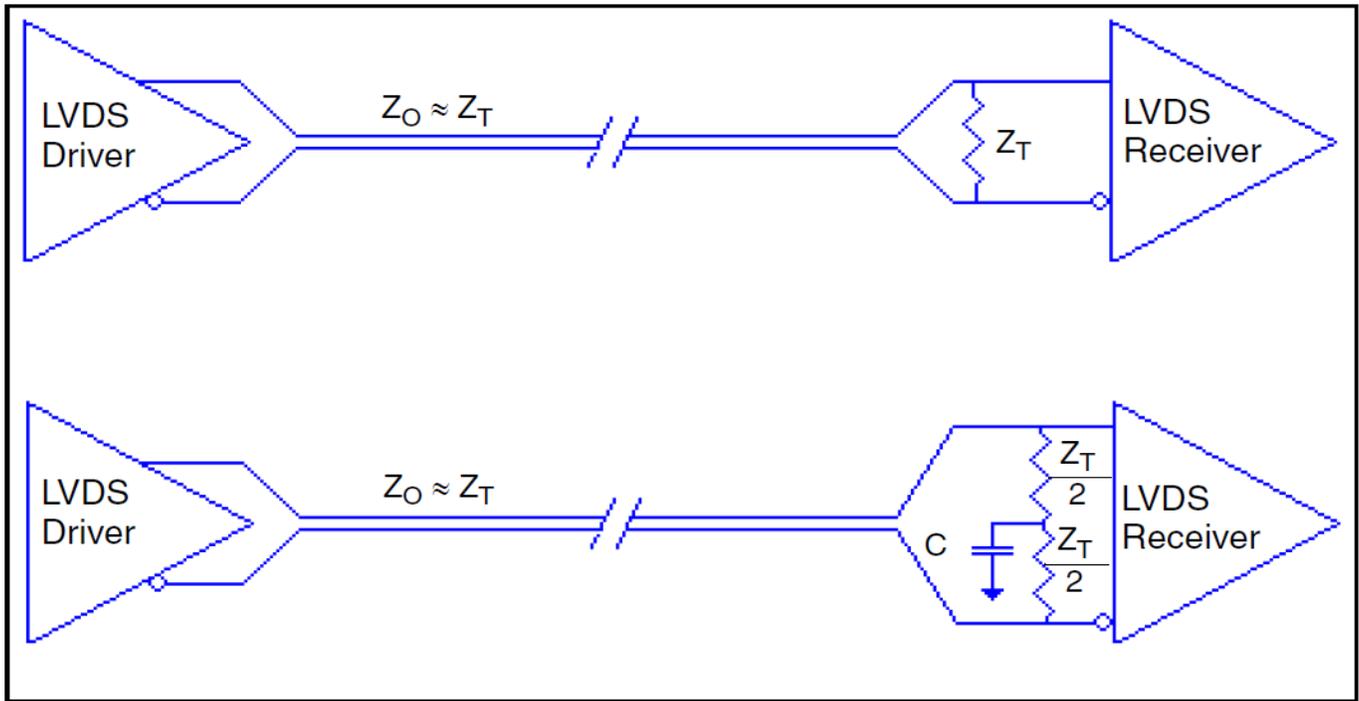

Figure 39. Recommended LVDS Output Port Line Termination

Table 28: LVDS Output Port Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{OD}	Differential Output Voltage	247		454	mV	
ΔV_{OD}	V_{OD} Magnitude Change			50	mV	
V_{OS}	Offset Voltage	1.125		1.375	V	
ΔV_{OS}	V_{OS} Magnitude Change			50	mV	
t_{RISE}/t_{FALL}	Output Rise/Fall time	90		400	ps	20% to 80%

8.3.4 OUTPUT CLOCK DUTY CYCLE

Table 29: Output Clock Duty Cycle

Clock Output Frequency	Min	Typ	Max	Unit	Test Condition
f_{OUT}<570MHz	45		55	%	
f_{OUT}≥570MHz	35		65	%	
NOTE: Output Duty Cycle configured using APLL.					

8.3.4.1 Single-Ended Input for Differential Input

Figure 40 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways.

First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Suggest edge rate faster than 1V/ns. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.
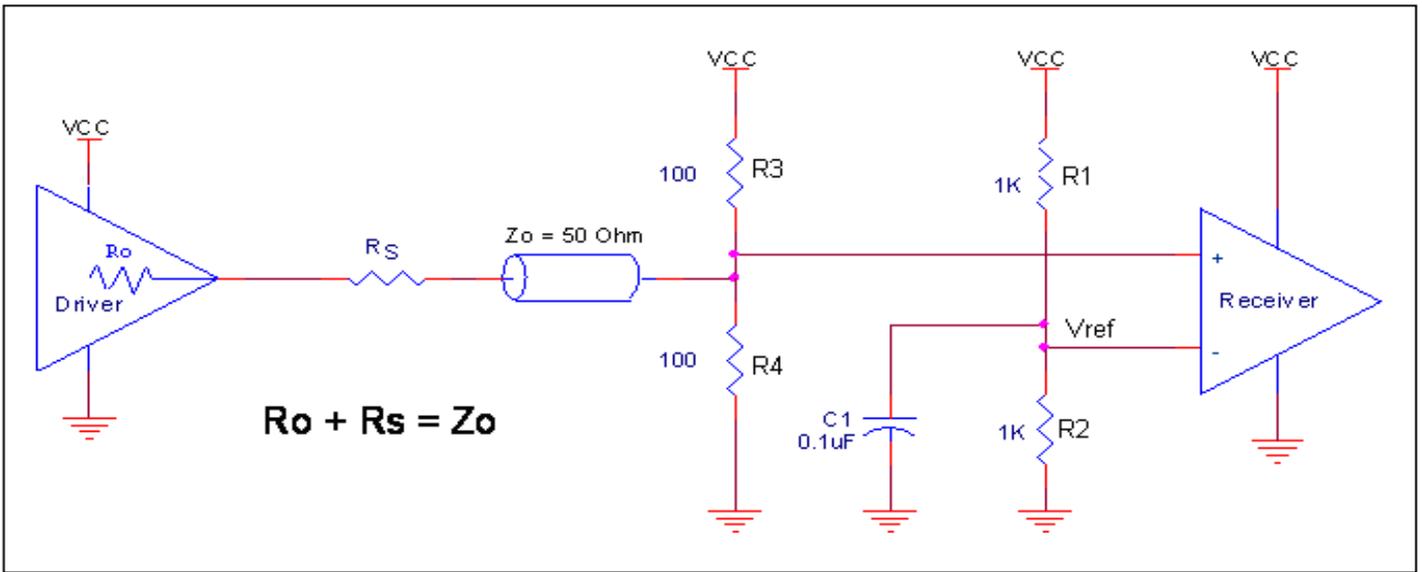

Figure 40. Example of Single-Ended Signal to Drive Differential Input

Vth = VCC*[R2/(R1+R2)]

For the example in Figure 40, R1 = R2, so Vth = VCC/2 =1.65 V

The suggested single-ended signal input:

V_{IHmax} = VCC

V_{ILmin} = 0 V

V_{swing} = 0.6 V ~ VCC

DC offset (Swing Center) = Vth/2 +/- V_{swing}*10%

8.4 JITTER PERFORMANCE

Table 30: Gigabit Ethernet Output Clock Jitter Generation
(jitter measured on one differential output of the APLL with one differential output enabled)

Output Frequency	RMS Jitter Typ (ps)	RMS Jitter Max (ps)	Test Filter	Notes
25 MHz	0.70	0.96	2.5 kHz - 5 MHz	ITU-T G.8262 limit 0.5 UI p-p (1 UI = 0.8 ns)
	0.55	0.73	12 kHz - 5 MHz	
	0.27	0.34	637 kHz - 5 MHz	IEEE 802.3-2008 limit 0.24 UI p-p / 0.0174 UI RMS (1 UI = 0.8 ns)
125MHz	0.71	1.00	2.5 kHz to 10 MHz	ITU-T G.8262 limit 0.5 UI p-p (1 UI = 0.8 ns)
	0.56	0.75	12 kHz - 20 MHz	
	0.19	0.24	637 kHz - 10 MHz	IEEE 802.3-2008 limit 0.24 UI p-p / 0.0174 UI RMS (1 UI = 0.8 ns)
156.25MHz	0.55	0.74	12 kHz - 20 MHz	
	0.52	1.18	20 kHz - 40 MHz	ITU-T G.8262 limit 0.5 UI p-p (1 UI = 100.47 ps)
	0.23	0.31	1 MHz - 30 MHz	
	0.17	0.24	1.875 MHz - 20 MHz	IEEE 802.3-2008 limit 0.28 UI p-p / 0.0203 UI RMS (1 UI = 100.47 ps)
625MHz	0.56	0.76	12 kHz - 20 MHz	
	0.52	0.65	20 kHz - 80 MHz	ITU-T G.8262 limit 0.5 UI p-p 0.0203 UI RMS (1 UI = 100.47 ps)
	0.16	0.29	1 MHz - 30 MHz	
	0.10	0.26	1.875 MHz - 20 MHz	IEEE 802.3-2008 limit 0.28 UI p-p / 0.0203 UI RMS (1 UI = 100.47 ps)
NOTE 1: DPLL locked to input clock NOTE 2: For BER = 10–12, RMS jitter = p-p jitter/13.8 per IEEE 802.3-2008 and IEEE 802.3ae-2002 section 48B.3.1.3.1				

Table 31: Gigabit Ethernet Output Clock Jitter Generation
(Jitter measured on one CMOS output of the APLL with one CMOS output enabled)

Output Frequency	RMS Jitter Typ (ps)	RMS Jitter Max (ps)	Test Filter	Notes
25 MHz	0.71	0.95	2.5 kHz - 5 MHz	ITU-T G.8262 limit 0.5 UI p-p (1 UI = 0.8 ns)
	0.54	0.70	12 kHz - 5 MHz	
	0.23	0.29	637 kHz - 5 MHz	IEEE 802.3-2008 limit 0.24 UI p-p / 0.0174 UI RMS (1 UI = 0.8 ns)
125MHz	0.78	1.07	2.5 kHz to 10 MHz	ITU-T G.8262 limit 0.5 UI p-p (1 UI = 0.8 ns)
	0.61	0.78	12 kHz - 20 MHz	
	0.20	0.25	637 kHz - 10 MHz	IEEE 802.3-2008 limit 0.24 UI p-p / 0.0174 UI RMS (1 UI = 0.8 ns)
NOTE 1: DPLL locked to input clock NOTE 2: For BER = 10–12, RMS jitter = p-p jitter/13.8 per IEEE 802.3-2008 and IEEE 802.3ae-2002 section 48B.3.1.3.1				

Table 32: SONET/SDH Output Clock Jitter Generation
(jitter measured on one differential output of the APLL with one differential output enabled

Output Frequency	RMS Jitter Typ (ps)	RMS Jitter Max (ps)	Test Filter	Notes
19.44 MHz	0.53	0.74	12 kHz to 1.3MHz	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p / 0.01 UI RMS (STM-16: 1UI = 0.40 ns)
	0.62	0.85	12kHz to 5MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.92	1.26	500 Hz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-4: 1 UI = 1.61 ns)
	0.90	1.27	1 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.32	0.43	65 kHz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-4: 1 UI = 1.61 ns)
	0.41	0.53	250 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-4: 1 UI = 1.61 ns)
77.76 MHz	0.57	1.02	12 kHz to 20 MHz	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p / 0.01 UI RMS (STM-16: 1UI = 0.40 ns)
	0.94	1.31	500 Hz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.87	1.24	1 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-4: 1 UI = 1.61 ns)
	0.27	0.36	65 kHz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.22	0.29	250 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-4: 1 UI = 1.61 ns)

Table 32: SONET/SDH Output Clock Jitter Generation
(jitter measured on one differential output of the APLL with one differential output enabled

Output Frequency	RMS Jitter Typ (ps)	RMS Jitter Max (ps)	Test Filter	Notes
155.52 MHz	0.56	0.77	12 kHz to 20 MHz	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p / 0.01 UI RMS (STM-16: 1UI = 0.40 ns)
	0.96	1.33	500 Hz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.88	1.26	1 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-4: 1 UI = 1.61 ns)
	0.68	0.97	5 kHz to 20 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-16: 1UI = 0.40 ns)
	0.28	0.37	65 kHz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.21	0.28	250 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-4: 1 UI = 1.61 ns)
	0.20	0.27	1 MHz to 20 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-16: 1UI = 0.40 ns)

Table 32: SONET/SDH Output Clock Jitter Generation
(jitter measured on one differential output of the APLL with one differential output enabled

Output Frequency	RMS Jitter Typ (ps)	RMS Jitter Max (ps)	Test Filter	Notes
622.08 MHz	0.58	0.83	12 kHz to 20 MHz	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p / 0.01 UI RMS (STM-16: 1UI = 0.40 ns)
	0.51	0.66	20kHz to 80 MHz	GR-253-CORE and ITU-T G.813 Option 2 limit 0.3 UI p-p (STM-64: 1 UI = 0.10 ns) ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-64: 1 UI = 0.10 ns)
	0.16	0.26	4 MHz to 80 MHz	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p (STM-64: 1 UI = 0.10 ns) ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-64: 1 UI = 0.10 ns)
	1.05	1.52	500 Hz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.97	1.44	1 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-4: 1 UI = 1.61 ns)
	0.73	1.06	5 kHz to 20 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-16: 1UI = 0.40 ns)
	0.29	0.39	65 kHz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.20	0.28	250 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-4: 1 UI = 1.61 ns)
	0.14	0.27	1 MHz to 20 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-16: 1UI = 0.40 ns)
NOTE 1: DPLL locked to input clock				

Table 33: SONET/SDH Output Clock Jitter Generation
(jitter measured on one CMOS output of the APLL with one CMOS output enabled)

Output Frequency	RMS Jitter Typ (ps)	RMS Jitter Max (ps)	Test Filter	Notes
19.44 MHz	0.50	0.71	12 kHz to 1.3MHz	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p / 0.01 UI RMS (STM-16: 1UI = 0.40 ns)
	0.54	0.74	12kHz to 5MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.89	1.23	500 Hz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-4: 1 UI = 1.61 ns)
	0.84	1.17	1 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.28	0.36	65 kHz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-4: 1 UI = 1.61 ns)
	0.27	0.36	250 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-4: 1 UI = 1.61 ns)
77.76 MHz	0.57	2.63	12 kHz to 20 MHz	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p (STM-4: 1 UI = 1.61 ns)
	0.93	1.30	500 Hz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.86	1.22	1 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.5 UI p-p (STM-4: 1 UI = 1.61 ns)
	0.28	0.37	65 kHz to 1.3 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-1: 1 UI = 6.43 ns)
	0.22	0.29	250 kHz to 5 MHz	ITU-T G.813 Option 1 limit 0.1 UI p-p (STM-4: 1 UI = 1.61 ns)
NOTE 1: DPLL locked to input clock				

Table 34: DPLL1/DPLL2 Output Clock Jitter Generation
(Jitter measured on one CMOS output of DPLL1/DPLL2 with all other outputs disabled)

| Output Frequency	RMS Jitter Typ (ps)	RMS Jitter Max (ps)	Test Filter	Notes
10 MHz	100.11	619.64	100 Hz - 100 kHz	
N x 1.544 MHz (Note 2)	100.63	543.45	100 Hz - 40 kHz	
	16.06	39.94	8 kHz - 40 kHz	ANSI T1.403 limit 0.07 UI p-p (DS1: 1 UI = 647 ns)
N x 2.048 MHz (Note 3)	99.42	449.83	100 Hz - 100 kHz	
	10.66	26.44	18 kHz - 100 kHz	ITU-T G.823 limit 0.2 UI p-p (E1: 1 UI = 488 ns)
34.368 MHz	101.67	202.75	100 Hz - 800 kHz	
	25.62	39.06	10 kHz - 800 kHz	ITU-T G.751 limit 0.05 UI p-p (E3: 1 UI = 29.10 ns)
44.736 MHz	105.16	198.15	100 Hz - 400 kHz	
	20.77	27.44	30 kHz - 400 kHz	
NOTE 1:DPLL1/2 locked to input clock NOTE 2: Measured on 12.352 MHz output clock NOTE 3: Measured on 16.384 MHz output clock				

Table 35: DPLL3 Output Clock Jitter Generation
(Jitter measured on one CMOS output of DPLL3 with all other outputs disabled)

Output Frequency	RMS Jitter Typ (ps)	RMS Jitter Max (ps)	Test Filter	Notes
N x 2.048 MHz Note 2	147.325	347.530	100 Hz - 100 kHz	
	8.02	17.24	18 kHz - 100 kHz	ITU-T G.823 limit 0.2 UI p-p (E1: 1 UI = 488 ns)
N x 1.544 MHz Note 3	133.88	303.43	100 Hz - 40 kHz	
	0.80	1.47	8 kHz - 40 kHz	ANSI T1.403 limit 0.07 UI p-p (DS1: 1 UI = 647 ns)
NOTE 1:DPLL3 locked to input clock NOTE 2: Measured on 12.288 MHz output clock NOTE 3: Measured on 12.352 MHz output clock				

8.5   INPUT / OUTPUT CLOCK TIMING

The inputs and outputs are aligned ideally. But due to the circuit delays, there is delay between the inputs and outputs.
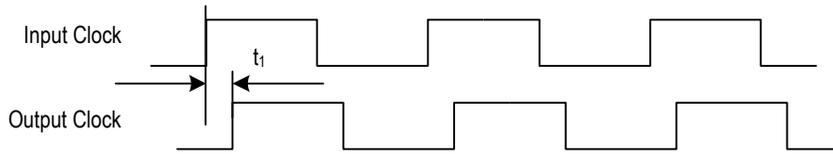
Figure 41. Input / output clock timing
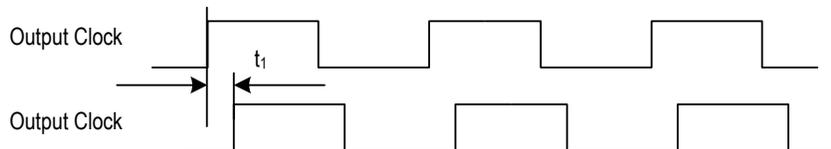
Table 36: Input-to-Output Delay via APLL

Output	t_1 Min (ns)	t_1 Max (ns)	t_1 Range (ns$_{pp}$)
Any LVCMOS Input to any of OUT01 or OUT02	13	19	6 (±3 around mean)
Any LVPECL/LVDS Input to any of OUT03 or OUT04	11.5	16.5	5 (±2.5 around mean)
Any Input to any APLL Output	10	19	9 (±4.5 around mean)
Any Input to [M]FRSYNC Output	0	8	8 (typical value is 2.5ns)

NOTE 1. The measurements in the above table takes into account any delays in the clock path from any input to any output; through either DPLL1 or DPLL2 and the APLL.
NOTE 2. The measurements in the above table are over operational temperature, varying power supply and repeated power on/off cycle.
NOTE 3. Measurements are taken using an ideal REF input and an ideal System clock to account for only internal delays in the device.

8.6   OUTPUT / OUTPUT CLOCK TIMING

Figure 42. Output / output clock timing

Table 37: APLL1/2 Output-to-Output Delay

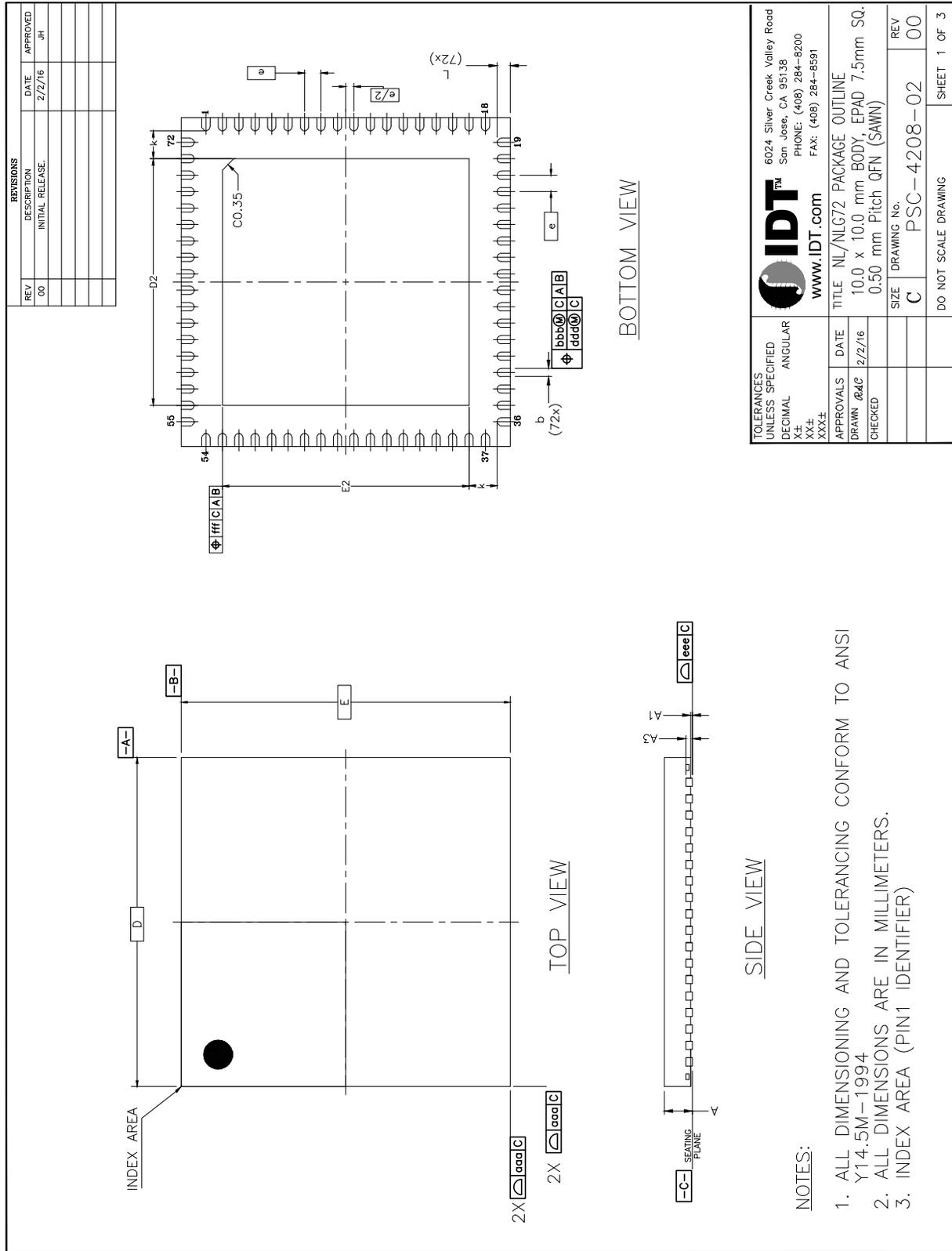| Output	t_1 Min (ps)	t_1 Max (ps)
Output-to-Output, LVCMOS (OUT01 to OUT02))	-110	110
Output-to-Output, LVPECL/LVDS Input to a LVPECL/LVDS Output (OUT03 to OUT04)	-85	85

PACKAGE OUTLINE DRAWINGS
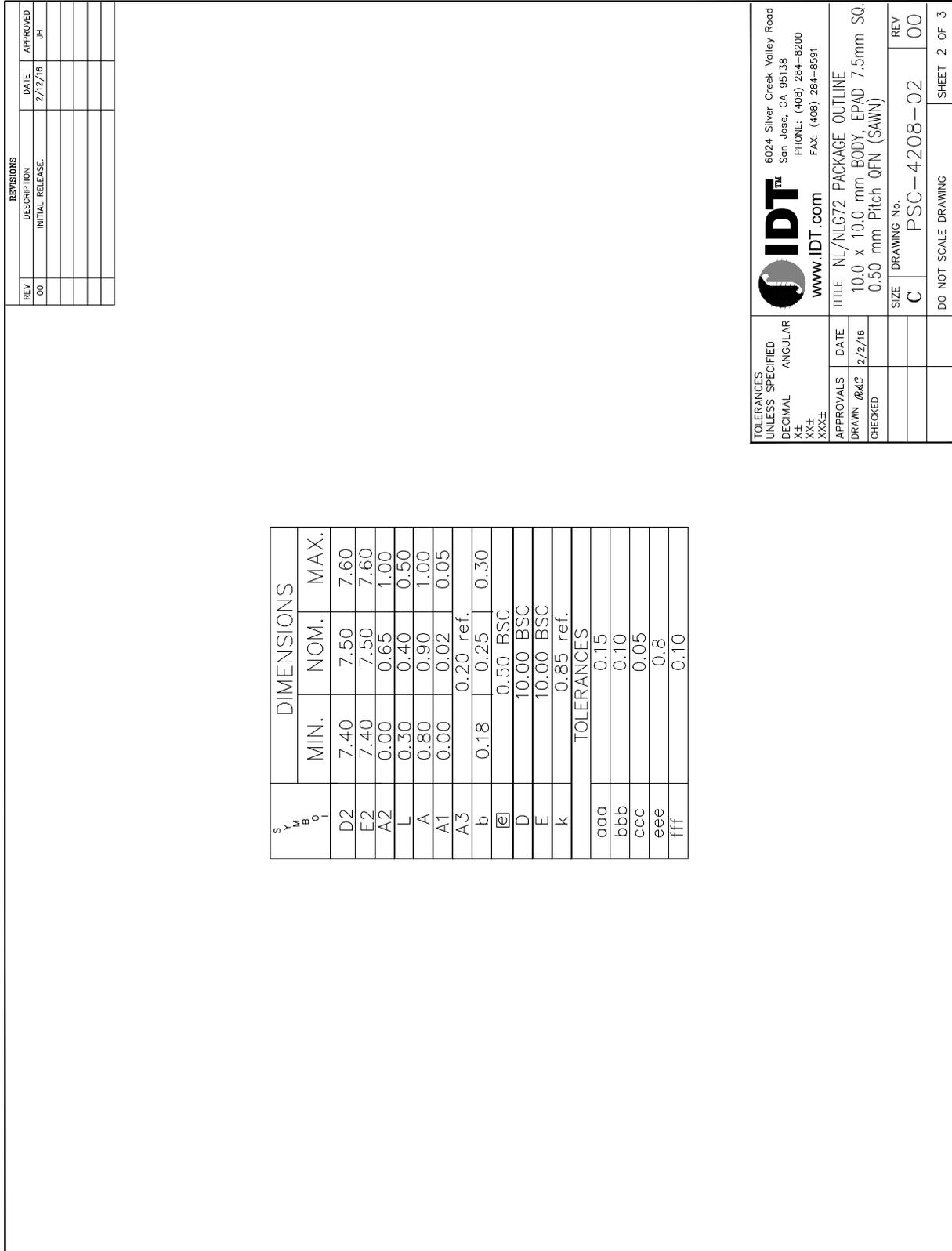

Figure 43. Package Outline Drawings – Page 1

SYMBOL	MIN.	NOM.	MAX.
D2	7.40	7.50	7.60
E2	7.40	7.50	7.60
A2	0.00	0.65	1.00
L	0.30	0.40	0.50
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20 ref.	
b	0.18	0.25	0.30
e		0.50 BSC	
D		10.00 BSC	
E		10.00 BSC	
k		0.85 ref.	

DIMENSIONS

TOLERANCES

aaa	0.15
bbb	0.10
ccc	0.05
eee	0.8
fff	0.10

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE.	2/12/16	JH

IDT™
6024 Silver Creek Valley Road
San Jose, CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-8591
www.IDT.com

TITLE NL/NLG72 PACKAGE OUTLINE
10.0 x 10.0 mm BODY, EPAD 7.5mm SQ.
0.50 mm Pitch QFN (SAWN)

DRAWING No. PSC-4208-02   REV 00

SIZE C

DO NOT SCALE DRAWING   SHEET 2 OF 3

TOLERANCES
UNLESS SPECIFIED
DECIMAL   ANGULAR
X±
XX±
XXX±

APPROVALS	DATE
DRAWN B&C	2/2/16
CHECKED	

Figure 44. Package Outline Drawings – Page 2

RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT
   FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

REVISIONS
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE.	2/2/16	JH

6024 Silver Creek Valley Road
San Jose, CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-8591
www.IDT.com

TITLE NL/NLG72 PACKAGE OUTLINE
10.0 x 10.0 mm BODY, EPAD 7.5mm SQ.
0.50 mm Pitch QFN (SAWN)

TOLERANCES
UNLESS SPECIFIED
DECIMAL   ANGULAR
X±
XX±
XXX±

APPROVALS	DATE
DRAWN RMC	2/2/16
CHECKED	

SIZE C   DRAWING No. PSC-4208-02   REV 00

DO NOT SCALE DRAWING   SHEET 3 OF 3

Figure 45. Package Outline Drawings – Page 3

ORDERING INFORMATION

Table 38: Ordering Information

Part/Order Number	Package	Shipping Packaging	Temperature
82P33813NLG	72-Pin QFN Green Package	Tray	-40° to +85°C
82P33813NLG8	72-Pin QFN Green Package	Tape & Reel, Pin 1 Orientation EIA-481-C	-40° to +85°C

REVISION HISTORY

Revision Date	Description of Change
September 5, 2017	* Updated the description of MS/SL in Table 1 * Added MS/SL PIN USAGE * Updated Table 8 * Updated the package outline drawings; however, no mechanical changes.
March 16, 2016	Table 42, added 82P33813NLG8 package. Removed "Confidential" label from header/footer.
December 16, 2016	Pages 31-32, 37-38, 67.

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