## Description

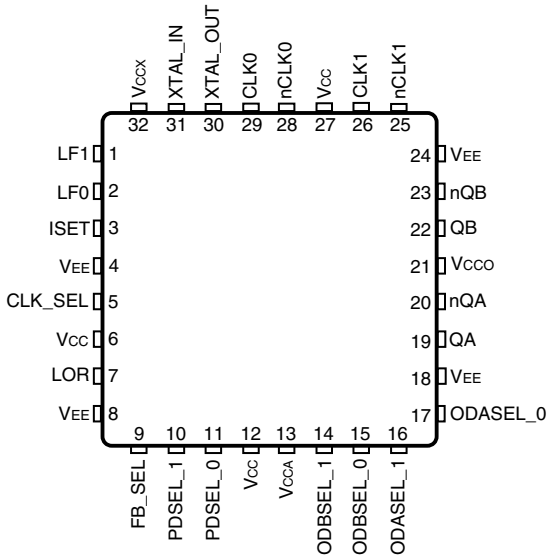
The 813N2532 device uses IDT's fourth generation FemtoClock® NG technology for optimal high clock frequency and low phase noise performance, combined with a low power consumption and high power supply noise rejection. The 813N2532 is a PLL based synchronous multiplier that is optimized for PDH or SONET to Ethernet clock jitter attenuation and frequency translation.

The 813N2532 is a fully integrated Phase Locked loop utilizing a FemtoClock NG Digital VCXO that provides the low jitter, high frequency SONET/PDH output clock that easily meets OC-48 jitter requirements. This VCXO technology simplifies PLL design by replacing the pullable crystal requirement of analog VCXOs with a fixed 27MHz generator crystal. Jitter attenuation down to 10Hz is provided by an external loop filter. Pre-divider and output divider multiplication ratios are selected using device selection control pins. The multiplication ratios are optimized to support most common clock rates used in PDH, SONET and Ethernet applications. The device requires the use of an external, inexpensive fundamental mode 27MHz crystal. The device is packaged in a space-saving 32-VFQFN package and supports commercial temperature range.

## Features

- Fourth generation FemtoClock® NG technology
- Two LVPECL output pairs
- Output frequencies: 19.44MHz, 25MHz, 125MHz, 155.52MHz and 156.25MHz
- Two differential inputs support the following input types: LVPECL, LVDS, LVHSTL, HCSL
- Accepts input frequencies from 8kHz to 38.88MHz including 8kHz, 19.44MHz, 25MHz and 38.88MHz
- Crystal interface optimized for a 27MHz, 10pF parallel resonant crystal
- Attenuates the phase jitter of the input clock by using a low-cost fundamental mode crystal
- Customized settings for jitter attenuation and reference tracking using external loop filter connection
- FemtoClock NG frequency multiplier provides low jitter, high frequency output
- Absolute pull range: ±100ppm
- Power supply noise rejection (PSNR): -95dB (typical)
- RMS phase jitter at 156.25MHz, using a 27MHz crystal (12kHz – 20MHz): 0.64ps (typical)
- RMS phase jitter at 155.52MHz, using a 27MHz crystal (12kHz – 20MHz): 0.64ps (typical)
- RMS phase jitter at 125MHz, using a 27MHz crystal (12kHz – 20MHz): 0.66ps (typical)
- 3.3V supply voltage
- 0°C to 70°C ambient operating temperature
- Lead-free (RoHS 6) packaging

## Pin Assignments



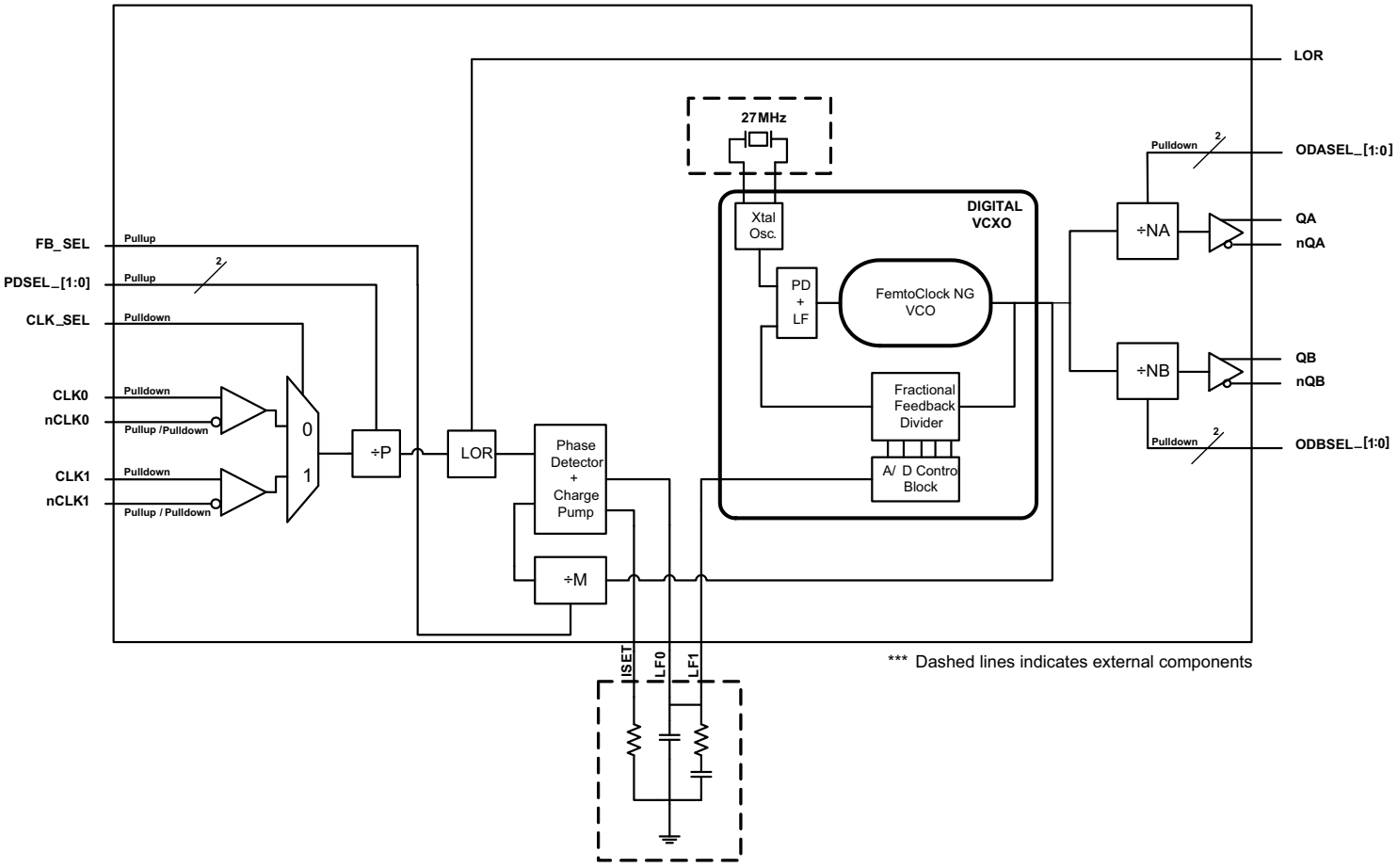

**813N2532**

**32 Lead VFQFN**
**5 x 5 x 0.925 mm package body**
**3.15 x 3.15 mm ePad size**

**K Package**

**Top View**

## Block Diagram



# Pin Description and Pin Characteristics Tables

**Table 1. Pin Descriptions**

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1, 2 | LF1, LF0 | Analog Input/Output | | Loop filter connection node pins. LF0 is the output. LF1 is the input. |
| 3 | ISET | Analog Input/Output | | Charge pump current setting pin. |
| 4, 8, 18, 24 | $V_{EE}$ | Power | | Negative supply pins. |
| 5 | CLK_SEL | Input | Pulldown | Input clock select. When HIGH selects CLK1, nCLK1. When LOW, selects CLK0, nCLK0. LVCMOS / LVTTL interface levels. |
| 6, 12, 27 | $V_{CC}$ | Power | | Core supply pins. |
| 7 | LOR | Output | | Loss of reference indicator. LVCMOS/LVTTL interface levels. |
| 9 | FB_SEL | Input | Pullup | Feedback divider select pin. LVCMOS/LVTTL interface levels. See Table 3B. |
| 10, 11 | PDSEL_1, PDSEL_0 | Input | Pullup | Pre-divider select pins. LVCMOS/LVTTL interface levels. See Table 3A. |
| 13 | $V_{CCA}$ | Power | | Analog supply pin. |
| 14, 15 | ODBSEL_1, ODBSEL_0 | Input | Pulldown | Frequency select pins for Bank B output. See Table 3C. LVCMOS/LVTTL interface levels. |
| 16, 17 | ODASEL_1, ODASEL_0 | Input | Pulldown | Frequency select pins for Bank A output. See Table 3C. LVCMOS/LVTTL interface levels. |
| 19, 20 | QA, nQA | Output | | Differential Bank A clock outputs. LVPECL interface levels. |
| 21 | $V_{CCO}$ | Power | | Output supply pin. |
| 22, 23 | QB, nQB | Output | | Differential Bank B clock outputs. LVPECL interface levels. |
| 25 | nCLK1 | Input | Pullup/ Pulldown | Inverting differential clock input. $V_{CC}/2$ bias voltage when left floating. |
| 26 | CLK1 | Input | Pulldown | Non-inverting differential clock input. |
| 28 | nCLK0 | Input | Pullup/ Pulldown | Inverting differential clock input. $V_{CC}/2$ bias voltage when left floating. |
| 29 | CLK0 | Input | Pulldown | Non-inverting differential clock input. |
| 30, 31 | XTAL_OUT, XTAL_IN | Input | | Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output. |
| 32 | $V_{CCX}$ | Power | | Power supply pin for the crystal oscillator. |

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

**Table 2. Pin Characteristics**

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 2 | | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | kΩ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | kΩ |

# Function Tables

### Table 3A. Pre-Divider Selection Function Table

| Inputs | | |
|---|---|---|
| PDSEL_1 | PDSEL_0 | ÷P Value |
| 0 | 0 | 1 |
| 0 | 1 | 1944 |
| 1 | 0 | 2500 |
| 1 | 1 | 3888 (default) |

### Table 3C. Output Divider Function Table

| Inputs | | |
|---|---|---|
| ODxSEL_1 | ODxSEL_0 | ÷Nx Value |
| 0 | 0 | 128 (default) |
| 0 | 1 | 100 |
| 1 | 0 | 20 |
| 1 | 1 | 16 |

NOTE: x denotes A or B.

### Table 3B. Feedback Divider Selection Function Table

| Input | |
|---|---|
| FB_SEL | VCO Frequency (MHz) |
| 0 | 2500 |
| 1 | 2488.32 (default) |

### Table 3D. Frequency Function Table

| Input Frequency (MHz) | ÷P Value | FemtoClock NG VCXO Center Frequency (MHz) | ÷Nx Value | Output Frequency (MHz) |
|---|---|---|---|---|
| 0.008 | 1 | 2488.32 | 128 | 19.44 |
| 0.008 | 1 | 2500 | 100 | 25 |
| 0.008 | 1 | 2500 | 20 | 125 |
| 0.008 | 1 | 2488.32 | 16 | 155.52 |
| 0.008 | 1 | 2500 | 16 | 156.25 |
| 19.44 | 1944 | 2488.32 | 128 | 19.44 |
| 19.44 | 1944 | 2500 | 100 | 25 |
| 19.44 | 1944 | 2500 | 20 | 125 |
| 19.44 | 1944 | 2488.32 | 16 | 155.52 |
| 19.44 | 1944 | 2500 | 16 | 156.25 |
| 25 | 2500 | 2488.32 | 128 | 19.44 |
| 25 | 2500 | 2500 | 100 | 25 |
| 25 | 2500 | 2500 | 20 | 125 |
| 25 | 2500 | 2488.32 | 16 | 155.52 |
| 25 | 2500 | 2500 | 16 | 156.25 |
| 38.88 | 3888 | 2488.32 | 128 | 19.44 |
| 38.88 | 3888 | 2500 | 100 | 25 |
| 38.88 | 3888 | 2500 | 20 | 125 |
| 38.88 | 3888 | 2488.32 | 16 | 155.52 |
| 38.88 | 3888 | 2500 | 16 | 156.25 |

NOTE: x denotes A or B.

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|---|---|
| Supply Voltage, $V_{CC}$ | 3.63V |
| Inputs, $V_I$<br>XTAL_IN<br>Other Inputs | <br>0V to 2V<br>-0.5V to $V_{CC}$+ 0.5V |
| Outputs, $I_O$<br>Continuous Current<br>Surge Current | <br>50mA<br>100mA |
| Package Thermal Impedance, $\theta_{JA}$ | 33.1°C/W (0 mps) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

## DC Electrical Characteristics

**Table 4A. LVPECL Power Supply DC Characteristics,** $V_{CC} = V_{CCO} = V_{CCX} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{CCA}$ | Analog Supply Voltage | | $V_{CC}$ – 0.29 | 3.3 | $V_{CC}$ | V |
| $V_{CCO}$ | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{CCX}$ | Crystal Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{EE}$ | Power Supply Current | | | | 312 | mA |
| $I_{CCA}$ | Analog Supply Current | | | | 29 | mA |

**Table 4B. LVCMOS/LVTTL DC Characteristics,** $V_{CC} = V_{CCO} = V_{CCX} = 3.3V \pm 5\%$, $T_A = 0°C$ to 70°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | 2 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | | -0.3 | | 0.8 | V |
| $I_{IH}$ | Input High Current | CLK_SEL, CLK0, ODASEL_[1:0], ODBSEL_[1:0] | $V_{CC} = V_{IN} = 3.465V$ | | | 150 | µA |
| | | FB_SEL, PDSEL_[1:0] | $V_{CC} = V_{IN} = 3.465V$ | | | 10 | µA |
| $I_{IL}$ | Input Low Current | CLK_SEL, CLK0, ODASEL_[1:0], ODBSEL_[1:0] | $V_{CC} = 3.465V$, $V_{IN} = 0V$ | -10 | | | µA |
| | | FB_SEL, PDSEL_[1:0] | $V_{CC} = 3.465$, $V_{IN} = 0V$ | -150 | | | µA |

**Table 4C. Differential DC Characteristics,** $V_{CC} = V_{CCO} = V_{CCX} = 3.3V \pm 5\%$, $T_A = 0°C$ to 70°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High Current | CLK0, nCLK0, CLK1, nCLK1 | $V_{CC} = V_{IN} = 3.465V$ | | | 150 | µA |
| $I_{IL}$ | Input Low Current | CLK0, CLK1 | $V_{CC} = 3.465V$, $V_{IN} = 0V$ | -10 | | | µA |
| | | nCLK0, nCLK1 | $V_{CC} = 3.465V$, $V_{IN} = 0V$ | -150 | | | µA |
| $V_{PP}$ | Peak-to-Peak Input Voltage; NOTE 1 | | | 0.15 | | 1.3 | V |
| $V_{CMR}$ | Common Mode Input Voltage; NOTES 1, 2 | | | $V_{EE}$ | | $V_{CC} – 0.85$ | V |

NOTE 1: $V_{IL}$ should not be less than -0.3V.
NOTE 2. Common mode voltage is defined at the crosspoint.

**Table 4D. LVPECL DC Characteristics,** $V_{CC} = V_{CCO} = V_{CCX} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage; NOTE 1 | | $V_{CCO} – 1.10$ | | $V_{CCO} – 0.75$ | V |
| $V_{OL}$ | Output Low Voltage; NOTE 1 | | $V_{CCO} – 2.0$ | | $V_{CCO} – 1.6$ | V |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{CCO} – 2V$. See Parameter Measurement Information section, *3.3V Output Load Test Circuit.*

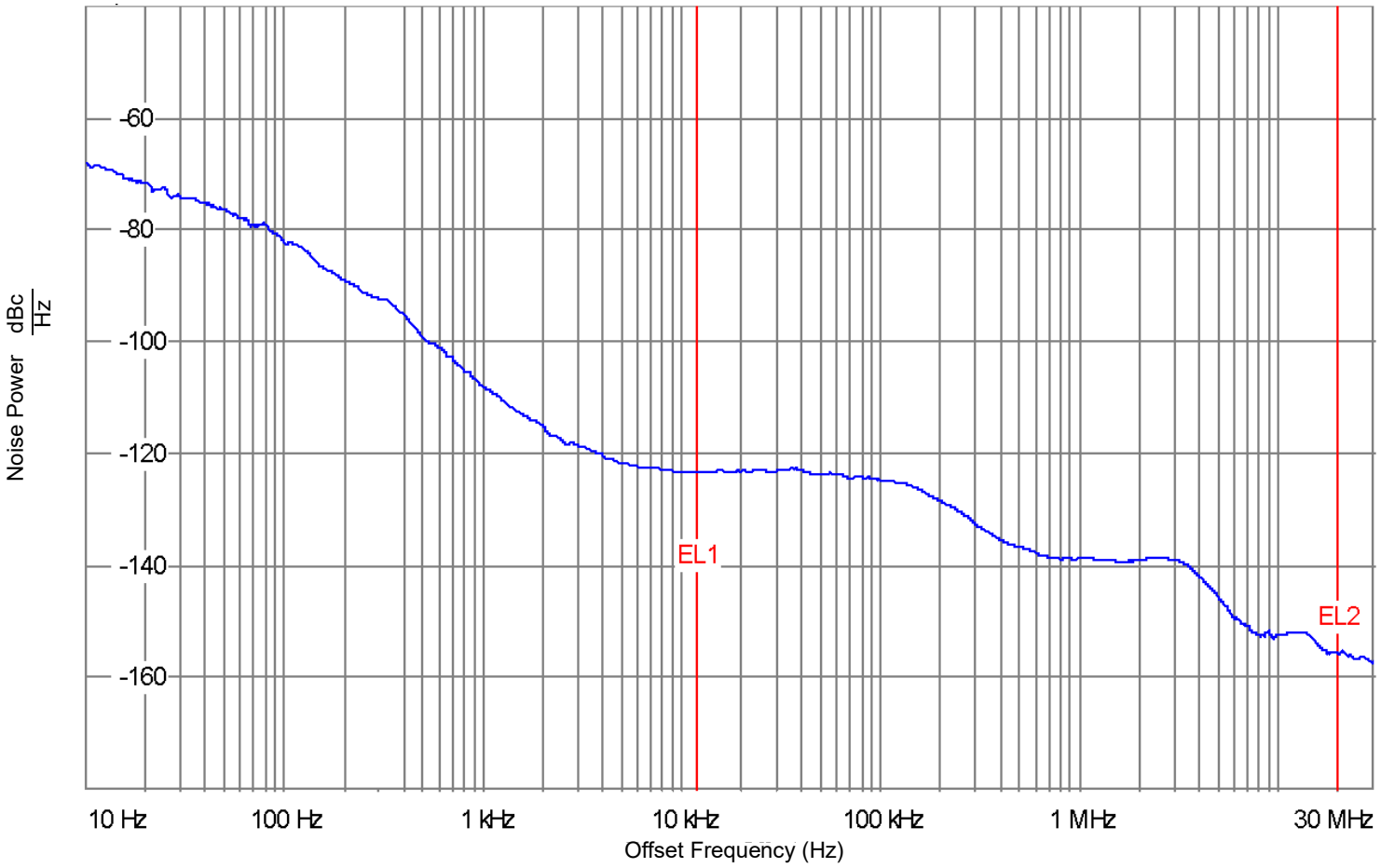
## AC Electrical Characteristics

**Table 5. AC Characteristics,** $V_{CC} = V_{CCO} = V_{CCX} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

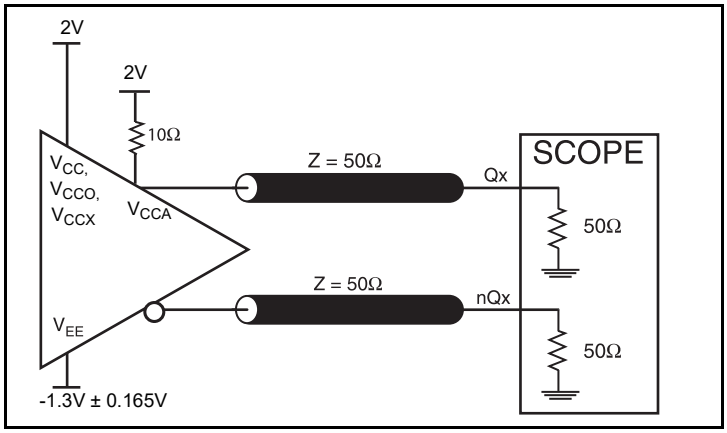
| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $f_{IN}$ | Input Frequency | | 0.008 | | 38.88 | MHz |
| $f_{OUT}$ | Output Frequency | | 19.44 | | 156.25 | MHz |
| *t*jit(Ø) | RMS Phase Jitter, (Random), NOTE 1 | 156.25MHz $f_{OUT}$, 27MHz crystal, Integration Range: 12kHz – 20MHz | | 0.64 | | ps |
| | | 155.52MHz $f_{OUT}$, 27MHz crystal, Integration Range: 12kHz – 20MHz | | 0.64 | | ps |
| | | 125MHz $f_{OUT}$, 27MHz crystal, Integration Range: 12kHz – 20MHz | | 0.66 | | ps |
| *t*sk(o) | Output Skew; NOTE 2, 3 | | | | 80 | ps |
| PSNR | Power Supply Noise Rejection; NOTE 4 | $V_{PP}$ = 50mV Sine Wave, Range: 10kHz – 10MHz | | -95 | | dB |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 200 | | 500 | ps |
| odc | Output Duty Cycle | | 48 | | 52 | % |
| $t_{LOCK}$ | Output-to-Input Phase Lock Time; NOTE 5 | Reference Clock Input is ±100ppm from Nominal Frequency | | 3 | | s |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized with outputs at the same frequency using the loop filter components for the 44Hz loop bandwidth. Refer to Jitter Attenuator Loop Bandwidth Selection Table.
NOTE 1: Refer to the Phase Noise Plot.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross point.
NOTE 4: PSNR results achieved by injecting noise on $V_{CCA}$ supply pin with no external filter network.
NOTE 5: Lock Time measured from power-up to stable output frequency.

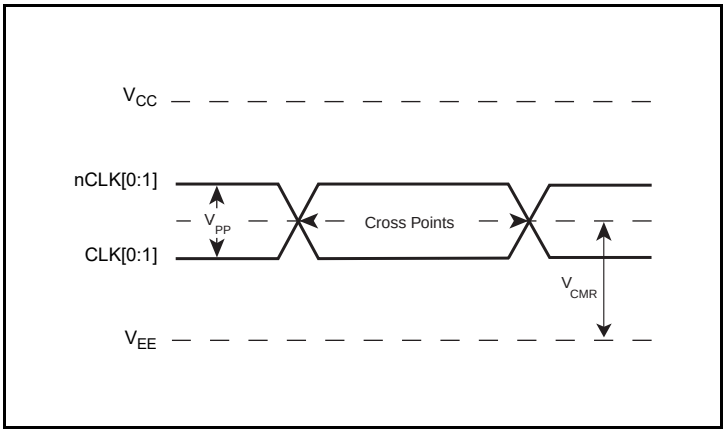
## Typical Phase Noise at 125MHz



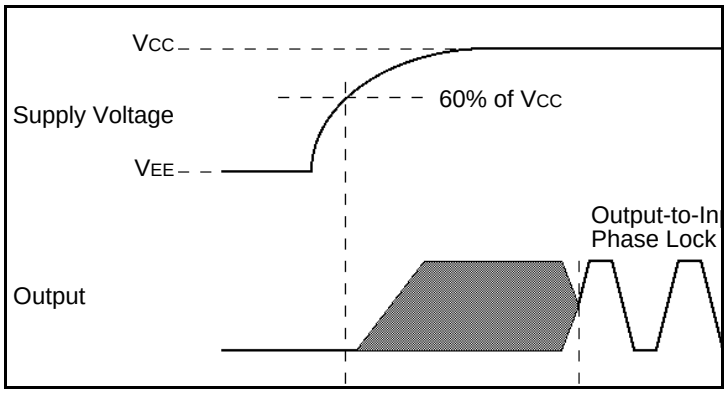
## Parameter Measurement Information



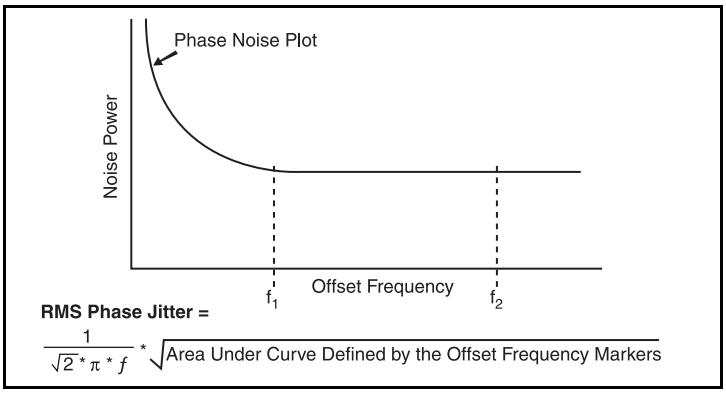

**3.3V LVPECL Output Load AC Test Circuit**



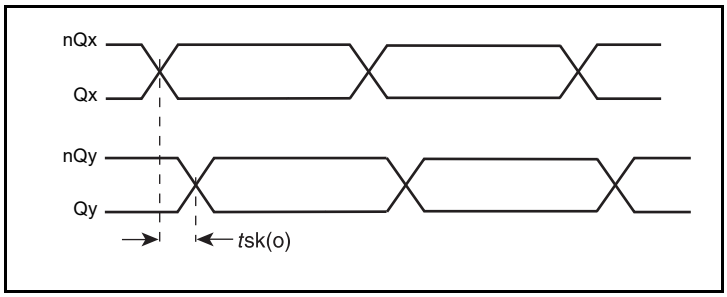

**Differential Input Level**



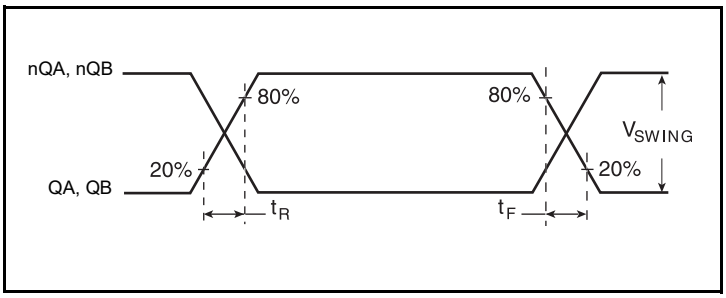

**Output-to-Input Phase Lock Time**



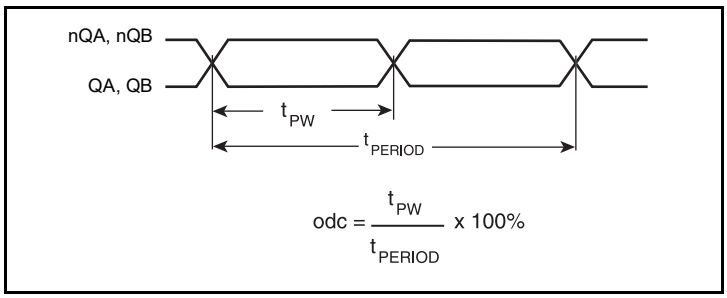

**RMS Phase Jitter**




**Output Skew**




**LVPECL Output Rise/Fall Time**




**Output Duty Cycle/Pulse Width/Period**

# Applications Information

## Wiring the Differential Input to Accept Single-Ended Levels

*Figure 1* shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the $V_1$ in the center of the input voltage swing. For example, if the input clock swing is 2.5V and $V_{CC}$ = 3.3V, R1 and R2 value should be adjusted to set $V_1$ at 1.25V. The values below are for when both the single ended swing and $V_{CC}$ are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however $V_{IL}$ cannot be less than -0.3V and $V_{IH}$ cannot be more than $V_{CC}$ + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

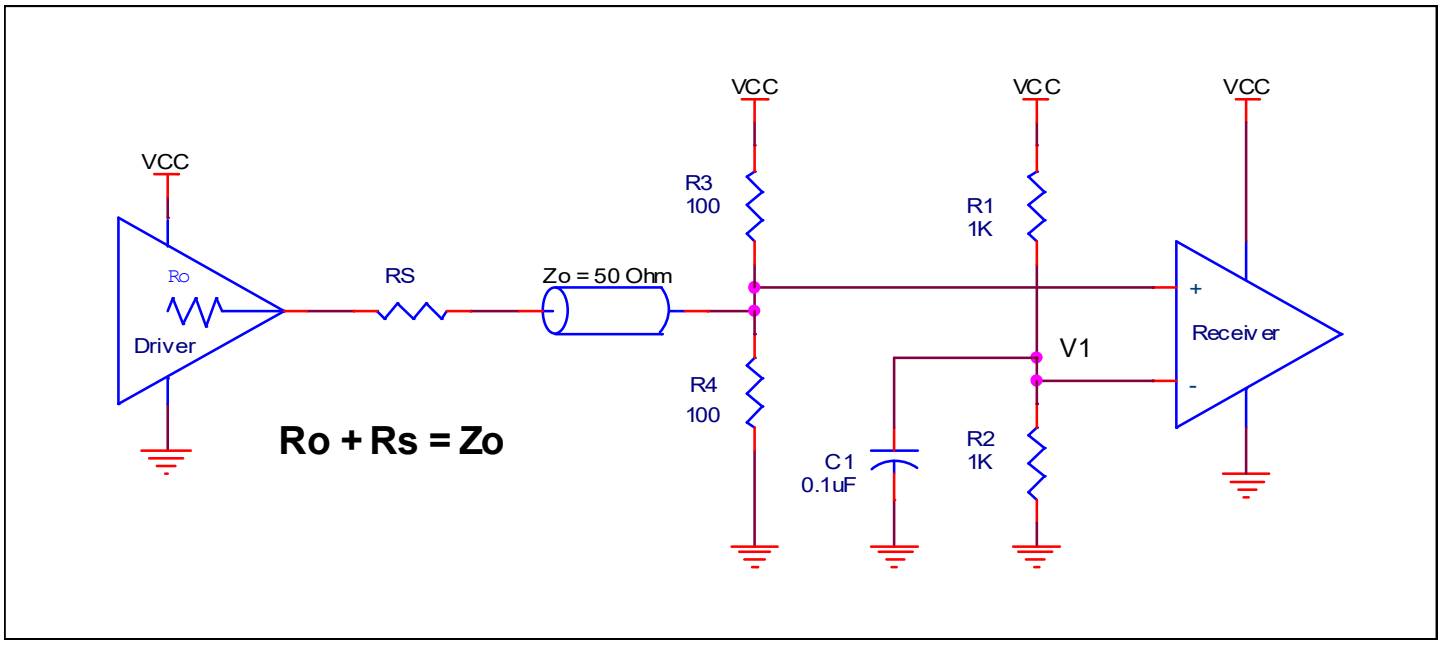



**Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels**

## Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both $V_{SWING}$ and $V_{OH}$ must meet the $V_{PP}$ and $V_{CMR}$ input requirements. *Figures 2A to 2E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

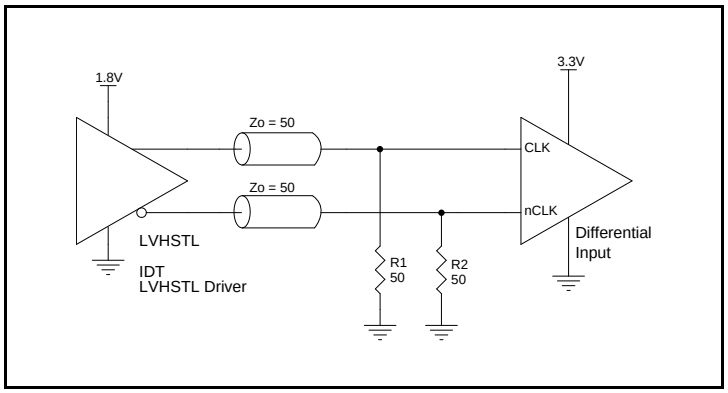



**Figure 2A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver**

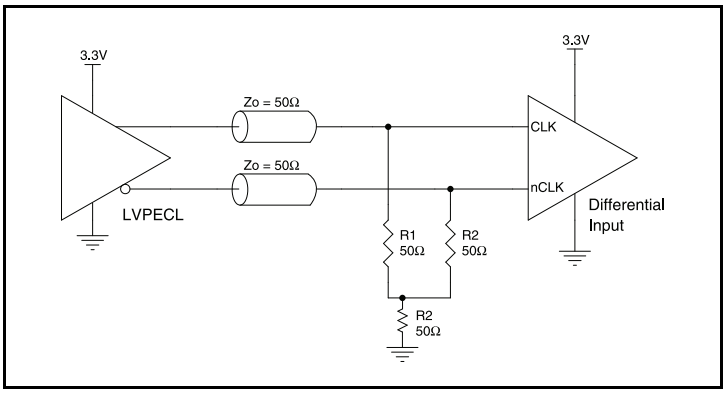



**Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**

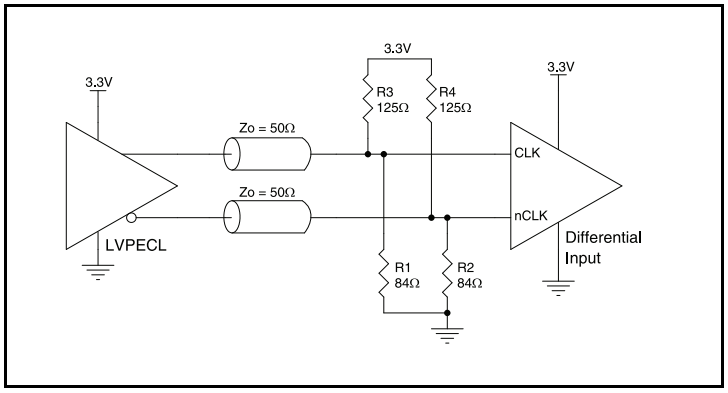



**Figure 2C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**

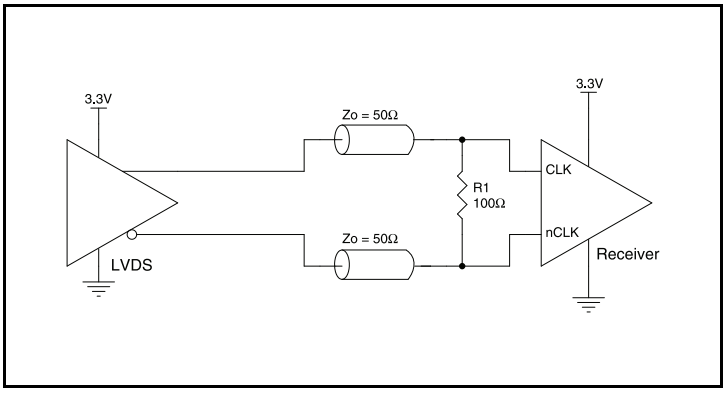



**Figure 2D. CLK/nCLK Input Driven by a 3.3V LVDS Driver**

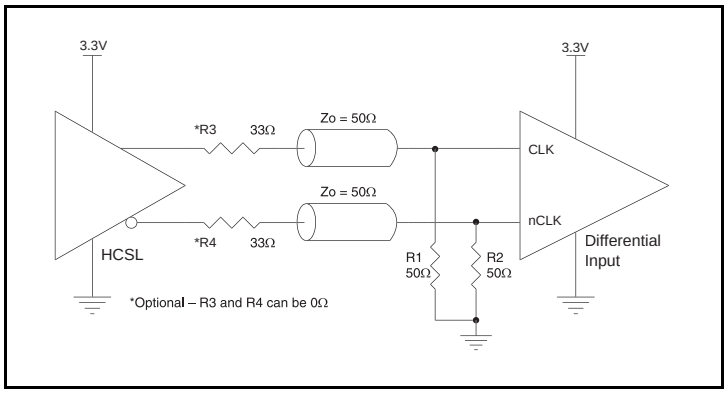



**Figure 2E. CLK/nCLK Input Driven by a 3.3V HCSL Driver**

## Recommendations for Unused Input and Output Pins

### Inputs:

#### CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

#### LVCMOS Control Pins

All control pins have internal pullup or pulldown resistors; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### Outputs:

#### LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

## Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

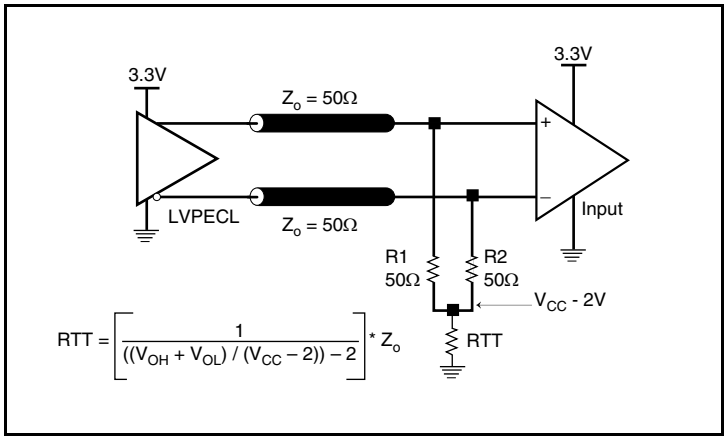



**Figure 3A. 3.3V LVPECL Output Termination**

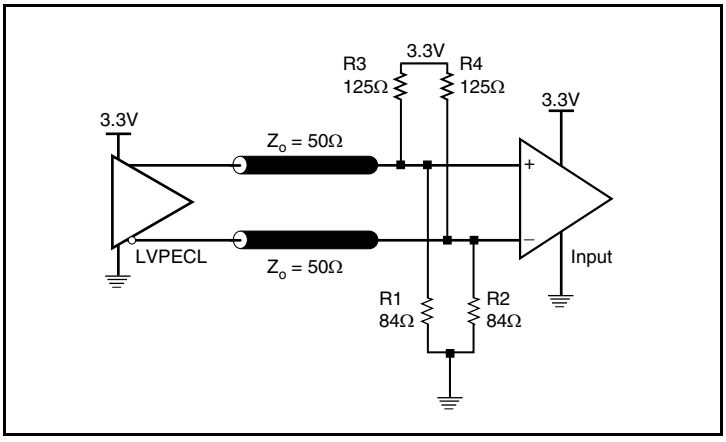



**Figure 3B. 3.3V LVPECL Output Termination**

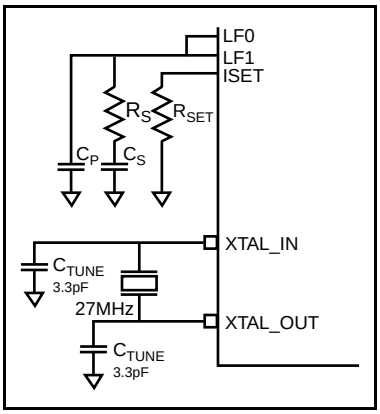
## Jitter Attenuator External Components

Choosing the correct external components and having a proper printed circuit board (PCB) layout is a key task for quality operation of the Jitter Attenuator. In choosing a crystal, special precaution must be taken with load capacitance ($C_L$), frequency accuracy and temperature range.

The crystal's $C_L$ characteristic determines its resonating frequency and is closely related to the center tuning of the crystal. The total external capacitance seen by the crystal when installed on a PCB is the sum of the stray board capacitance, IC package lead capacitance, internal device capacitance and any installed tuning capacitors (CTUNE). The recommended $C_L$ in the Crystal Parameter Table balances the tuning range by centering the tuning curve for a typical PCB. If the crystal $C_L$ is greater than the total external capacitance, the crystal will oscillate at a higher frequency than the specification. If the crystal $C_L$ is lower than the total external capacitance, the crystal will oscillate at a lower frequency than the specification. Tuning adjustments might be required depending on the PCB parasitics or if using a crystal with a higher $C_L$ specification.

In addition, the frequency accuracy specification in the crystal characteristics table are used to calculate the APR (Absolute Pull Range)

.




### Crystal Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| | Mode of Oscillation | | | Fundamental | | |
| $f_N$ | Frequency | | | 27 | | MHz |
| $f_T$ | Frequency Tolerance | | | | ±20 | ppm |
| $f_S$ | Frequency Stability | | | | ±20 | ppm |
| | Operating Temperature Range | | 0 | | +70 | $^0$C |
| $C_L$ | Load Capacitance | | | 10 | | pF |
| $C_O$ | Shunt Capacitance | | | 4 | | pF |
| ESR | Equivalent Series Resistance | | | | 40 | Ω |
| | Drive Level | | | | 1 | mW |
| | Aging @ 25 $^0$C | First Year | | | ±3 | ppm |

The VCXO-PLL Loop Bandwidth Selection Table shows $R_S$, $C_S$, $C_P$ and $R_{SET}$ values for recommended high, mid and low loop bandwidth configurations. The device has been characterized using these parameters. In addition, the digital VCXO gain ($K_{VCXO}$) has been provided for additional loop filter requirements.

**Jitter Attenuator Characteristics Table**

| Symbol | Parameter | Typical | Unit |
|---|---|---|---|
| $k_{VCXO}$ | VCXO Gain | 2.78 | kHz/V |

**Jitter Attenuator Loop Bandwidth Selection Table** ($2^{ND}$ Order Loop Filter)

| Bandwidth | Crystal Frequency | $R_S$ (kΩ) | $C_S$ (µF) | $C_P$ (µF) | R3 (kΩ) | C3 (µF) | $R_{SET}$ (kΩ) |
|---|---|---|---|---|---|---|---|
| 15Hz (Low) | 27MHz | 215 | 10 | 0.022 | 0 | DEPOP | 2.74 |
| 30Hz (Mid) | 27MHz | 365 | 2.2 | 0.0047 | 0 | DEPOP | 2.74 |
| 60Hz (High) | 27MHz | 470 | 1 | 0.0022 | 0 | DEPOP | 1.5 |

NOTE: See Application schematic to identify loop filter components $R_S$, $C_S$, $C_P$, R3, C3 and $R_{SET}$.

For applications in which there is substantial low frequency jitter in the input reference and the phase detector frequency of 8kHz or 10kHz lies in or near a jitter mask, a three pole filter is recommended. Suggested part values are in the table below. Note that the option of a three pole filter can be left open by laying out the three pole filter but setting R3 to 0Ω and not populating C3. Refer to the application schematic for a specific example.

**Jitter Attenuator Loop Bandwidth Selection Table** ($3^{RD}$ Order Loop Filter)

| Bandwidth | Crystal Frequency | $R_S$ (kΩ) | $C_S$ (µF) | $C_P$ (µF) | R3 (kΩ) | C3 (µF) | $R_{SET}$ (kΩ) |
|---|---|---|---|---|---|---|---|
| 15Hz (Low) | 27MHz | 196 | 10 | 0.022 | 82.5 | 0.010 | 2.74 |
| 30Hz (Mid) | 27MHz | 392 | 2.2 | 0.0047 | 165 | 0.0022 | 2.74 |
| 60Hz (High) | 27MHz | 432 | 1 | 0.0022 | 182 | 0.001 | 1.5 |

NOTE: See Application schematic to identify loop filter components $R_S$, $C_S$, $C_P$, R3, C3 and $R_{SET}$.

The crystal and external loop filter components should be kept as close as possible to the device. Loop filter and crystal traces should be kept short and separated from each other. Other signal traces should be kept separate and not run underneath the device, loop filter or crystal components.

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

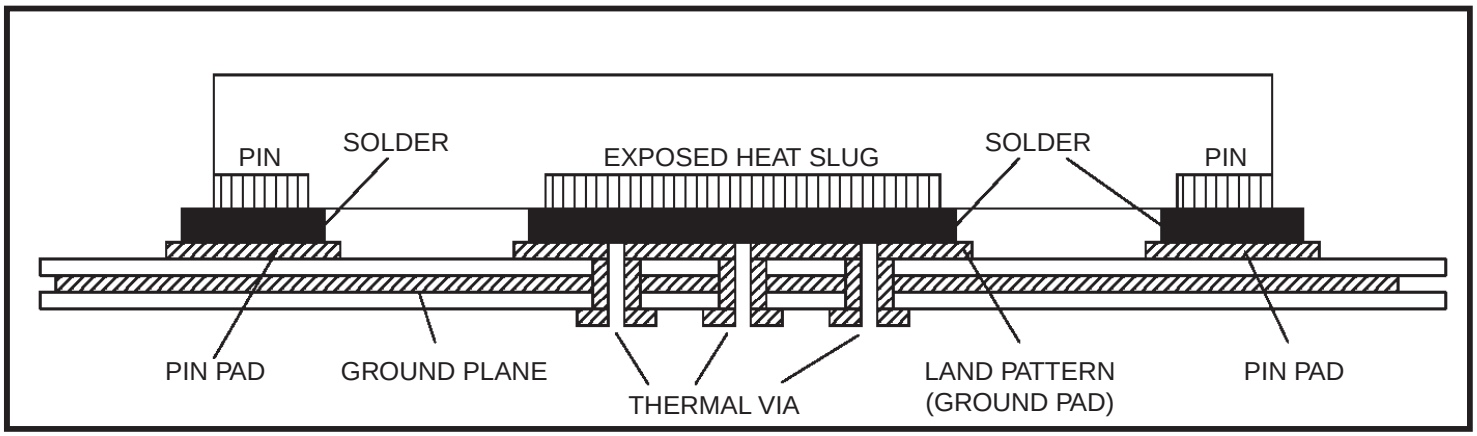



**Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**

## Schematic Example

*Figure 5* shows an example of the 813N2532 application schematic. In this example, the device is operated at $V_{CC} = V_{CCA} = V_{CCX} = V_{CCO}$ = 3.3V. The inputs are driven by a 3.3V LVPECL driver and an LVDS driver. Two examples of LVPECL output terminations are shown in this schematic.

Selection of either the two pole or three pole filter is based on the application. A three pole loop filter is used for the greater reduction of 8kHz or 10kHz phase detector spurs relative to that afforded by a two pole loop filter. These spurs are generated when the input reference contains low frequency jitter in the pass band of the closed loop response. So for example if the 813N2532 is placed downstream from an IDT WAN PLL, then this jitter will not be present, allowing a two pole filter to be used. If however the 813N2532 is used to directly jitter attenuate a line recovered clock, then a three pole filter must be used. It is recommended that the loop filter components be laid out for the 3-pole option. With a three pole layout, the two pole filter option is preserved by depopulating C3 and setting R3 = 0. The loop filter components should be laid out on the 813N2532 side of the PCB directly adjacent to the LF0 and LF1 pins.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 813N2532 provides separate $V_{CC}$, $V_{CCA}$, $V_{CCX}$ and $V_{CCO}$ power supplies for each jitter attenuator to isolate any high switching noise from coupling into the internal PLLs.

In order to achieve the best possible filtering, it is highly recommended that the 0.1uF capacitors on the device side of the ferrite beads be placed on the device side of the PCB as close to the power pins as possible. This is represented by the placement of these capacitors in the schematic. If space is limited, the ferrite beads, 10µF and 0.1µF capacitor connected to 3.3V can be placed on the opposite side of the PCB. If space permits, place all filter components on the device side of the board.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

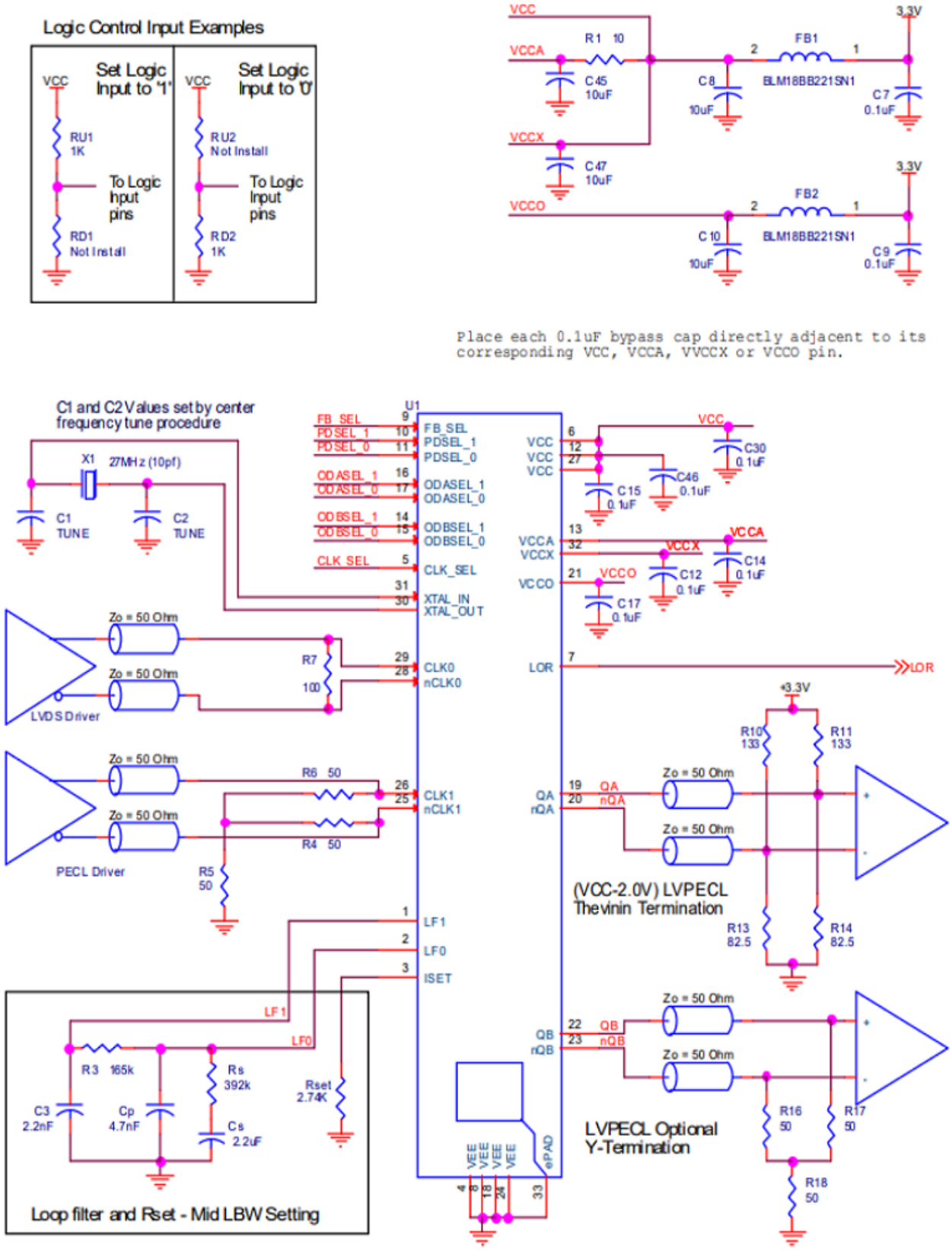



**Figure 5. 813N2532 Schematic Example**

# Power Considerations

This section provides information on power dissipation and junction temperature for the 813N2532.
Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 813N2532 is the sum of the core power plus the power dissipated due to loading.
The following is the power dissipation for $V_{CCO}$ = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated due to loading.

- Power $(core)_{MAX}$ = $V_{CCO\_MAX}$ * $I_{EE\_MAX}$ = 3.465V * 312mA = **1081.1mW**
- Power $(outputs)_{MAX}$ = **31.55mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 31.55mW = **63.1mW**

**Total Power_**$_{MAX}$ (3.465V, with all outputs switching) = 1081.1mW + 63.1mW = **1144.2mW**

### 2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 33.1°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 1.1442W * 33.1°C/W = 107.9°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 6. Thermal Resistance $\theta_{JA}$ for 32 Lead VFQFN, Forced Convection**

| $\theta_{JA}$ by Velocity | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **3** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 33.1°C/W | 28.1°C/W | 25.4°C/W |

**3. Calculations and Equations.**

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 6.*

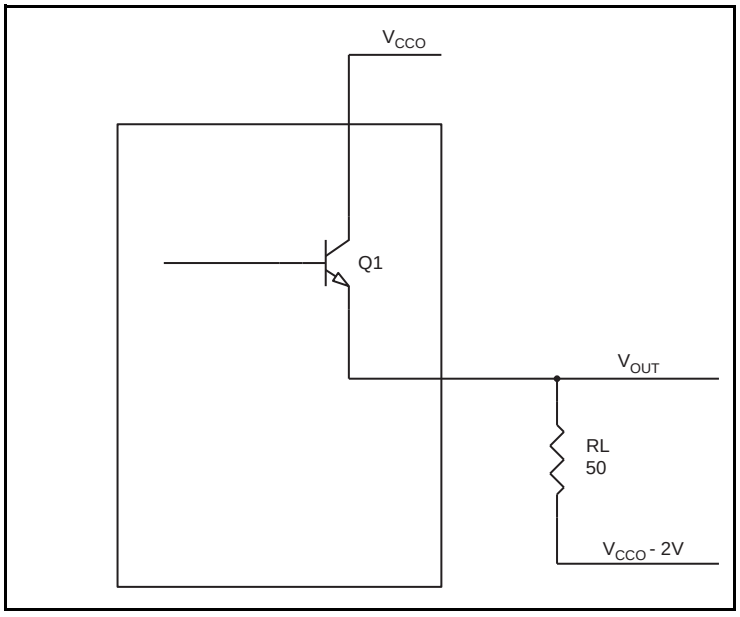



**Figure 6. LVPECL Driver Circuit and Termination**

To calculate power dissipation per output pair due to loading, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO}$ – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} =$ **$V_{CCO\_MAX}$ – 0.75V**
  ($V_{CC\_MAX} – V_{OH\_MAX}$) = **0.75V**
- For logic low, $V_{OUT} = V_{OL\_MAX} =$ **$V_{CCO\_MAX}$ – 1.6V**
  ($V_{CC\_MAX} – V_{OL\_MAX}$) = **1.6V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V– (V_{CCO\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) =$
$[(2V– 0.75V)/50Ω] * 0.75V =$ **18.75mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.6V)/50Ω] * 1.6V =$ **12.80mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **31.55mW**

# Reliability Information

**Table 7. $\theta_{JA}$ vs. Air Flow Table for a 32 Lead VFQFN**

| $\theta_{JA}$ vs. Air Flow | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **3** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 33.1°C/W | 28.1°C/W | 25.4°C/W |

## Transistor Count

The transistor count for 813N2532 is: 44,795

# Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.renesas.com/us/en/document/psc/package-outline-drawing-package-code-nlg32p1-32-vfqfpn-50-x-50-x-09-mm-body-05-mm-pitch

# Ordering Information

**Table 9. Ordering Information**

| Part Number | Marking | Package | Shipping Packaging | Temperature Range |
|---|---|---|---|---|
| 813N2532CKLF | ICS3N2532CL | “Lead-Free” 32-VFQFPN | Tray | 0°C to 70°C |
| 813N2532CKLFT | ICS3N2532CL | “Lead-Free” 32-VFQFPN | Tape & Reel | 0°C to 70°C |

## Revision History

| Revision Date | Page | Description of Change |
|---|---|---|
| June 1, 2011 | 5<br>2 | Supply Voltage, $V_{CC.}$ Rating changed from 4.5V min. to 3.63V per Errata NEN-11-03.<br>Correct typo in block diagram from /2 to /3 for PDSEL[2:0]. |
| June 3, 2011 | 1<br>2<br><br>11 | Features Section, deleted SSTL for the Two differential inputs bullet.<br>Corrected block diagram from /3 back to /2 on the PDSEL[1:0]. Removed the connection between the FB_SEL line and the PDSEL[1:0] line.<br>Clock Input Interface Section, deleted all references to SSTL |
| August 3, 2012 | 1<br>5<br><br>7<br><br>13<br>16<br><br><br>17<br><br>18<br>19 | Features: Updated RMS Phase Jitter data to reflect RMS Phase Jitter data in Table 5<br>Analog Supply Voltage. Changed from $V_{CC}$-0.31V to $V_{CC}$-0.29V, Power Supply Current changed from 300mA to 312mA, Analog Supply Current changed from 31mA to 29mA.<br>RMS Phase Jitter, 156.25MHz changed 0.6ps to 0.64ps, RMS Phase Jitter, 155.52MHz changed 0.622ps to 0.644ps, RMS Phase Jitter, 125MHz changed 0.6ps to 0.66ps.<br>Jitter Attenuator Char Table: changed kVCXO - 2.79 kHz/V Typical to 2.02 Typical kHz/V<br>Power Considerations: changed IEE_MAX = 300mA to 312mA; 1039.55mW to 1081.1mW; Total Power_MAX CHANGED 1039.55mW to 1081.1mW, 1102.65mW 1144.2mW. Tj changed 1.103W and 106.5C to 1.1442W and 107.9C.<br>Changed text: “To calculate worst case power dissipation into the load” to “To calculate power dissipation per output pair due to loading”.<br>Changed transistor count from 44,832 to 44,795.<br>Changed part order number and marking from Rev A to Rev C. Deleted count for Tape and Reel. Deleted Lead-Free note. |
| September 21, 2012 | 10<br>14<br><br>17, 18 | Updated Wiring the Differential Input to Accept Single-Ended Levels text and schematic.<br>Jitter Attenuator Characteristics Table: $k_{VCXO}$ 2.78kHz/V.<br>Added Jitter Attenuator Loop Bandwidth Selection Tables: 2nd and 3rd Order Loop Filter.<br>Replaced text and schematic. |
| October 2, 2013 | 10<br>14 | Applications Information - deleted *Power Supply Filtering Techniques* application note. It is included in the schematic example on page 17.<br>Jitter Attenuator Loop Bandwidth Selection Table ($3^{RD}$ Order Loop Filter):<br>corrected C3 (kΩ) heading to C3(µF). |
| April 8, 2016 | | Deleted “ICS” prefix from part number through out the datasheet.<br>Updated datasheet header/footer. |
| September 19, 2019 | | Updated the schematic diagram in Figure 5<br>Updated the package outline drawings; however, no technical changes were made |
| February 3, 2023 | | Updated package drawing link in Package Outline Drawings. |

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