VCXO W/3.3V, 2.5V LVPECL FemtoClock™ PLL

813321-04

PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES MAY 6, 2017

DATASHEET

General Description

The 813321-04 is a two stage device – a VCXO followed by a FemtoClock™ PLL. The FemtoClock PLL can multiply the crystal frequency of the VCXO up to a range of 122MHz to 160MHz, with a random rms phase jitter of less than 1ps (1.875MHz – 20MHz). This phase jitter performance meets the requirements of 1Gb/10Gb Ethernet, 1Gb, 2Gb, 4Gb and 10Gb Fibre Channel, and SONET up to OC48.

Features

- One 3.3V or 2.5V LVPECL output pair
- Crystal operating frequency range: 14MHz - 20MHz
- VCO range: 490MHz - 640MHz
- Output frequency range: 122MHz - 160MHz
- VCXO pull range: ±50ppm (typical APR) @ 3.3V
- Supports the following applications (among others): SONET, Ethernet, Fibre Channel
- RMS phase jitter @ 156.25MHz (1.875MHz - 20MHz): 0.53ps (typical) @ 3.3V
- Supply voltage modes:

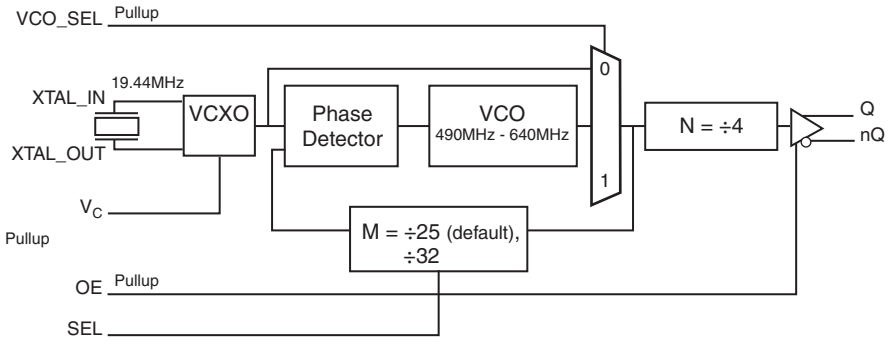
  V_{CC}/V_{CCO}

  3.3V/3.3V

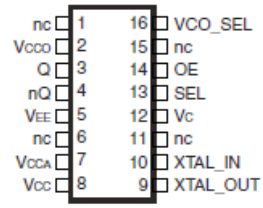
  3.3V/2.5V

  2.5V/2.5V
- 0°C to 70°C ambient operating temperature
- Available in both lead-free (RoHS 6) package
- For functional replacement part use 8N3QV01EG-0016CDI

Block Diagram



Pin Assignment



813321-04

16-Lead TSSOP

4.4mm x 5.0mm x 0.92mm package body

G Package

Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 6, 11, 15	nc	Unused		No connect.
2	V_{CCO}	Power		Output supply pin.
3, 4	Q, nQ	Output		Differential clock outputs. LVPECL interface levels.
5	V_{EE}	Power		Negative supply pin.
7	V_{CCA}	Power		Analog supply pin.
8	V_{CC}	Power		Core supply pin.
9, 10	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
12	V_C	Input		VCXO control voltage input.
13	SEL	Input	Pulldown	Select pin. LVCMOS/LVTTL interface levels. See Table 3.
14	OE	Input	Pullup	Output enable pin. When HIGH, the output is active. When LOW, the output is in a high impedance state. LVCMOS/ LVTTL interface.
16	VCO_SEL	Input	Pullup	VCO select pin. LVCMOS/LVTTL interface levels.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics Table, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Table 3. SEL Function Table

Control Input	M
SEL	
0	÷25 (defalut)
1	÷32

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL)	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	92.4°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.10	3.3	V_{CC}	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{CCA}	Analog Supply Current				10	mA
I_{EE}	Power Supply Current				130	mA

Table 4B. Power Supply DC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $V_{CCO} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.10	3.3	V_{CC}	V
V_{CCO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{CCA}	Analog Supply Current				10	mA
I_{EE}	Power Supply Current				130	mA

Table 4C. Power Supply DC Characteristics, $V_{CC} = V_{CCO} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.375	2.5	2.625	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.10	2.5	V_{CC}	V
V_{CCO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{CCA}	Analog Supply Current				10	mA
I_{EE}	Power Supply Current				125	mA

TABLE 4D. LVCMOS / LVTTL DC CHARACTERISTICS, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
				1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
				-0.3		0.7	V
I_{IH}	Input High Current	OE, VCO_SEL				5	µA
		SEL				150	µA
I_{IL}	Input Low Current	OE, VCO_SEL		-150			µA
		SEL		-5			µA

TABLE 4E. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCO}$ = 3.3V±5%, V_{EE} = 0V, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50 to V_{CCO} - 2V.

TABLE 4F. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V±5% OR 2.5V±5%, V_{CCO} = 2.5V±5%, V_{EE} = 0V, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.5	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.4		1.0	V

NOTE 1: Outputs terminated with 50 to V_{CCO} - 2V.

TABLE 5A. AC CHARACTERISTICS, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	VCO_SEL = 1	122		160	MHz
tjit(Ø)	RMS Phase Jitter, (Random); NOTE 1, 2	155.52MHz (1.875MHz - 20MHz)		0.53		ps
f_{VCO}	PLL VCO Lock Range		490		640	MHz
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		600	ps
odc	Output Duty Cycle		48		52	%

NOTE 1: Phase jitter using a crystal interface.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, $V_{CC} = 3.3V \pm 5\%$, $V_{CCO} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	VCO_SEL = 1	122		160	MHz
tjit(Ø)	RMS Phase Jitter, (Random); NOTE 1, 2	155.52MHz (1.875MHz - 20MHz)		0.64		ps
f_{VCO}	PLL VCO Lock Range		490		640	MHz
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		600	ps
odc	Output Duty Cycle		48		52	%

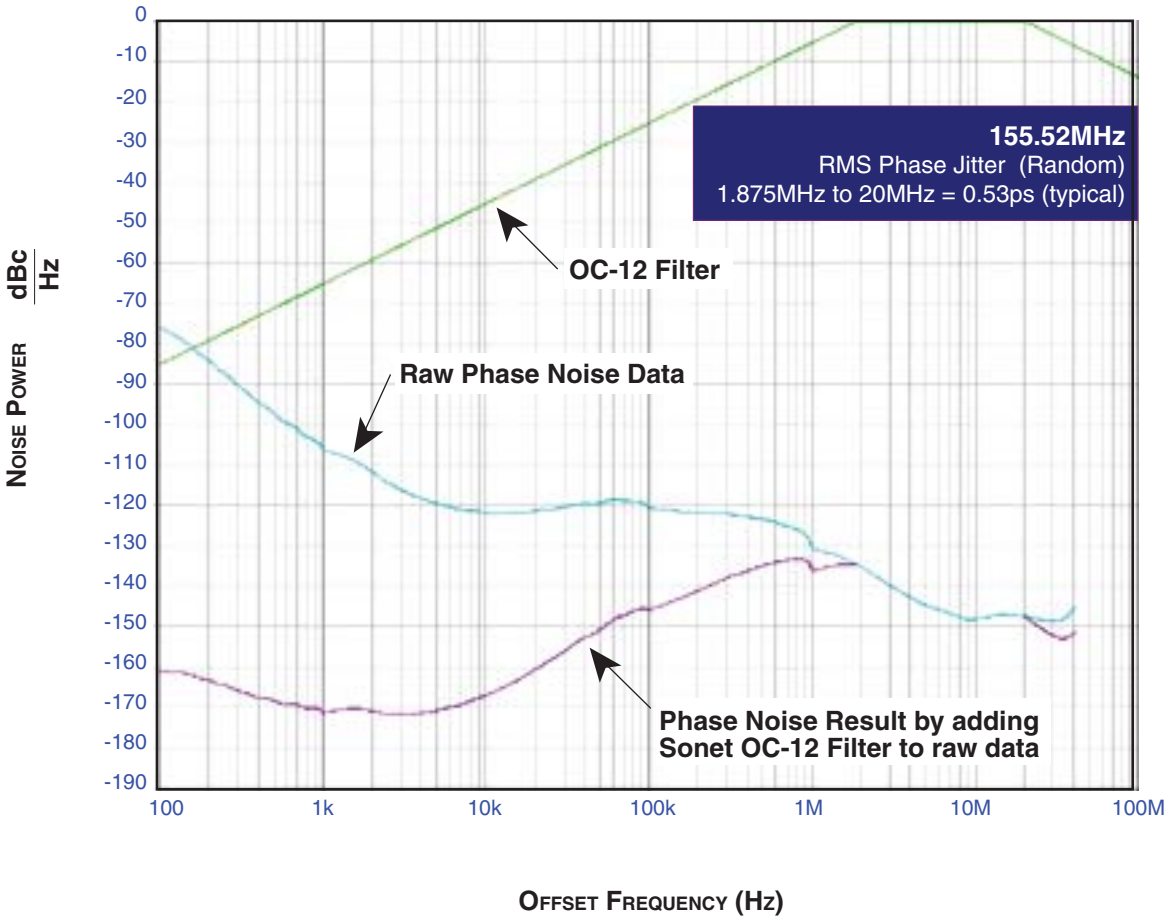
NOTE 1: Phase jitter using a crystal interface.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5C. AC CHARACTERISTICS, $V_{CC} = V_{CCO} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0°C$ TO $70°C$

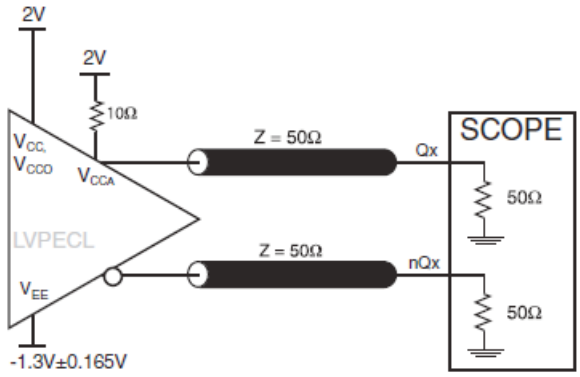
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	VCO_SEL = 1	122		160	MHz
tjit(Ø)	RMS Phase Jitter, (Random); NOTE 1, 2	155.52MHz (1.875MHz - 20MHz)		0.53		ps
f_{VCO}	PLL VCO Lock Range		490		640	MHz
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		600	ps
odc	Output Duty Cycle		48		52	%

NOTE 1: Phase jitter using a crystal interface.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

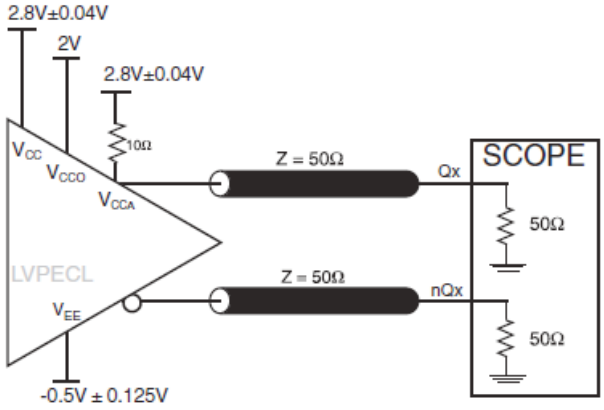
Typical Phase Noise at 155.52MHz



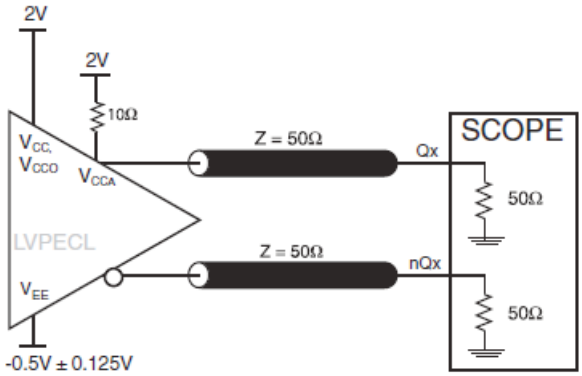
Parameter Measurement Information



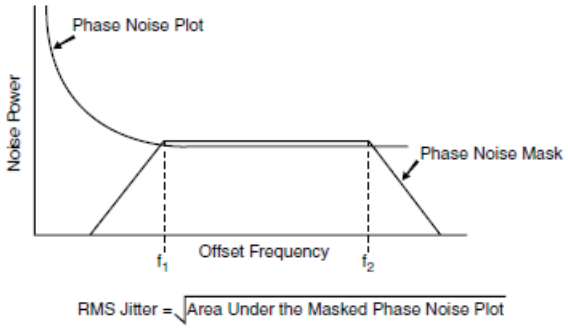
3.3V Core/3.3V LVPECL Output Load AC Test Circuit



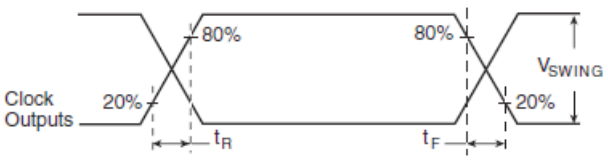
3.3V Core/2.5V LVPECL Output Load AC Test Circuit



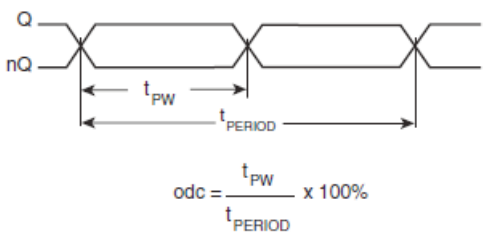
2.5V Core/2.5V LVPECL Output Load AC Test Circuit



RMS Phase Jitter



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 813321-04 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional10Ω resistor along with a 10µF bypass capacitor be connected to the V_{CCA} pin.

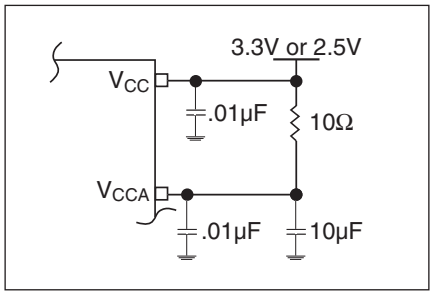


FIGURE 1. POWER SUPPLY FILTERING

RECOMMENDATIONS FOR UNUSED INPUT PINS

INPUTS:

LVCMOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Termination for 3.3V LVPECL Output

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

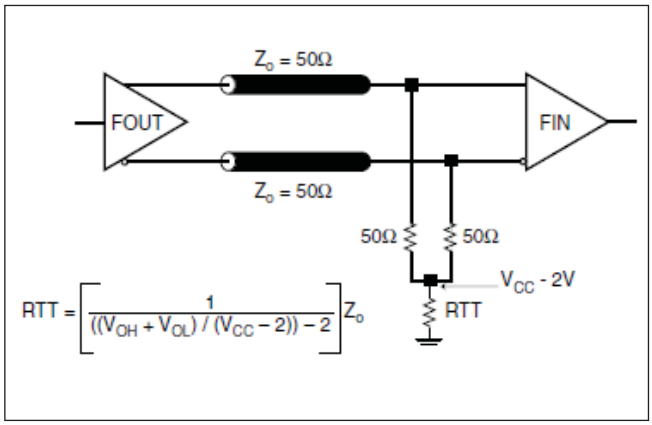


Figure 2A. LVPECL Output Termination

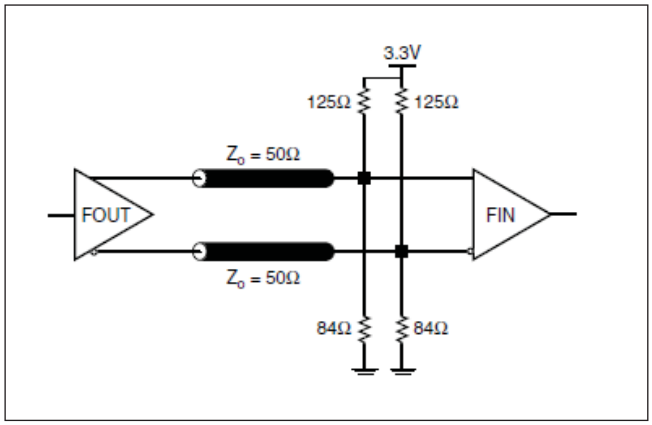


Figure 2B. LVPECL Output Termination

Termination for 2.5V LVPECL Output

Figure 3A and *Figure 3B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{cc} - 2V. For V_{cco} = 2.5V, the V_{cco} - 2V is very close to ground level. The R3 in Figure 3B can be eliminated and the termination is shown in *Figure 3C*.

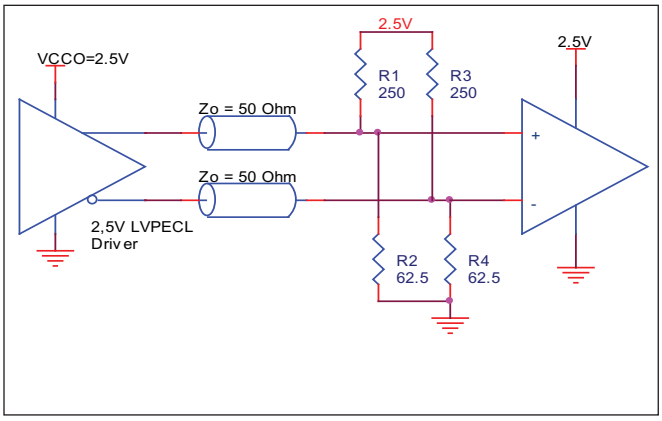


Figure 3A. 2.5V LVPECL Driver Termination Example

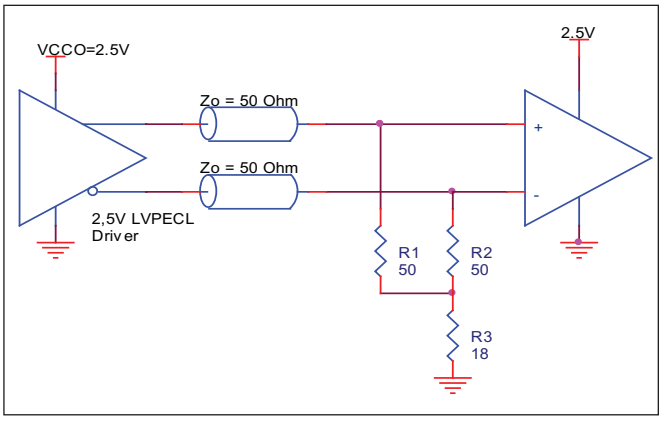


Figure 3B. 2.5V LVPECL Driver Termination Example

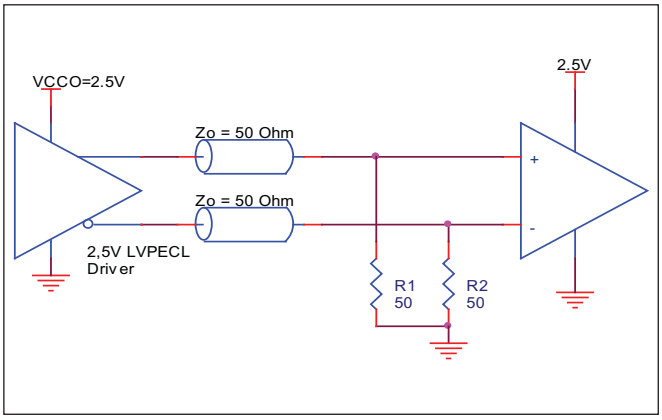
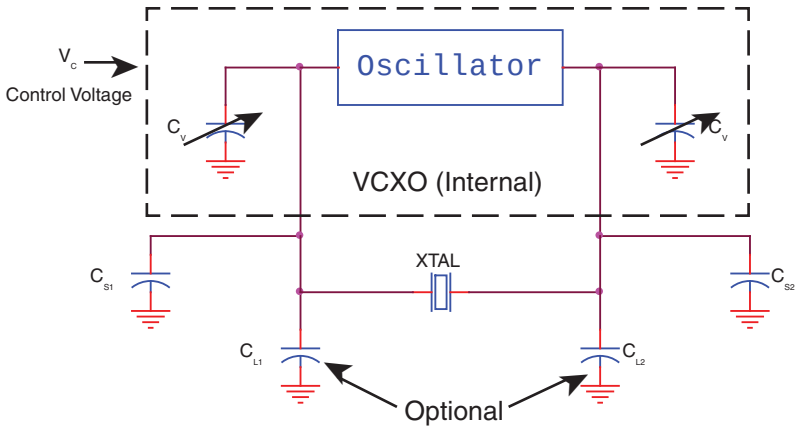


Figure 3C. 2.5V LVPECL Termination Example

VCXO Crystal Selection

Choosing a crystal with the correct characteristics is one of the most critical steps in using a Voltage Controlled Crystal Oscillator (VCXO). The crystal parameters affect the tuning range and accuracy of a VCXO. Below are the key variables and an example of using the crystal parameters to calculate the tuning range of the VCXO.



V_C - Control voltage used to tune frequency

C_V - Varactor capacitance, varies due to the change in control voltage

C_{L1}, C_{L2} - Load tuning capacitance used for fine tuning or centering nominal frequency

C_{S1}, C_{S2} - Stray Capacitance caused by pads, vias, and other board parasitics

Figure 4. VCXO Oscillator Circuit

Table 6. Example Crystal Parameters

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_N	Nominal Frequency		14		20	MHz
f_T	Frequency Tolerance				±20	ppm
f_S	Frequency Stability				±20	ppm
	Operating Temperature Range		0		70	°C
C_L	Load Capacitance			12		pF
C_O	Shunt Capacitance			4		pF
C_1, C_2	Pullability Ratio			220	240	
ESR	Equivalent Series Resistance				20	
	Drive Level				1	mW
	Aging @ 25°C		±3 per year			ppm
	Mode of Operation		Fundamental			

TABLE 7. VARACTOR PARAMETERS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{V_LOW}	Low Varactor Capacitance	V_C = 0V		6		pF
C_{V_HIGH}	High Varactor Capacitance	V_C = 3.3V		11		pF

FORMULAS

$$C_{Low} = \frac{(C_{L1} + C_{S1} + C_{V\_Low}) \cdot (C_{L2} + C_{S2} + C_{V\_Low})}{(C_{L1} + C_{S1} + C_{V\_Low}) + (C_{L2} + C_{S2} + C_{V\_Low})}$$

$$C_{High} = \frac{(C_{L1} + C_{S1} + C_{V\_High}) \cdot (C_{L2} + C_{S2} + C_{V\_High})}{(C_{L1} + C_{S1} + C_{V\_High}) + (C_{L2} + C_{S2} + C_{V\_High})}$$

- C_{Low} is the effective capacitance due to the low varactor capacitance, load capacitance and stray capacitance. C_{Low} determines the high frequency component on the TPR.
- C_{High} is the effective capacitance due to the high varactor capacitance, load capacitance and stray capacitance. C_{High} determines the low frequency component on the TPR.

$$Total\ Pull\ Range\ (TPR) = \left(\frac{1}{2 \cdot C_0/C_1 \cdot \left(1 + C_{Low}/C_0\right)} - \frac{1}{2 \cdot C_0/C_1 \cdot \left(1 + C_{High}/C_0\right)} \right) \cdot 10^6$$

Absolute Pull Range (APR) = Total Pull Range – (Frequency Tolerance + Frequency Stability + Aging)

EXAMPLE CALCULATIONS

Using the tables and figures above, we can now calculate the TPR and APR of the VCXO using the example crystal parameters. For the numerical example below there were some assumptions made. First, the stray capacitance (C_{S1}, C_{S2}), which is all the excess capacitance due to board parasitic, is 4pF. Second, the expected lifetime of the project is 5 years; hence the inaccuracy due to aging is ±15ppm. Third, though many boards will not require load tuning capacitors (C_{L1}, C_{L2}), it is recommended for long-term consistent performance of the system that two tuning capacitor pads be placed into every design. Typical values for the load tuning capacitors will range from 0 to 4pF.

$$C_{Low} = \frac{(0 + 4pf + 15pf) \cdot (0 + 4pf + 15pf)}{(0 + 4pf + 15pf) \cdot (0 + 4pf + 15pf)} = 9.5pf$$

$$C_{High} = \frac{(0 + 4pf + 27.4pf) \cdot (0 + 4pf + 27.4pf)}{(0 + 4pf + 27.4pf) \cdot (0 + 4pf + 27.4pf)} = 15.7pf$$

$$TPR = \left(\frac{1}{2 \cdot 220 \cdot \left(1 + 9.5pf/4pf\right)} - \frac{1}{2 \cdot 220 \cdot \left(1 + 15.7pf/4pf\right)} \right) \cdot 10^6 = 212\text{ppm}$$

TPR = ±106ppm
APR = 106ppm – (20ppm + 20ppm + 15ppm) = ±51ppm

The example above will ensure a total pull range of ±106 ppm with an APR of ±51ppm. Many times, board designers may select their own crystal based on their application. If the application requires a tighter APR, a crystal with better pullability (C0/C1 ratio) can be used. Also, with the equations above, one can vary the frequency tolerance, temperature stability, and aging or shunt capacitance to achieve the required pullability.

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 813321-04.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the 813321-04 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 130mA = **450mW**

  Total Power$_{_MAX}$ (3.465V, with output switching) = 450mW + 30mW = **480mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 92.4°C/W per Table 8 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.480W * 92.4°C/W = 114.4°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 8. THERMAL RESISTANCE θ_{JA} FOR 16-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	92.4°C/W	88.0°C/W	75.91°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 5.*

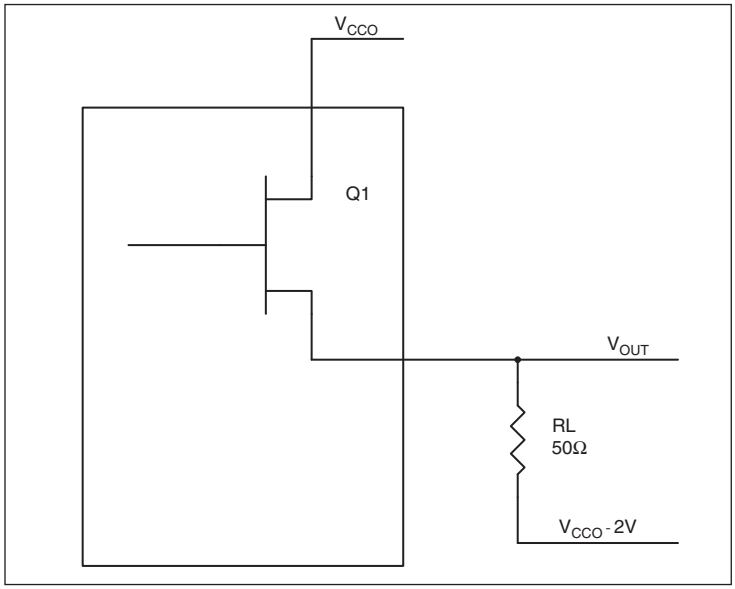


FIGURE 5. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{cco} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$

$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 9. θ_{JA} vs. Air Flow Table for 16 Lead TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	92.4°C/W	88.0°C/W	75.91°C/W

Transistor Count

The transistor count for 813321-04 is: 3948

Package Outline - G Suffix for 16 Lead TSSOP

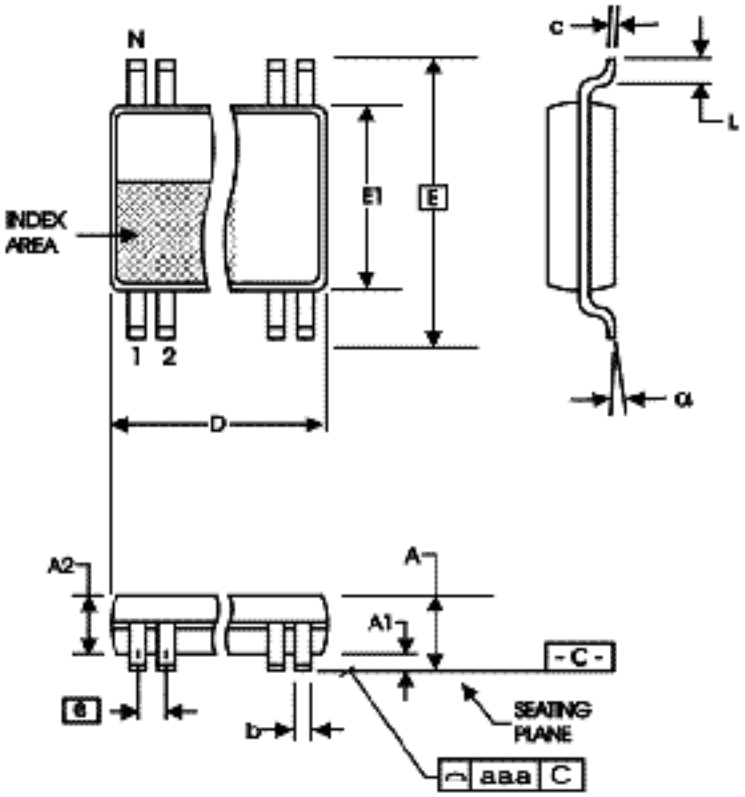


Table 10. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 11. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS813321AG-04LF	3321A04L	16 lead “Lead-Free” TSSOP	tube	0°C to 70°C
ICS813321AG-04LFT	3321A04L	16 lead “Lead-Free” TSSOP	tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T11	17	Removed leaded devices and updated data sheet format	3/19/15
A			Product Discontinuation Notice - Last time buy expires May 6, 2017 PDN CQ-16-01	5/5/16

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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