Dual VCXO w/3.3V, 2.5V LVPECL FemtoClock™ PLL

813001I

DATASHEET

General Description

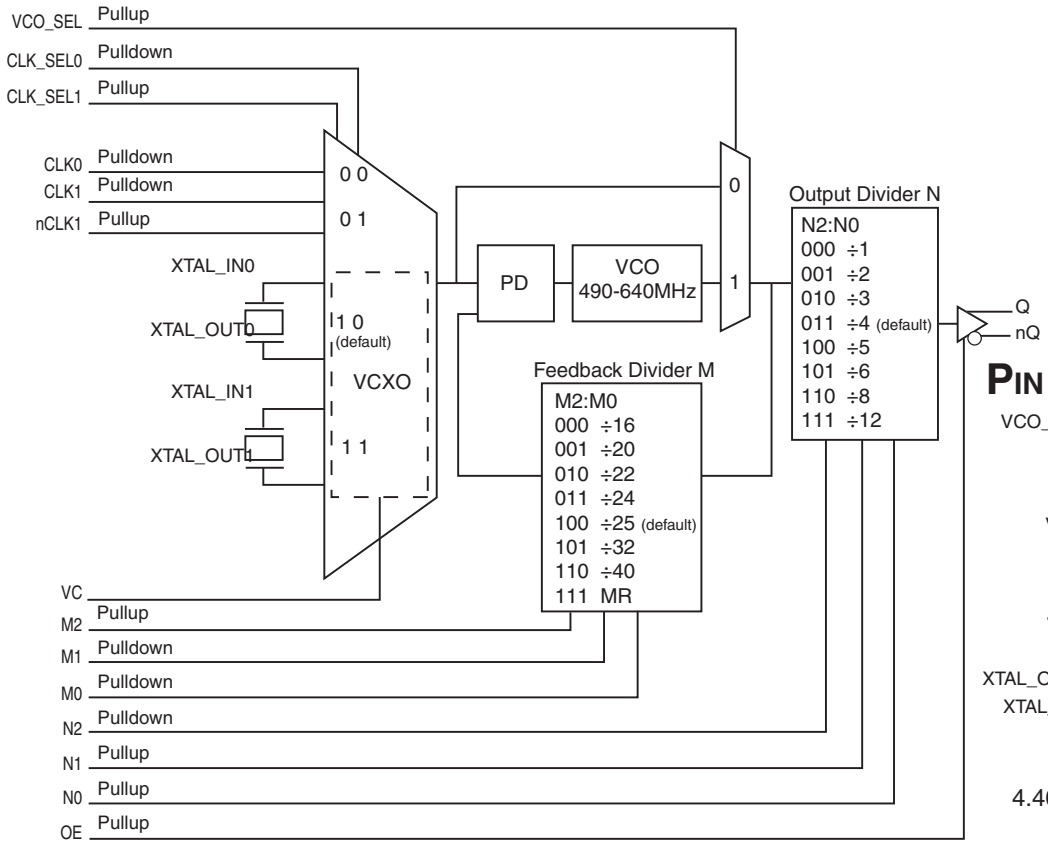
The 813001I is a dual VCXO + FemtoClock™ Multiplier designed for use in Discrete PLL loops. Two selectable external VCXO crystals allow the device to be used in multi-rate applications, where a given line card can be switched, for example, between 1Gb Ethernet (125MHz system reference clock) and 1Gb Fibre Channel (106.25MHz system reference clock) modes. Of course, a multitude of other applications are also possible such as switching between 74.25MHz and 74.175824MHz for HDTV, switching between SONET, FEC and non FEC rates, etc.

The 813001I is a two stage device – a VCXO followed by a FemtoClock PLL. The FemtoClock PLL can multiply the crystal frequency of the VCXO to provide an output frequency range of 40.83MHz to 640MHz, with a random rms phase jitter of less than 1ps (12kHz – 20MHz). This phase jitter performance meets the requirements of 1Gb/10Gb Ethernet, 1Gb, 2Gb, 4Gb and 10Gb Fibre Channel, and SONET up to OC48. The FemtoClock PLL can also be bypassed if frequency multiplication is not required. For testing/debug purposes, de-assertion of the output enable pin will place both Q and nQ in a high impedance state.

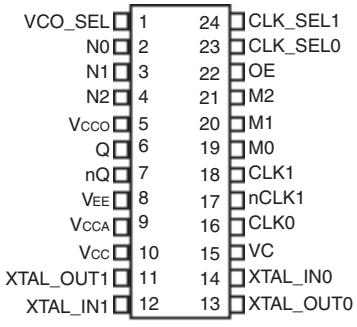
Features

- One 3.3V or 2.5V LVPECL output pair
- Two selectable crystal oscillator interfaces for the VCXO, one differential clock or one LVCMOS/LVTTL clock inputs
- CLK1/nCLK1 supports the following input types: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Crystal operating frequency range: 14MHz - 24MHz
- VCO range: 490MHz - 640MHz
- Output frequency range: 40.83MHz - 640MHz
- VCXO pull range: ±100ppm (typical)
- Supports the following applications (among others): SONET, Ethernet, Fibre Channel, HDTV, MPEG
- RMS phase jitter @ 622.08MHz (12kHz - 20MHz): 0.84 (typical)
- Supply voltage modes:
  V_{CC}/V_{CCO}
  3.3V/3.3V
  3.3V/2.5V
  2.5V/2.5V
- -40°C to 85°C ambient operating temperature
- Available in RoHS/Lead-Free compliant package

Block Diagram



Pin Assignment



813001I
24-Lead TSSOP
4.40mm x 7.8mm x 0.92mm
package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	VCO_SEL	Input	Pullup	VCO select pin. LVCMOS/LVTTL interface levels.
2, 3	N0, N1	Input	Pullup	Output divider select pins. Default value = ÷4. LVCMOS/LVTTL interface levels.
4	N2	Input	Pulldown	
5	V_{CCO}	Power		Output supply pin.
6, 7	Q, nQ	Ouput		Differential output pair. LVPECL interface levels.
8	V_{EE}	Power		Negative supply pin.
9	V_{CCA}	Power		Analog supply pin.
10	V_{CC}	Power		Core supply pin.
11 12	XTAL_OUT1, XTAL_IN1	Input		Parallel resonant crystal interface. XTAL_OUT1 is the output, XTAL_IN1 is the input.
13 14	XTAL_OUT0, XTAL_IN0	Input		Parallel resonant crystal interface. XTAL_OUT0 is the output, XTAL_IN0 is the input.
15	VC	Input		VCXO control voltage input.
16	CLK0	Input	Pulldown	LVCMOS/LVTTL clock input.
17	nCLK1	Input	Pullup	Inverting differential clock input.
18	CLK1	Input	Pulldown	Non-inverting differential clock input.
19, 20	M0, M1	Input	Pulldown	Feedback divider select pins. Default value = ÷25. LVCMOS/LVTTL interface levels.
21	M2	Input	Pullup	
22	OE	Input	Pullup	Output enable. When HIGH, the output is active. When LOW, the output is in a high impedance state. LVCMOS/LVTTL interface levels.
23	CLK_SEL0	Input	Pulldown	Clock select pin. LVCMOS/LVTTL interface levels. Refer to Table 3.
24	CLK_SEL1	Input	Pullup	

NOTE: refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Table 3. Control Input Function Table

Inputs		
CLK_SEL1	**CLK_SEL0**	**Selected Input**
0	0	CLK0
0	1	CLK1, nCLK1
1	0	XTAL0
1	1	XTAL1

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL)	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	70°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				130	mA
I_{CCA}	Analog Supply Current				10	mA

Table 4B. Power Supply DC Characteristics, $V_{CC} = V_{CCA}$ = 3.3V±5%, V_{CCO} = 2.5V±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current				130	mA
I_{CCA}	Analog Supply Current				10	mA

Table 4C. Power Supply DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO}$ = 2.5V±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.375	2.5	2.625	V
V_{CCA}	Analog Supply Voltage		2.375	2.5	2.625	V
V_{CCO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current				125	mA
I_{CCA}	Analog Supply Current				10	mA

TABLE 4C. LVCMOS / LVTTL DC CHARACTERISTICS, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.3V	2.0		V_{CC} + 0.3	V
			V_{CC} = 2.5V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.3V	-0.3		0.8	V
			V_{CC} = 2.5V	-0.3		0.7	V
VC	VCXO Control Voltage			0		V_{CC}	V
I_{IH}	Input High Current	N2, M0, M1, CLK0, CLK_SEL0	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
		N0, N1, M2, VCO_SEL, CLK_SEL1	V_{CC} = V_{IN} = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	N2, M0, M1, CLK0, CLK_SEL0	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
		N0, N1, M2, VCO_SEL, CLK_SEL1	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
I_{VC}	Input Current of V_c pin		V_{CC} = 3.465V or 2.625V	-100		100	µA

TABLE 4D. DIFFERENTIAL DC CHARACTERISTICS, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK1	V_{IN} = V_{CC} = 3.465V or 2.625V			150	µA
		nCLK1	V_{IN} = V_{CC} = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	CLK1	V_{IN} = 0V, V_{CC} = 3.465V or 2.625V	-5			µA
		nCLK1	V_{IN} = 0V, V_{CC} = 3.465V or 2.625V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 0.5		V_{CC} - 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended appliations, the maximum input voltage for CLK1, nCLK1 is V_{CC} + 0.3V.

TABLE 4E. LVPECL DC CHARACTERISTICS, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.

TABLE 5A. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	VCO_SEL = 1	40.83		640	MHz
tjit(Ø)	RMS Phase Jitter, (Random); NOTE 1	622.08MHz (12kHz - 20MHz)		0.84		ps
f_{VCO}	PLL VCO Lock Range		490		640	MHz
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		500	ps
odc	Output Duty Cycle	N ÷ 1	43		57	%
		N ≠ ÷1	48		52	%

NOTE 1: Phase jitter using a crystal interface.

TABLE 5B. AC CHARACTERISTICS, $V_{CC} = V_{CCA}$ = 3.3V±5%, V_{CCO} = 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	VCO_SEL = 1	40.83		640	MHz
tjit(Ø)	RMS Phase Jitter, (Random); NOTE 1	622.08MHz (12kHz - 20MHz)		0.87		ps
f_{VCO}	PLL VCO Lock Range		490		640	MHz
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		500	ps
odc	Output Duty Cycle	N ÷ 1	43		57	%
		N ≠ ÷1	48		52	%

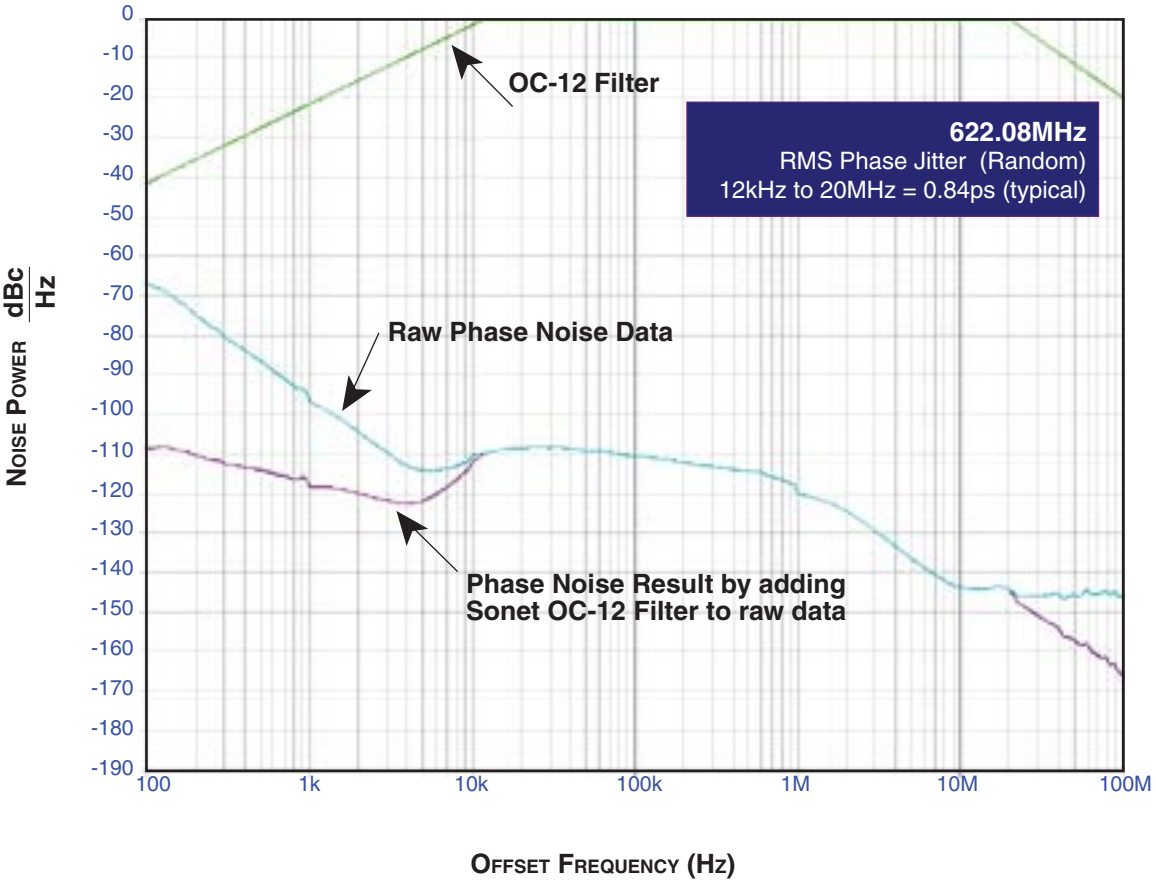
NOTE 1: Phase jitter using a crystal interface.

TABLE 5C. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO}$ = 2.5V±5%, TA = -40°C TO 85°C

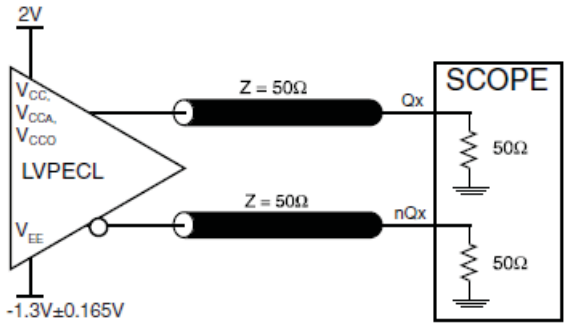
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	VCO_SEL = 1	40.83		640	MHz
tjit(Ø)	RMS Phase Jitter, (Random); NOTE 1	622.08MHz (12kHz - 20MHz)		1.2		ps
f_{VCO}	PLL VCO Lock Range		490		640	MHz
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		500	ps
odc	Output Duty Cycle	N ÷ 1	43		57	%
		N ≠ ÷1	48		52	%

NOTE 1: Phase jitter using a crystal interface.

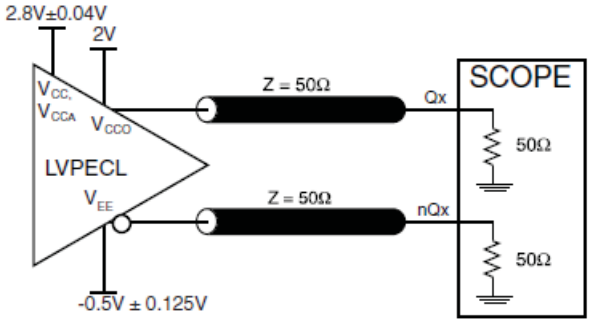
Typical Phase Noise at 622.08MHz @ 3.3V



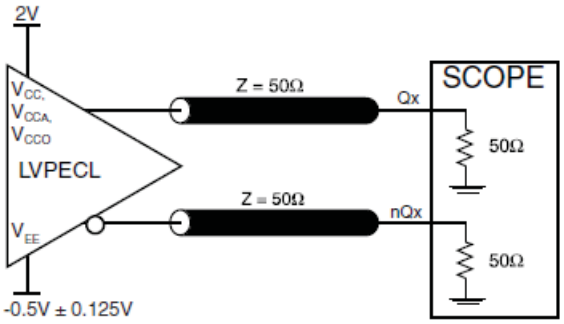
PARAMETER MEASUREMENT INFORMATION



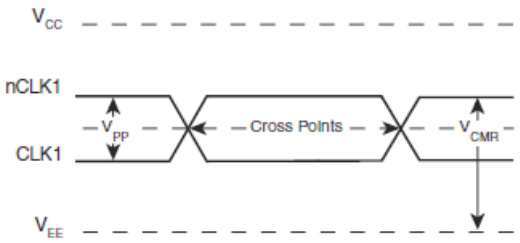
3.3V CORE/3.3V LVPECL OUTPUT LOAD AC TEST CIRCUIT



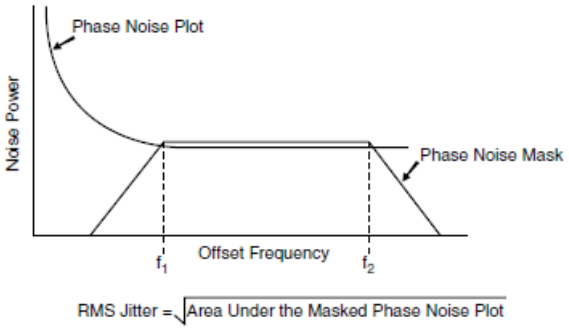
3.3V CORE/2.5V LVPECL OUTPUT LOAD AC TEST CIRCUIT



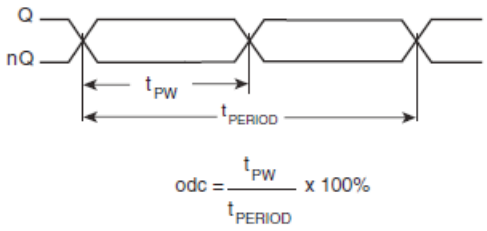
2.5V CORE/2.5V LVPECL OUTPUT LOAD AC TEST CIRCUIT



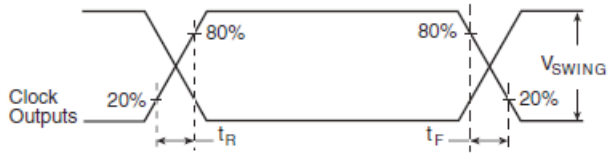
DIFFERENTIAL INPUT LEVELS



RMS PHASE JITTER



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 813001I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA}.

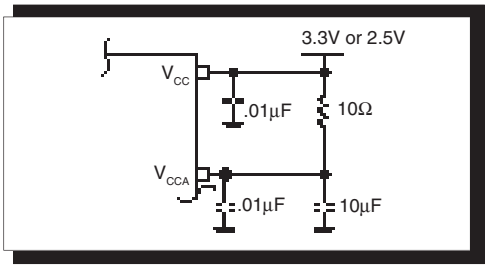


FIGURE 1. POWER SUPPLY FILTERING

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{CC}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

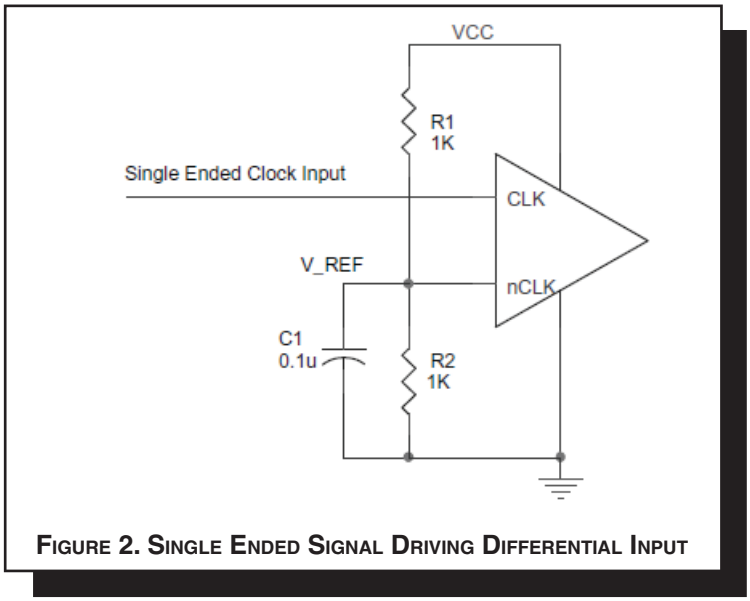
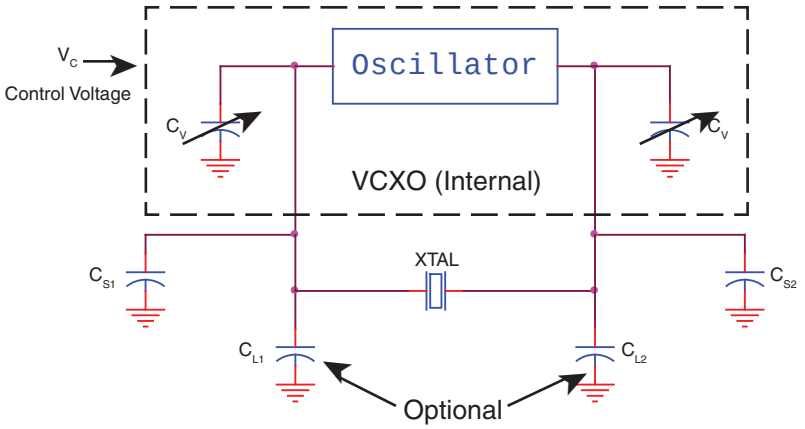


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

VCXO Crystal Selection

Choosing a crystal with the correct characteristics is one of the most critical steps in using a Voltage Controlled Crystal Oscillator (VCXO). The crystal parameters affect the tuning range and accuracy of a VCXO. Below are the key variables and an example of using the crystal parameters to calculate the tuning range of the VCXO.



V_C - Control voltage used to tune frequency

C_V - Varactor capacitance, varies due to the change in control voltage

C_{L1}, C_{L2} - Load tuning capacitance used for fine tuning or centering nominal frequency

C_{S1}, C_{S2} - Stray Capacitance caused by pads, vias, and other board parasitics

Figure 3. VCXO Oscillator Circuit

Table 6. Example Crystal Parameters

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_N	Nominal Frequency		14		24	MHz
f_T	Frequency Tolerance				±20	ppm
f_S	Frequency Stability				±20	ppm
	Operating Temperature Range		0		70	°C
C_L	Load Capacitance			12		pF
C_O	Shunt Capacitance			4		pF
C_1, C_2	Pullability Ratio			220	240	
ESR	Equivalent Series Resistance				20	
	Drive Level				1	mW
	Aging @ 25°C		±3 per year			ppm
	Mode of Operation		Fundamental			

Table 7. Varactor Parameters

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{V_LOW}	Low Varactor Capacitance	V_C = 0V		15		pF
C_{V_HIGH}	High Varactor Capacitance	V_C = 3.3V		27.4		pF

Formulas

$$C_{Low} = \frac{(C_{L1} + C_{S1} + C_{V\_Low}) \cdot (C_{L2} + C_{S2} + C_{V\_Low})}{(C_{L1} + C_{S1} + C_{V\_Low}) + (C_{L2} + C_{S2} + C_{V\_Low})}$$

$$C_{High} = \frac{(C_{L1} + C_{S1} + C_{V\_High}) \cdot (C_{L2} + C_{S2} + C_{V\_High})}{(C_{L1} + C_{S1} + C_{V\_High}) + (C_{L2} + C_{S2} + C_{V\_High})}$$

- C_{Low} is the effective capacitance due to the low varactor capacitance, load capacitance and stray capacitance. C_{Low} determines the high frequency component on the TPR.
- C_{High} is the effective capacitance due to the high varactor capacitance, load capacitance and stray capacitance. C_{High} determines the low frequency component on the TPR.

$$Total\ Pull\ Range\ (TPR) = \left(\frac{1}{2 \cdot C_0/C_1 \cdot \left(1 + C_{Low}/C_0\right)} - \frac{1}{2 \cdot C_0/C_1 \cdot \left(1 + C_{High}/C_0\right)} \right) \cdot 10^6$$

Absolute Pull Range (APR) = Total Pull Range – (Frequency Tolerance + Frequency Stability + Aging)

Example Calculations

Using the tables and figures above, we can now calculate the TPR and APR of the VCXO using the example crystal parameters. For the numerical example below there were some assumptions made. First, the stray capacitance (C_{S1}, C_{S2}), which is all the excess capacitance due to board parasitic, is 4pF. Second, the expected lifetime of the project is 5 years; hence the inaccuracy due to aging is ±15ppm. Third, though many boards will not require load tuning capacitors (C_{L1}, C_{L2}), it is recommended for long-term consistent performance of the system that two tuning capacitor pads be placed into every design. Typical values for the load tuning capacitors will range from 0 to 4pF.

$$C_{Low} = \frac{(0 + 4pf + 15pf) \cdot (0 + 4pf + 15pf)}{(0 + 4pf + 15pf) \cdot (0 + 4pf + 15pf)} = 9.5pf$$

$$C_{High} = \frac{(0 + 4pf + 27.4pf) \cdot (0 + 4pf + 27.4pf)}{(0 + 4pf + 27.4pf) \cdot (0 + 4pf + 27.4pf)} = 15.7pf$$

$$TPR = \left(\frac{1}{2 \cdot 220 \cdot \left(1 + 9.5pf/4pf\right)} - \frac{1}{2 \cdot 220 \cdot \left(1 + 15.7pf/4pf\right)} \right) = \cdot 10^6 \cdot = 212\text{ppm}$$

TPR = ±106ppm
APR = 106ppm – (20ppm + 20ppm + 15ppm) = ±51ppm

The example above will ensure a total pull range of ±106 ppm with an APR of ±51ppm. Many times, board designers may select their own crystal based on their application. If the application requires a tighter APR, a crystal with better pullability (C0/C1 ratio) can be used. Also, with the equations above, one can vary the frequency tolerance, temperature stability, and aging or shunt capacitance to achieve the required pullability.

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 4A to4E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 4A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

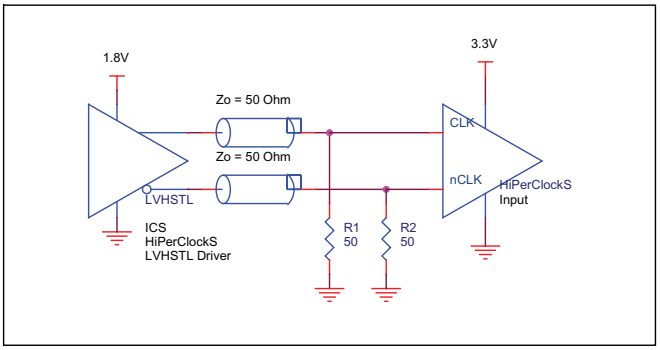


Figure 4A. CLK/nCLK Input Driven by ICS HiPerClockS LVHSTL Driver

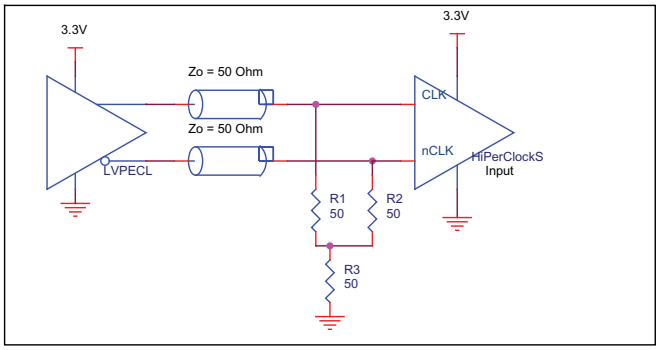


Figure 4B. CLK/nCLK Input Driven by 3.3V LVPECL Driver

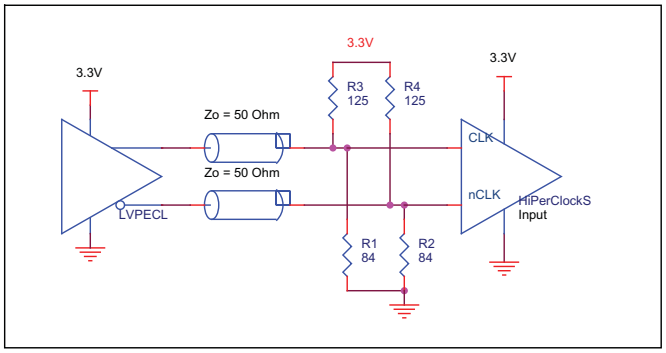


Figure 4C. CLK/nCLK Input Driven by 3.3V LVPECL Driver

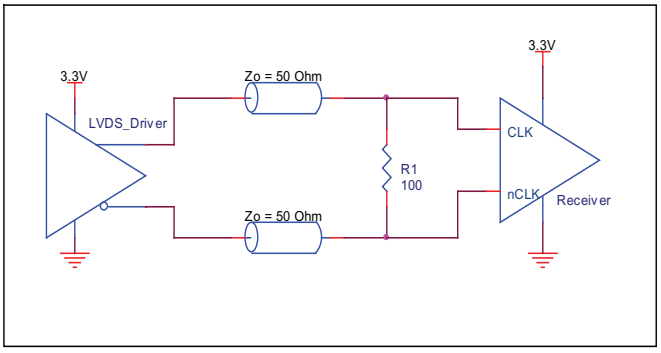


Figure 4D. CLK/nCLK Input Driven by 3.3V LVDS Driver

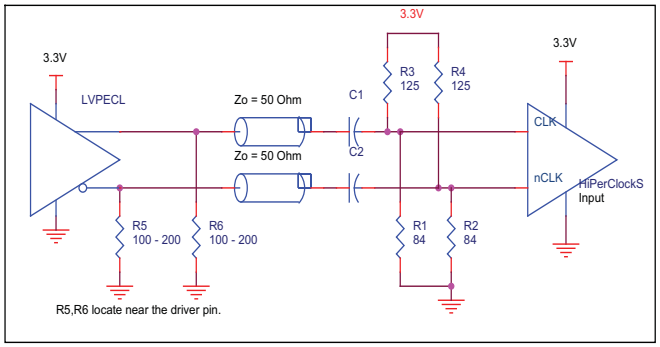


Figure 4E. CLK/nCLK Input Driven by 3.3V LVPECL Driver with AC Couple

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Input:
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

CLK Input:
For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

CLK/nCLK Input:
For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS Control Pins:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

VC input pin - do not float, must be biased.

Outputs:

LVPECL Output
All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Output

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

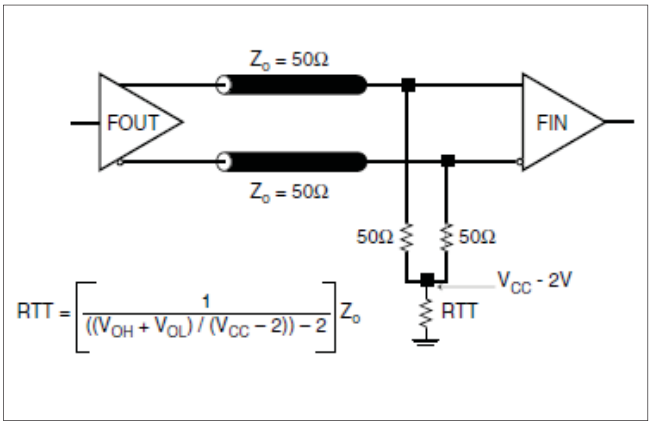


Figure 5A. LVPECL Output Termination

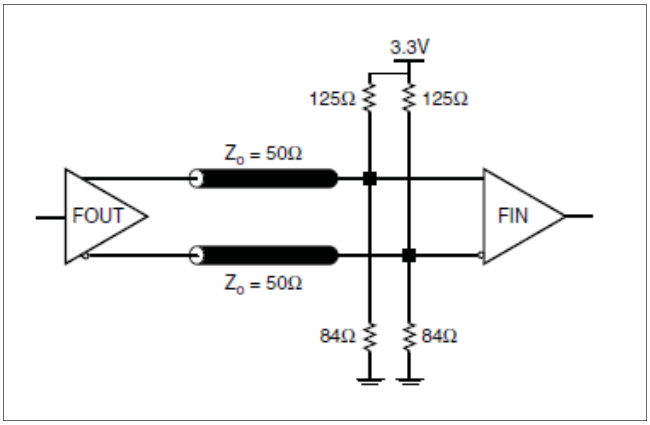


Figure 5B. LVPECL Output Termination

Termination for 2.5V LVPECL Output

Figure 6A and *Figure 6B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CCO} = 2.5V, the V_{CCO} - 2V is very close to ground level. The R3 in Figure 6B can be eliminated and the termination is shown in *Figure 6C.*

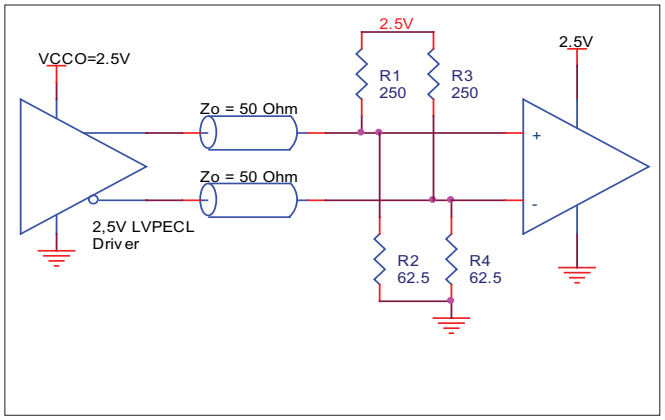


Figure 6A. 2.5V LVPECL Driver Termination Example

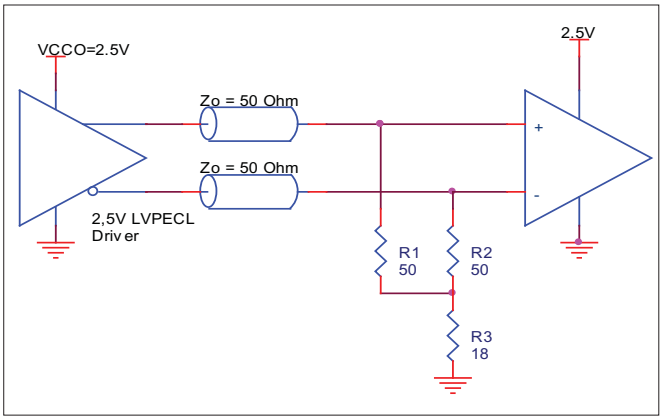


Figure 6B. 2.5V LVPECL Driver Termination Example

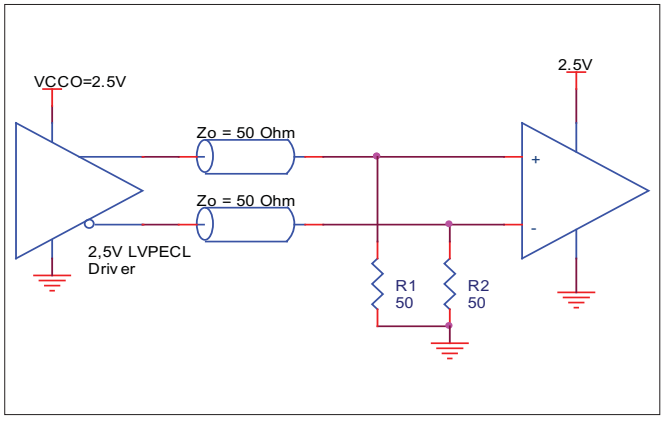


Figure 6C. 2.5V LVPECL Termination Example

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 813001I.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the 813001I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 130mA = **450.45mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**

Total Power$_{_MAX}$ (3.465V, with output switching) = 450.45mW + 30mW = **480.5mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 70°C/W per Table 8 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.481W * 65°C/W = 116.3°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 8. THERMAL RESISTANCE θ_{JA} FOR 24-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 7.*

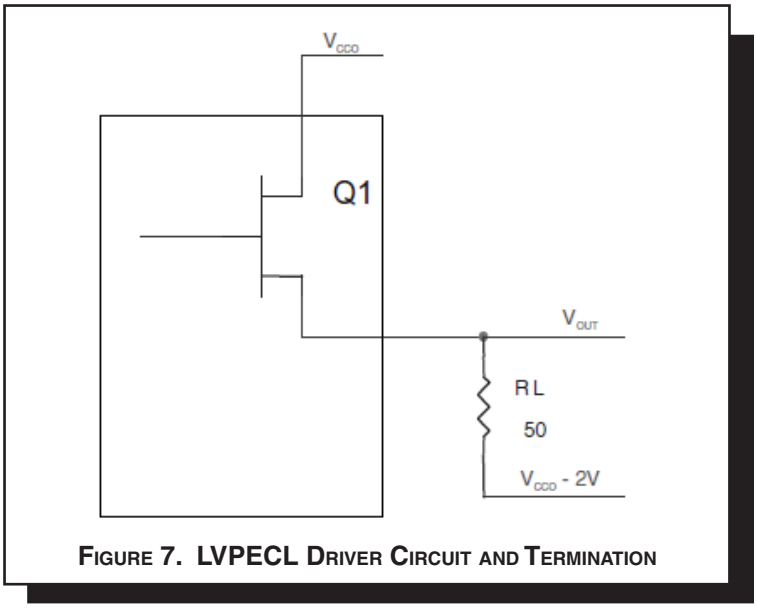


FIGURE 7. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination
voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} – 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} – 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 9. θ_{JA} vs. Air Flow Table for 24 Lead TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

Transistor Count

The transistor count for 813001I is: 3948

Package Outline - G Suffix for 24 Lead TSSOP

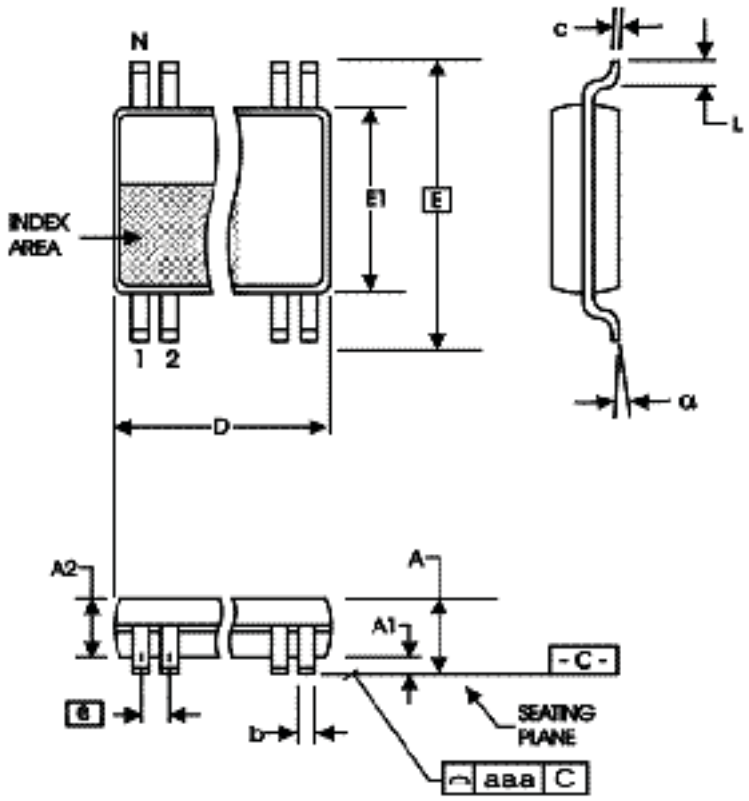


Table 10. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 11. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS813001AGILF	ICS813001AGIL	24 Lead “Lead-Free” TSSOP	tube	-40°C to 85°C
ICS813001AGILFT	ICS813001AGIL	24 Lead “Lead-Free” TSSOP	tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an LF suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T11	18	Ordering information - PDN - removed leaded devices Updated datasheet format	3/17/15

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