General Description

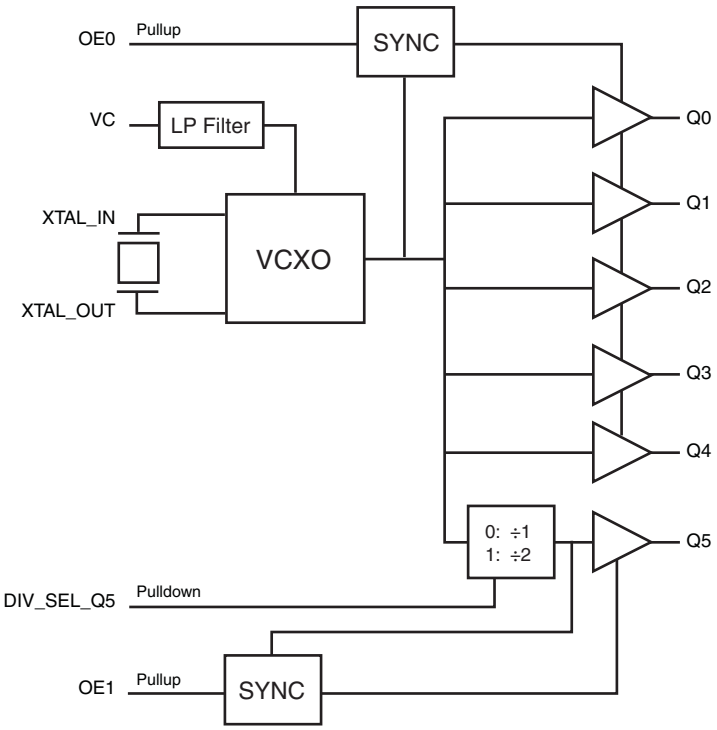
The ICS81006I is a high performance, low jitter/ low phase noise VCXO. The ICS81006I works in conjunction with a pullable crystal to generate an output clock over the range of 12MHz – 31.25MHz and has 6 LVCMOS outputs, effectively integrating a fanout buffer function.

The frequency of the VCXO is adjusted by the VC control voltage input. The output range is ±100ppm around the nominal crystal frequency. The VC control voltage range is 0 – V_{DD}. The device is packaged in a small 4mm x 4mm VFQFN package and is ideal for use on space constrained boards typically encountered in ADSL/VDSL applications.

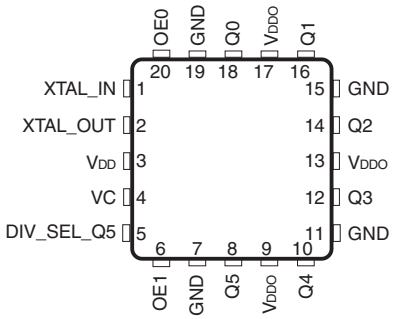
Features

- Six LVCMOS/LVTTL outputs, 20Ω nominal output impedance
- Output Q5 can be selected for ÷1 or ÷2 frequency relative to the crystal frequency
- Output frequency range: 12MHz to 31.25MHz
- Crystal pull range: ±90ppm (typical)
- Synchronous output enable places outputs in High-Impedance state
- On-chip filter on VIN to suppress noise modulation of VCXO
- V_{DD}/V_{DDO} combinations
  3.3V/3.3V
  3.3V/2.5V
  3.3V/1.8V
  2.5V/2.5V
  2.5V/1.8V
- 4mm x 4mm 20-Lead VFQFN package is ideal for space constrained designs
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

Block Diagram



Pin Assignment



ICS81006I

20-Lead VFQFN
4mm x 4mm x 0.925 package body
K Package

Top View

Pin Descriptions and Characteristics

Table 1. Pin Descriptions[1]

Number	Name	Type		Description
1, 2	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
3	V_{DD}	Power		Positive supply pin.
4	VC	Input		Control voltage input.
5	DIV_SEL_Q5	Input	Pulldown	Output divider select pin for Q5 output. When LOW, ÷1. When HIGH, ÷2. LVCMOS/LVTTL interface levels.
6	OE1	Input	Pullup	Output enable pin. When HIGH, Q5 output is enabled. When LOW, forces Q5 to a high impedance state. LVCMOS/LVTTL interface levels.
7, 11, 15, 19	GND	Power		Power supply ground.
8, 10, 12, 14, 16, 18	Q5, Q4, Q3, Q2, Q1, Q0	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels. 20Ω output impedance.
9, 13, 17	V_{DDO}	Power		Output supply pins.
20	OE0	Input	Pullup	Output enable pin. When HIGH, Q0:Q4 outputs are enabled. When LOW, forces Q0:Q4 to a high impedance state. LVCMOS/LVTTL interface levels.

NOTE 1: *Pullup* and *Pulldown* refers to internal input resistors. See *Table 2*, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	OE0, OE1			4		pF
C_{PD}	Power Dissipation Capacitance		$V_{DD} = V_{DDO} = 3.465V$			3	pF
			$V_{DD} = 3.465V$ or $2.625V$, $V_{DDO} = 2.625V$			4	pF
			$V_{DD} = 3.465V$ or $2.625V$, $V_{DDO} = 2V$			6	pF
R_{PULLUP}	Input Pullup Resistor				51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{OUT}	Output Impedance		$V_{DDO} = 3.3V$			20	Ω
			$V_{DDO} = 2.5V$			25	Ω
			$V_{DDO} = 1.8V$			38	Ω

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Electrical Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	60.4°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, V_{DD} = 3.3V±5%, V_{DDO} = 3.3V ±5%, 2.5V ±5% or 1.8V ±0.2V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
			1.6	1.8	2.0	V
I_{DD}	Power Supply Current				50	mA
I_{DDO}	Output Supply Current				20	mA

Table 3B. Power Supply DC Characteristics, V_{DD} = 2.5V±5%, V_{DDO} = 2.5V ±5% or 1.8V ±0.2V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
			1.6	1.8	2.0	V
I_{DD}	Power Supply Current				50	mA
I_{DDO}	Output Supply Current				20	mA

Table 3C. LVCMOS/LVTTL DC Characteristics, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V ±5%	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V ±5%	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	OE0, OE1, DIV_SEL_Q5	V_{DD} = 3.3V ±5%	-0.3		0.8	V
			V_{DD} = 2.5V ±5%	-0.3		0.7	V
VC	VCXO Control Voltage			0		V_{DD}	V
I_{IH}	Input High Current	DIV_SEL_Q5	V_{DD} = 3.3V or 2.5V ±5%			150	µA
		OE0, OE1	V_{DD} = 3.3V or 2.5V ±5%			5	µA
I_{IL}	Input Low Current	DIV_SEL_Q5	V_{DD} = 3.3V or 2.5V ±5%	-5			µA
		OE0, OE1	V_{DD} = 3.3V or 2.5V ±5%	-150			µA
I_I	Input Current of VC pin		V_{DD} = 3.465V or 2.625V	-100		100	µA
V_{OH}	Output High Voltage[1]		V_{DDO} = 3.3V ±5%	2.6			V
			V_{DDO} = 2.5V ±5%	1.8			V
			V_{DDO} = 1.8V ±0.2V	1.5			V
V_{OL}	Output Low Voltage[1]		V_{DDO} = 3.3V or 2.5V ±5%			0.5	V
			V_{DDO} = 1.8V ±0.2V			0.4	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See *Parameter Measurement Information* section, "Load Test Circuit" diagrams.

AC Characteristics

Table 4A. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			12	19.44	31.25	MHz
$t_{jit}(\emptyset)$	RMS Phase Jitter (Random)[1]		Integration Range: 1kHz – 1MHz		0.35		ps
tsk(o)	Output Skew[2, 3]	Q0:Q4				30	ps
		Q0:Q5	DIV_SEL_Q5 = ÷1			100	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	200		750	ps
odc	Output Duty Cycle			44		56	%

NOTE 1: Refer to the *Phase Noise Plot*.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential crosspoints.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

Table 4B. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			12	19.44	31.25	MHz
$t_{jit}(\emptyset)$	RMS Phase Jitter (Random)[1]		Integration Range: 1kHz – 1MHz		0.38		ps
tsk(o)	Output Skew[2, 3]	Q0:Q4				20	ps
		Q0:Q5	DIV_SEL_Q5 = ÷1			90	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	300		800	ps
odc	Output Duty Cycle			45		55	%

NOTE 1: Refer to the *Phase Noise Plot*.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential crosspoints.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

Table 4C. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			12	19.44	31.25	MHz
$t_{jit}(\emptyset)$	RMS Phase Jitter (Random)[1]		Integration Range: 1kHz – 1MHz		0.27		ps
tsk(o)	Output Skew[2, 3]	Q0:Q4				50	ps
		Q0:Q5	DIV_SEL_Q5 = ÷1			180	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	450		1400	ps
odc	Output Duty Cycle			45		55	%

NOTE 1: Refer to the *Phase Noise Plot*.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential crosspoints.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

Table 4D. AC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			12	19.44	31.25	MHz
$t_{jit}(\emptyset)$	RMS Phase Jitter (Random)[1]		Integration Range: 1kHz – 1MHz		0.28		ps
tsk(o)	Output Skew[2, 3]	Q0:Q4				25	ps
		Q0:Q5	DIV_SEL_Q5 = ÷1			105	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	300		800	ps
odc	Output Duty Cycle			45		55	%

NOTE 1: Refer to the *Phase Noise Plot*.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential crosspoints.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

Table 4E. AC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, T_A = -40°C to 85°C

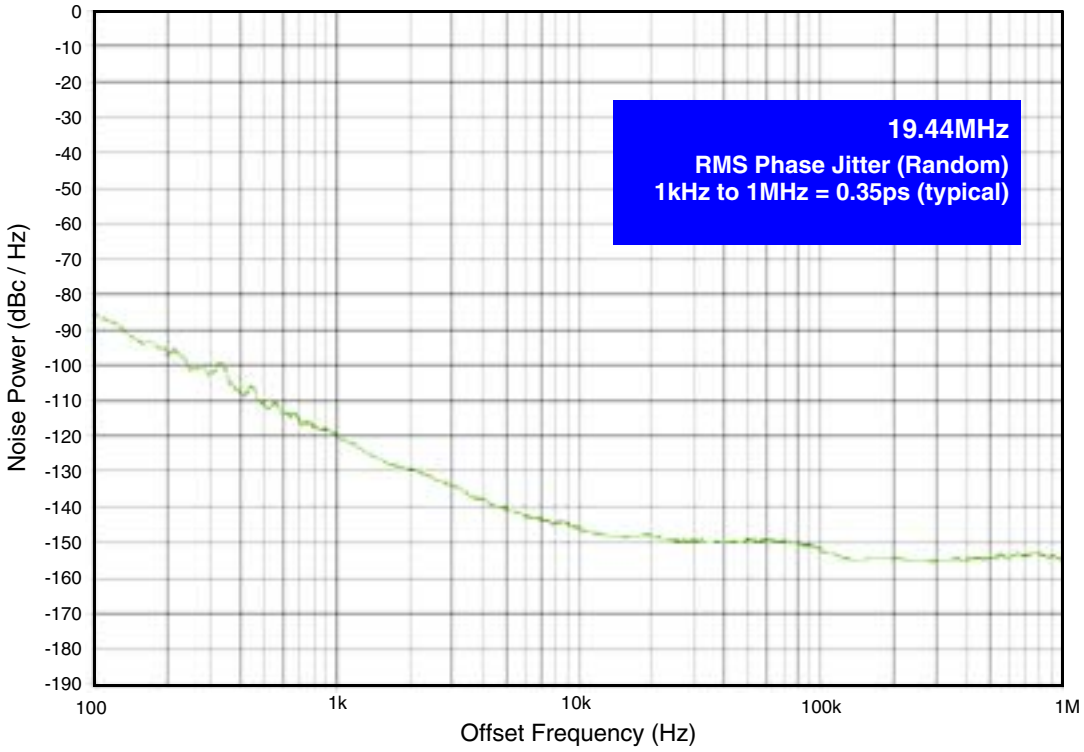
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			12	19.44	31.25	MHz
$t_{jit}(\emptyset)$	RMS Phase Jitter (Random)[1]		Integration Range: 1kHz – 1MHz		0.26		ps
tsk(o)	Output Skew[2, 3]	Q0:Q4				40	ps
		Q0:Q5	DIV_SEL_Q5 = ÷1			185	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	450		1400	ps
odc	Output Duty Cycle			40		60	%

NOTE 1: Refer to the *Phase Noise Plot*.

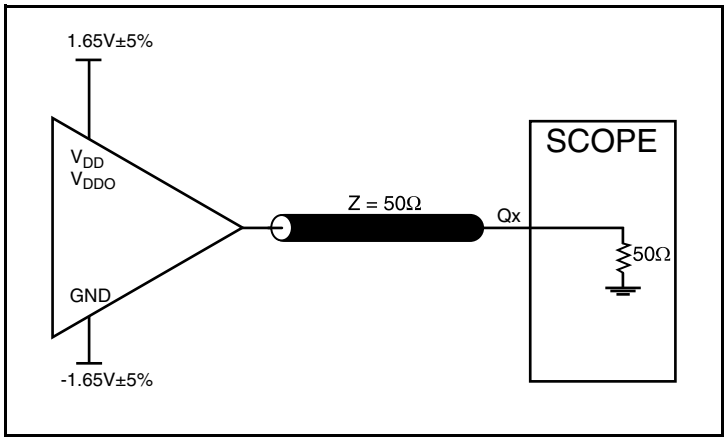
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential crosspoints.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

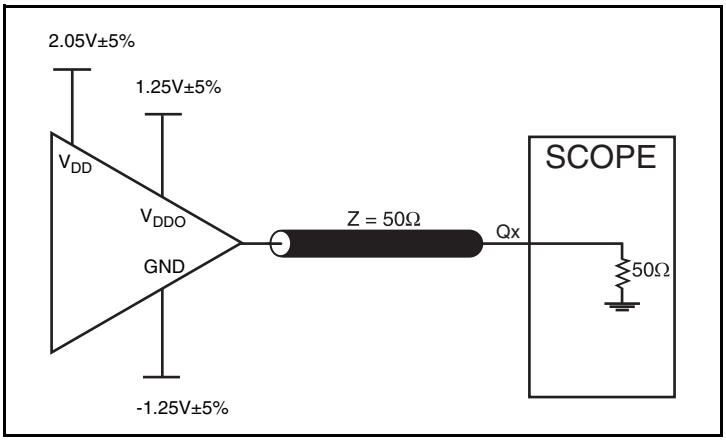
Typical Phase Noise at 19.44MHz @3.3V CORE/3.3V Output



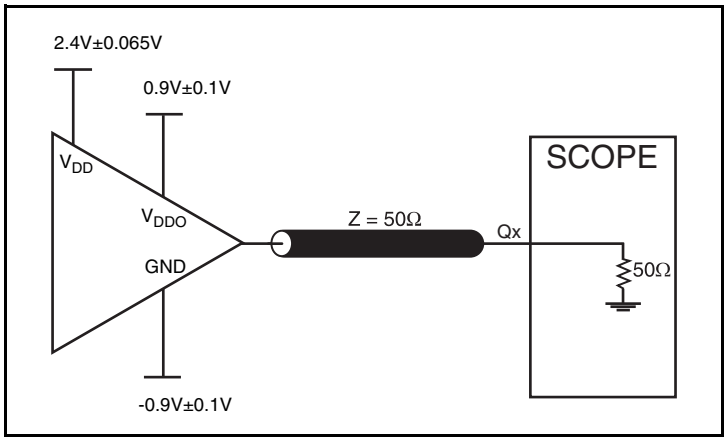
Parameter Measurement Information



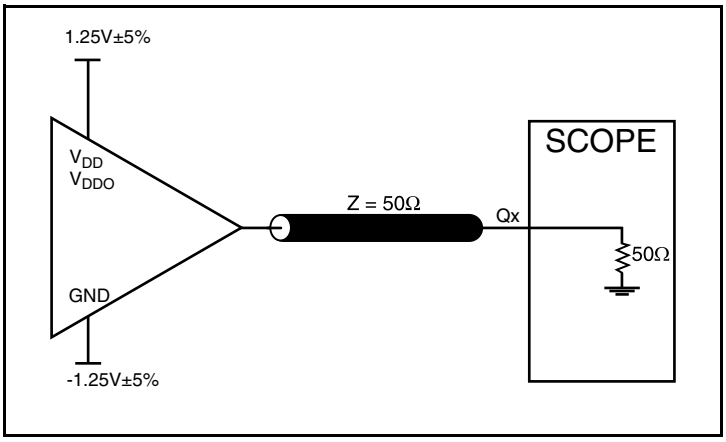
3.3V Core/3.3V Output Load Test Circuit



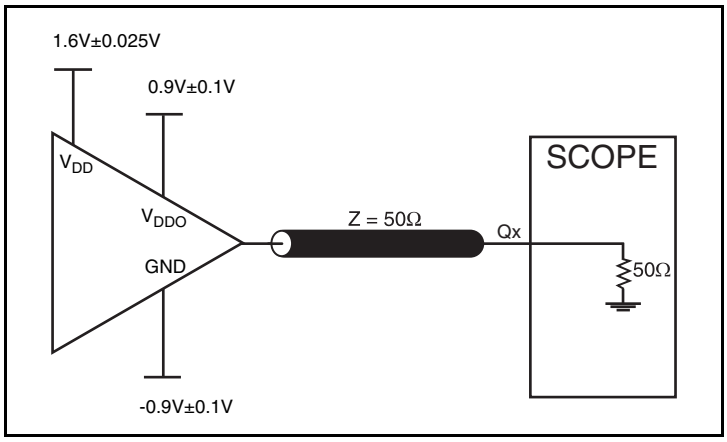
3.3V Core/2.5V Output Load Test Circuit



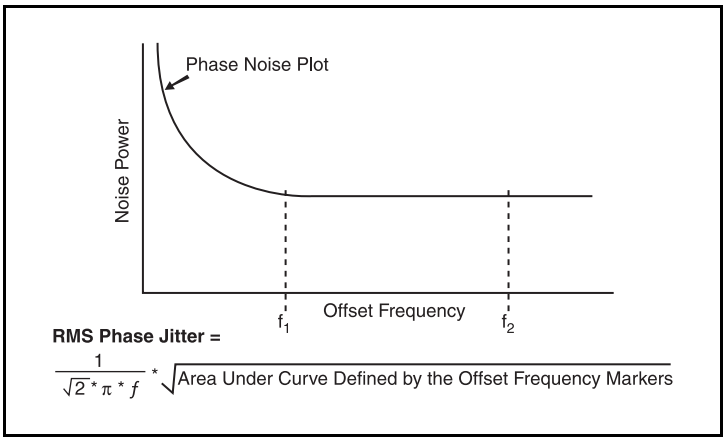
3.3V Core/1.8V Output Load Test Circuit



2.5V Core/2.5V Output Load Test Circuit

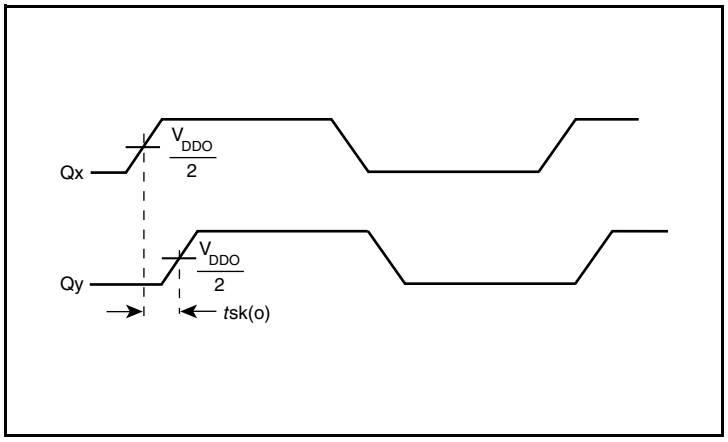


2.5V Core/1.8V Output Load Test Circuit

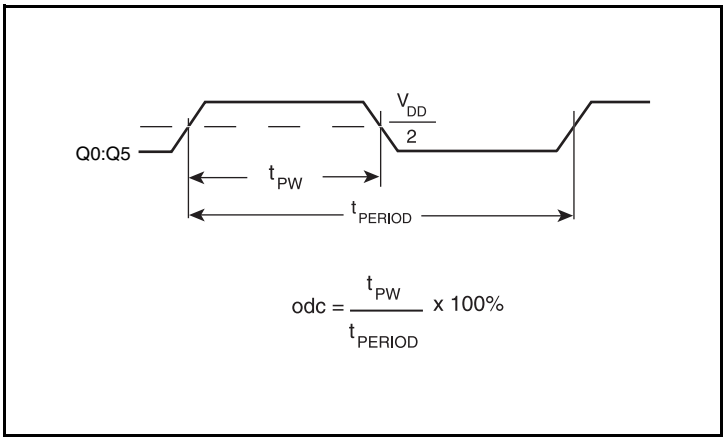


RMS Phase Jitter

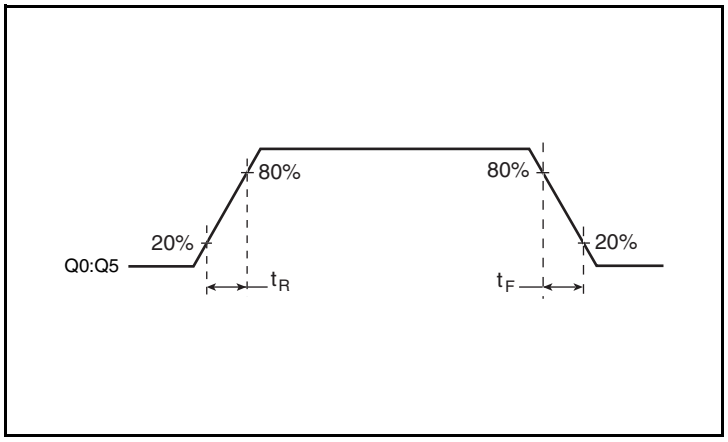
Parameter Measurement Information, Continued



Output Skew



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Applications Information

VCXO Crystal Selection

Choosing a crystal with the correct characteristics is one of the most critical steps in using a Voltage Controlled Crystal Oscillator (VCXO). The crystal parameters affect the tuning range and accuracy of a VCXO. Below are the key variables and an example of using the crystal parameters to calculate the tuning range of the VCXO.

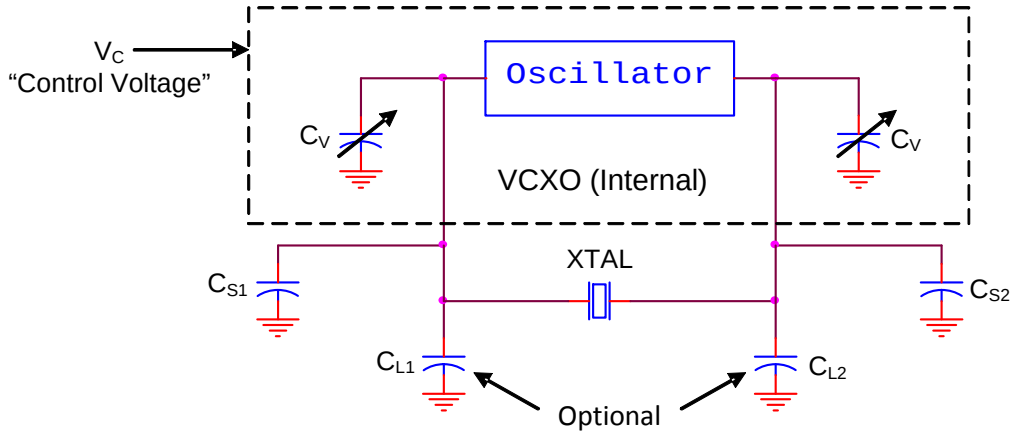


Figure 1. VCXO Oscillator Circuit

V_C -Control voltage used to tune frequency

C_V -Varactor capacitance, varies due to the change in control voltage

C_{L1}, C_{L2} -Load tuning capacitance used for fine tuning or centering nominal frequency

C_{S1}, C_{S2} -Stray Capacitance caused by pads, vias, and other board parasitics

Table 5. Example Crystal Parameters

Symbol	Parameter	Test Conditions	Min	Typical	Max	Units
f_N	Nominal Frequency			19.44		MHz
f_T	Frequency Tolerance				±20	ppm
f_S	Frequency Stability				±20	ppm
	Operating Temp Range		0		70	°C
C_L	Load Capacitance			12		pF
C_O	Shunt Capacitance			4		pF
C_O/C_1	Pullability Ratio			220	240	
ESR	Equivalent Series Resistance				20	
	Drive Level				1	mW
	Aging @ 25°C			±3 per year		ppm
	Mode of Operation			Fundamental		

Table 6. Varactor Parameters

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Unit
C_{V_LOW}	Low Varactor Capacitance	V_C = 0V		15.4		pF
C_{V_HIGH}	High Varactor Capacitance	V_C = 3.3V		29.6		pF

Formulas

$$C_{Low} = \frac{(C_{L1} + C_{S1} + C_{V\_Low}) \cdot (C_{L2} + C_{S2} + C_{V\_Low})}{(C_{L1} + C_{S1} + C_{V\_Low}) + (C_{L2} + C_{S2} + C_{V\_Low})}$$

$$C_{High} = \frac{(C_{L1} + C_{S1} + C_{V\_High}) \cdot (C_{L2} + C_{S2} + C_{V\_High})}{(C_{L1} + C_{S1} + C_{V\_High}) + (C_{L2} + C_{S2} + C_{V\_High})}$$

- C_{Low} is the effective capacitance due to the low varactor capacitance, load capacitance and stray capacitance. C_{Low} determines the high frequency component on the TPR.
- C_{High} is the effective capacitance due to the high varactor capacitance, load capacitance and stray capacitance. C_{High} determines the low frequency component on the TPR.

$$Total\ \ Pull\ \ Range\ (TPR) = \left(\frac{1}{2 \cdot C_0/C_1 \cdot \left(1 + C_{Low}/C_0\right)} - \frac{1}{2 \cdot C_0/C_1 \cdot \left(1 + C_{High}/C_0\right)} \right) \cdot 10^6$$

Absolute Pull Range (APR) = Total Pull Range – (Frequency Tolerance + Frequency Stability + Aging)

Example Calculations

Using the tables and figures above, we can now calculate the TPR and APR of the VCXO using the example crystal parameters. For the numerical example below there were some assumptions made. First, the stray capacitance (C_{S1}, C_{S2}), which is all the excess capacitance due to board parasitic, is 4pF. Second, the expected lifetime of the project is 5 years; hence the inaccuracy due to aging is ±15ppm.

Third, though many boards will not require load tuning capacitors (C_{L1}, C_{L2}), it is recommended for long-term consistent performance of the system that two tuning capacitor pads be placed into every design. Typical values for the load tuning capacitors will range from 0 to 4 pF.

$$C_{Low} = \frac{(0 + 4pf + 15.4pf) \cdot (0 + 4pf + 15.4pf)}{(0 + 4pf + 15.4pf) + (0 + 4pf + 15.4pf)} = 9.7\,pf$$

$$C_{High} = \frac{(0 + 4pf + 29.6pf) \cdot (0 + 4pf + 29.6pf)}{(0 + 4pf + 29.6pf) + (0 + 4pf + 29.6pf)} = 16.8\,pf$$

$$TPR = \left(\frac{1}{2 \cdot 220 \cdot \left(1 + 9.7pF/4pF\right)} - \frac{1}{2 \cdot 220 \cdot \left(1 + 16.8pF/4pF\right)} \right) \cdot 10^6 \cdot = 226.5\,ppm$$

TPR = ±113.25ppm

APR = 113.25ppm – (20ppm + 20ppm + 15ppm) = ±58.25ppm

The example above will ensure a total pull range of ±113.25 ppm with an APR of ±58.25ppm. Many times, board designers may select their own crystal based on their application. If the application requires a tighter APR, a crystal with better pullability (C0/C1 ratio) can be used.

Also, with the equations above, one can vary the frequency tolerance, temperature stability, and aging or shunt capacitance to achieve the required pullability.

Recommendations for Unused Input Pins

Inputs:

Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used. The VC pin can not be floated.

Outputs:

LVCMOS Outputs

All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

Schematic Example

Figure 2 shows an example of ICS81006I application schematic. The decoupling capacitors should be located as close as possible to the power pin. For the LVCMOS 20Ω output drivers, series termination example is shown in the schematic. Additional termination approaches are shown in the LVCMOS Termination Application Note.

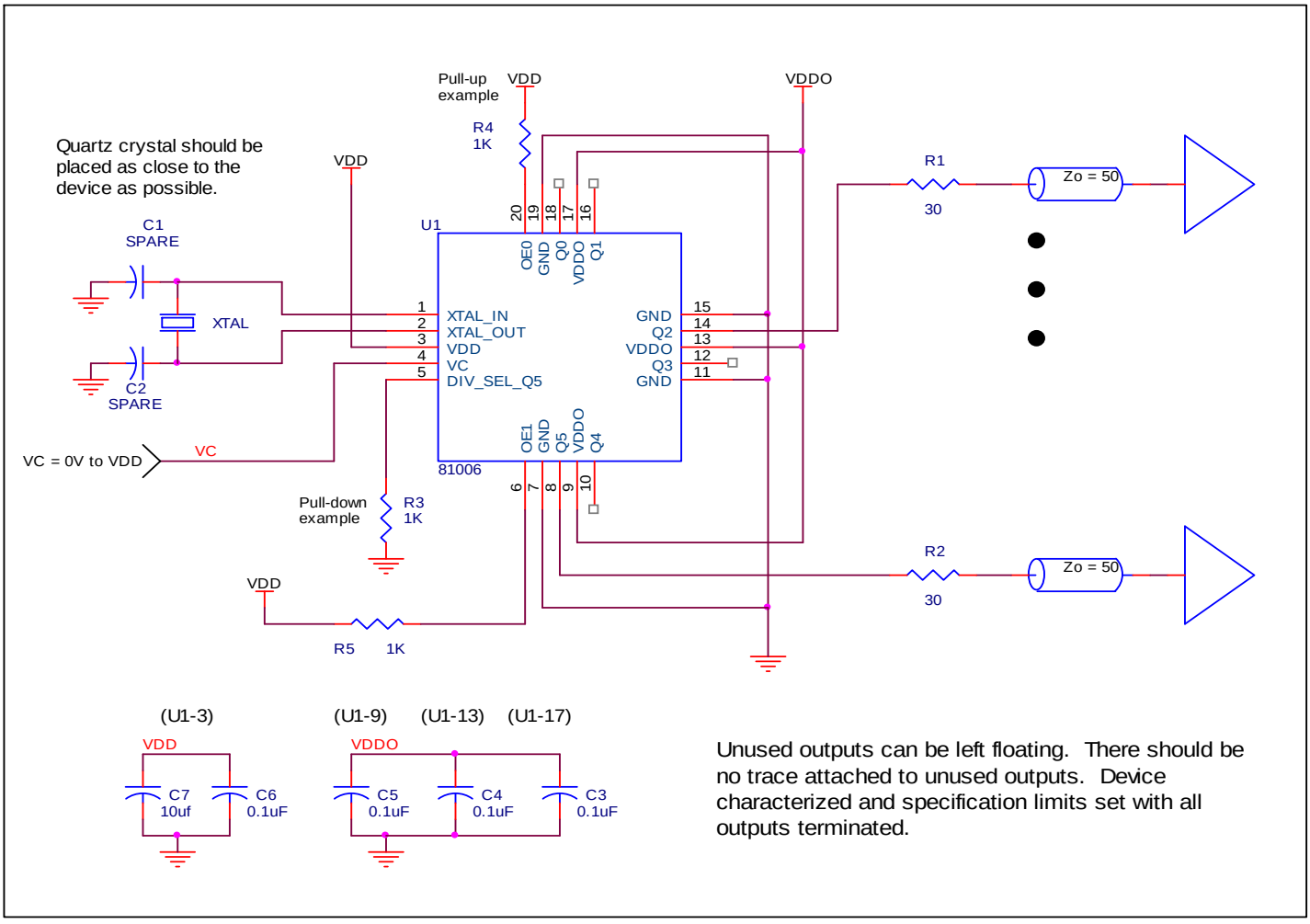


Figure 2. ICS81006I Schematic Example

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

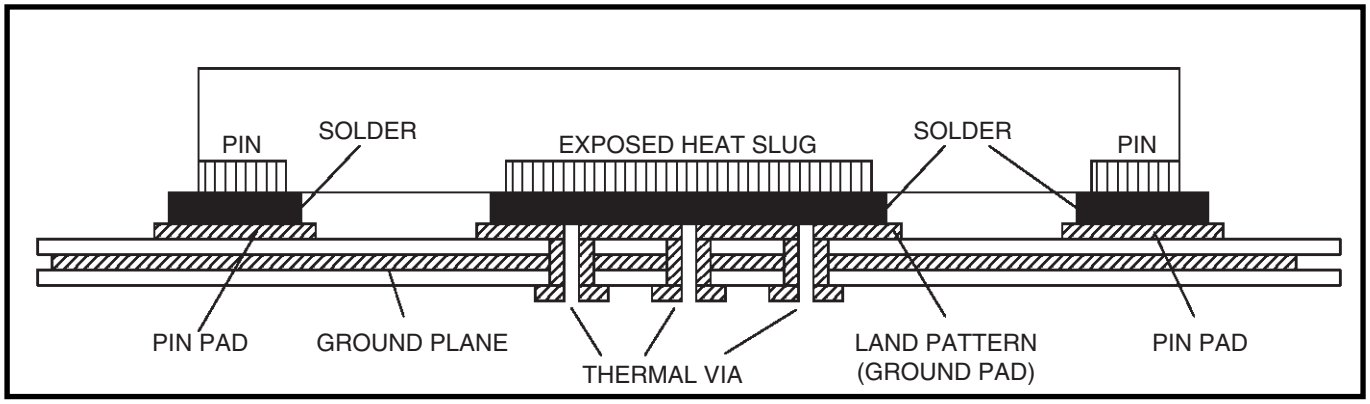


Figure 3. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 20-Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**3**
Multi-Layer PCB, JEDEC Standard Test Boards	60.4°C/W	52.8°C/W	46.0°C/W

Transistor Count

The transistor count for the ICS81006I is: 983

Package Outline and Package Dimensions

Package Outline - K Suffix for 20-Lead VFQFN

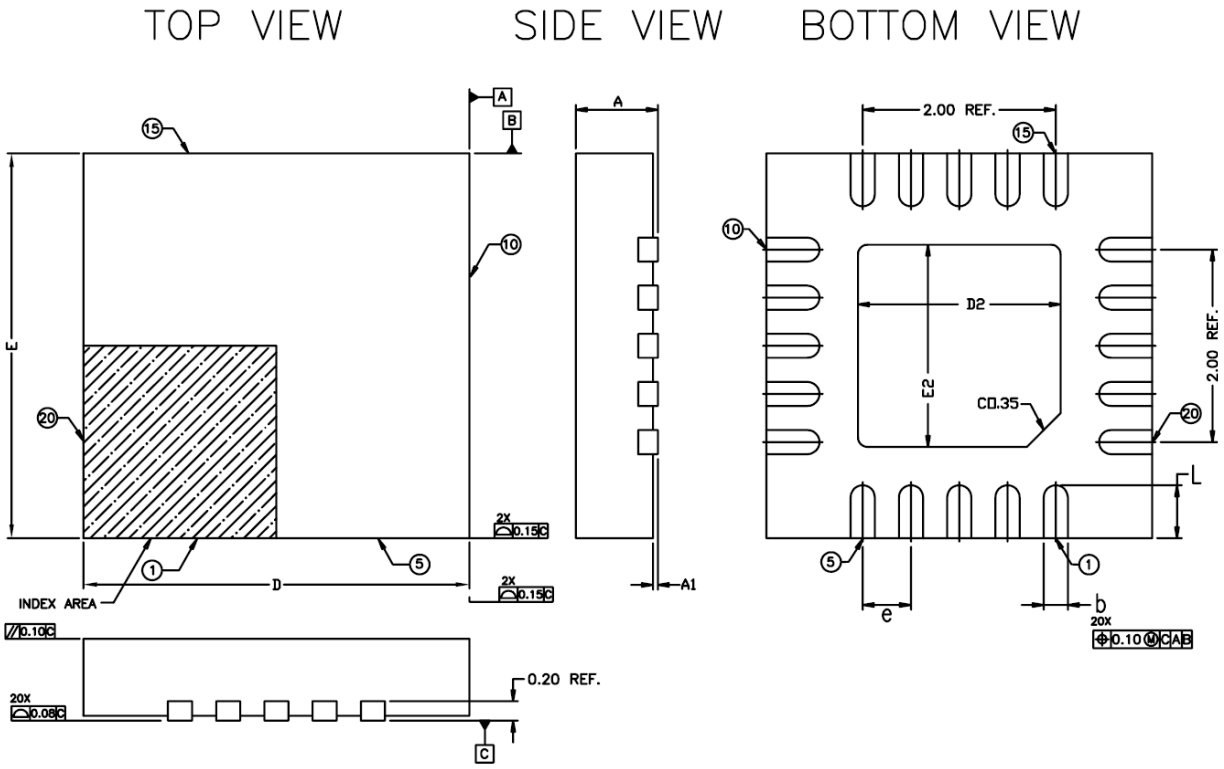


Table 8. Package Dimensions for 20-Lead VFQFN

All Dimensions in Millimeters			
Symbol	**Minimum**	**Nom**	**Maximum**
b	0.20	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	1.95	2.10	2.25
E2	1.95	2.10	2.25
L	0.45	0.55	0.65
e	0.50 BSC		
N	20		
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	0.2 REF		

Reference Document: JEDEC Publication 95, MO-220

NOTE:

The drawing and dimension data originate from IDT package outline drawing PSC-4170, rev03.

1. Dimensions and tolerances conform to ASME Y14.5M-1994
2. All dimensions are in millimeters. All angles are in degrees.
3. N is the total number of terminals.
4. All specifications comply with JEDEC MO-220.

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
81006AKILF	006AIL	“Lead-Free” 20-Lead VFQFN	Tube	-40°C to 85°C
81006AKILFT	006AIL	“Lead-Free” 20-Lead VFQFN	Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T4A - T4D T9	1 4-5 6 15	General Description and Features section changed output frequency max. from 40MHz to 31.25MHz. AC Tables - changed output frequency from 40MHz max. to 31.25MHz max. Added Phase Noise Plot. Ordering Information Table - added lead-free marking	10/8/08
B	 T8 T9	 15 15 1, 16	Updated datasheet to current format. Updated Package Outline Updated package dimensions to reflect tighter tolerances. Removed leaded ordering option.	7/25/14
B		1	PDN CQ-15-01	2/10/15
B			Added OBSOLETE to the front page.	7/29/16

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