

FEATURES:

- 2.3V to 2.7V Operation
- SSTL\_2 Class I style data inputs/outputs
- Differential CLK input
- $\overline{\text{RESET}}$  control compatible with LVC MOS levels
- Flow-through architecture for optimum PCB design
- Drive up to equivalent of 14 SDRAM loads
- Latch-up performance exceeds 100mA
- ESD >2000V per MIL-STD-883, Method 3015; >200V using machine model (C = 200pF, R = 0)
- Available in TSSOP package

APPLICATIONS:

- Along with CSPT857C, Zero Delay PLL Clock buffer, provides complete solution for DDR1 DIMMs

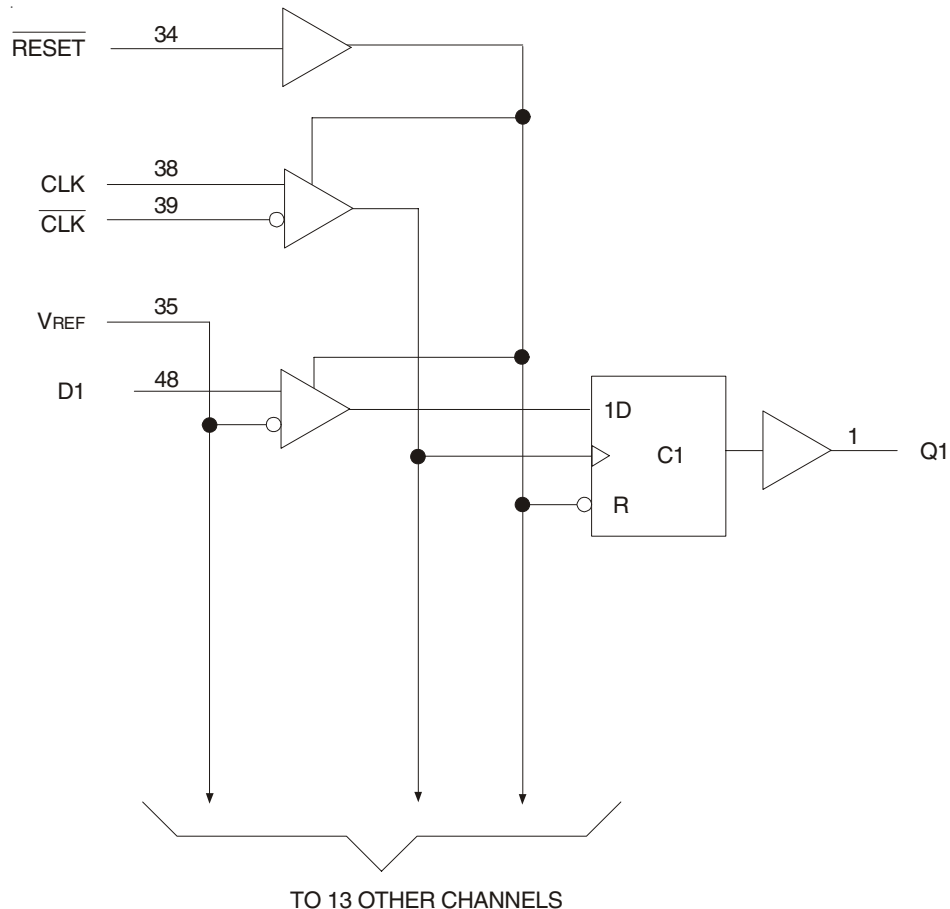
DESCRIPTION:

The SSTVF16857 is a 14-bit registered buffer designed for 2.3V-2.7V  $V_{DD}$  and supports low standby operation. All data inputs and outputs are SSTL\_2 level compatible with JEDEC standard for SSTL\_2.

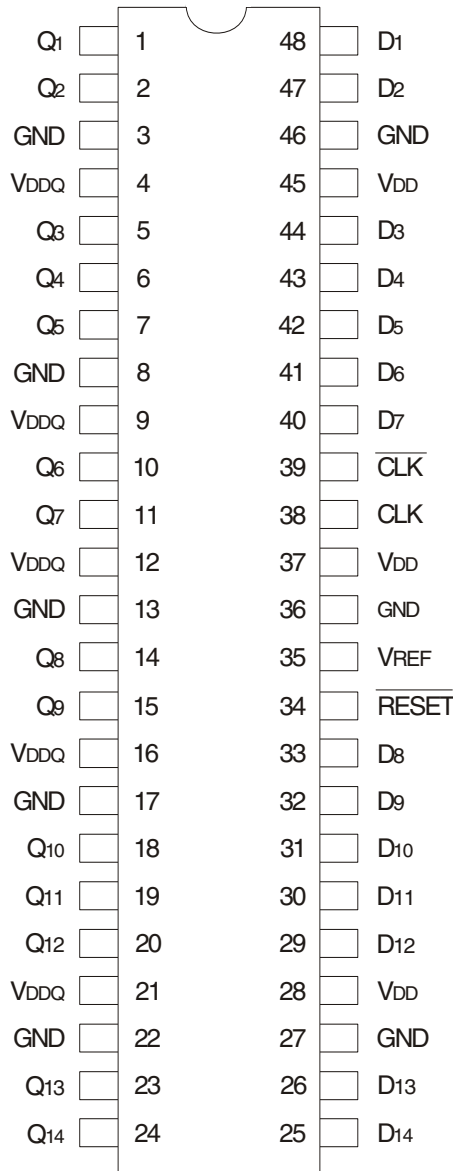
$\overline{\text{RESET}}$  is an LVC MOS input since it must operate predictably during the power-up phase.  $\overline{\text{RESET}}$ , which can be operated independent of CLK and  $\overline{\text{CLK}}$ , must be held in the low state during power-up in order to ensure predictable outputs (low state) before a stable clock has been applied.

$\overline{\text{RESET}}$ , when in the low state, will disable all input receivers, reset all registers, and force all outputs to a low state, before a stable clock has been applied. With inputs held low and a stable clock applied, outputs will remain low during the Low-to-High transition of  $\overline{\text{RESET}}$ .

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TSSOP  
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

| Symbol                        | Description   | Max.               | Unit |
|-------------------------------|---|--------------------|------|
| VDD or VDDQ                   | Supply Voltage Range  | -0.5 to 3.6        | V    |
| V <sub>I</sub> <sup>(2)</sup> | Input Voltage Range   | -0.5 to VDD + 0.5  | V    |
| V <sub>O</sub> <sup>(3)</sup> | Output Voltage Range  | -0.5 to VDDQ + 0.5 | V    |
| I <sub>IK</sub>               | Input Clamp Current, V <sub>I</sub> < 0                           | -50                | mA   |
| I <sub>OK</sub>               | Output Clamp Current, V <sub>O</sub> < 0 or V <sub>O</sub> > VDDQ | ±50                | mA   |
| I <sub>O</sub>                | Continuous Output Current, V <sub>O</sub> = 0 to VDDQ             | ±50                | mA   |
| VDD                           | Continuous Current through each VDD, VDDQ or GND                  | ±100               | mA   |
| T <sub>STG</sub>              | Storage Temperature Range   | -65 to +150        | °C   |

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- The input and output negative voltage ratings may be exceeded if the ratings of the I/P and O/P clamp current are observed.
- The output current will flow if the following conditions are observed:
  - Output in HIGH state
  - V<sub>O</sub> = VDDQ

FUNCTION TABLE (1)

| Input |        |        |   | Q Outputs                     |
|-------|--------|--------|---|-------------------------------|
| RESET | CLK    | CLK    | D |                               |
| H     | ↑      | ↓      | L | L                             |
| H     | ↑      | ↓      | H | H                             |
| H     | L or H | L or H | X | Q <sub>0</sub> <sup>(2)</sup> |
| L     | X      | X      | X | L                             |

NOTES:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
↑ = LOW to HIGH  
↓ = HIGH to LOW
- Q<sub>0</sub> = Output level before the indicated steady-state conditions were established.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{DD} = 2.5\text{V} \pm 0.2\text{V}$ ,  $V_{DDQ} = 2.5\text{V} \pm 0.2\text{V}$

| Symbol   | Parameter                               | Test Conditions   | Min.           | Typ. | Max.    | Unit                              |
|----------|---|---|----------------|------|---------|-----------------------------------|
| $V_{IK}$ | Control Inputs                          | $V_{DD} = 2.3\text{V}$ , $I_I = -18\text{mA}$   | —              | —    | -1.2    | V                                 |
| $V_{OH}$ |   | $V_{DD} = 2.3\text{V}$ to $2.7\text{V}$ , $I_{OH} = -100\mu\text{A}$  | $V_{DD} - 0.2$ | —    | —       | V                                 |
|          |   | $V_{DD} = 2.3\text{V}$ , $I_{OH} = -8\text{mA}$   | 1.95           | —    | —       |                                   |
| $V_{OL}$ |   | $V_{DD} = 2.3\text{V}$ to $2.7\text{V}$ , $I_{OL} = 100\mu\text{A}$   | —              | —    | 0.2     | V                                 |
|          |   | $V_{DD} = 2.3\text{V}$ , $I_{OL} = 8\text{mA}$  | —              | —    | 0.35    |                                   |
| $I_I$    | All Inputs                              | $V_{DD} = 2.7\text{V}$ , $V_I = V_{DD}$ or GND  | —              | —    | $\pm 5$ | $\mu\text{A}$                     |
| $I_{DD}$ | Static Standby                          | $I_O = 0$ , $V_{DD} = 2.7\text{V}$ , $\overline{\text{RESET}} = \text{GND}$   | —              | —    | 0.01    | mA                                |
|          | Static Operating                        | $I_O = 0$ , $V_{DD} = 2.7\text{V}$ , $\overline{\text{RESET}} = V_{DD}$ , $V_I = V_{IH}$ (AC) or $V_{IL}$ (AC)  | —              | 6    | —       |                                   |
| $I_{DD}$ | Dynamic Operating (Clock Only)          | $I_O = 0$ , $V_{DD} = 2.7\text{V}$ , $\overline{\text{RESET}} = V_{DD}$ , $V_I = V_{IH}$ (AC) or $V_{IL}$ (AC), CLK and $\overline{\text{CLK}}$ Switching 50% Duty Cycle.   | —              | —    | —       | $\mu\text{A}/\text{Clock}$<br>MHz |
|          | Dynamic Operating (Per Each Data Input) | $I_O = 0$ , $V_{DD} = 2.7\text{V}$ , $\overline{\text{RESET}} = V_{DD}$ , $V_I = V_{IH}$ (AC) or $V_{IL}$ (AC), CLK and $\overline{\text{CLK}}$ Switching 50% Duty Cycle. One Data Input Switching at Half Clock Frequency, 50% Duty Cycle. | —              | —    | —       |                                   |
| $C_I$    | Data Inputs                             | $V_{DD} = 2.5\text{V}$ , $V_I = V_{REF} \pm 310\text{mV}$   | 2.5            | —    | 3.5     | pF                                |
|          | CLK and $\overline{\text{CLK}}$         | $V_{ICR} = 1.25\text{V}$ , $V_I(\text{PP}) = 360\text{mV}$  | 2.5            | —    | 3.5     |                                   |
|          | $\overline{\text{RESET}}$               | $V_I = V_{DD}$ or GND   | —              | —    | —       |                                   |

## OPERATING CHARACTERISTICS, $T_A = 25^\circ\text{C}$ (1)

| Symbol           | Parameter                                   | Min.                         | Typ. <sup>(1)</sup>      | Max.                     | Unit             |    |
|------------------|---|------------------------------|--------------------------|--------------------------|------------------|----|
| $V_{DD}$         | Supply Voltage                              | $V_{DDQ}$                    | —                        | 2.7                      | V                |    |
| $V_{DDQ}$        | Output Supply Voltage                       | 2.3                          | 2.5                      | 2.7                      | V                |    |
| $V_{REF}$        | Reference Voltage ( $V_{REF} = V_{DDQ}/2$ ) | 1.15                         | 1.25                     | 1.35                     | V                |    |
| $V_{TT}$         | Termination Voltage                         | $V_{REF} - 40\text{mV}$      | $V_{REF}$                | $V_{REF} + 40\text{mV}$  | V                |    |
| $V_I$            | Input Voltage                               | 0                            | —                        | $V_{DD}$                 | V                |    |
| $V_{IH}$         | AC High-Level Input Voltage                 | Data Inputs                  | $V_{REF} + 310\text{mV}$ | —                        | V                |    |
| $V_{IL}$         | AC Low-Level Input Voltage                  | Data Inputs                  | —                        | $V_{REF} - 310\text{mV}$ | V                |    |
| $V_{IH}$         | DC High-Level Input Voltage                 | Data Inputs                  | $V_{REF} + 150\text{mV}$ | —                        | V                |    |
| $V_{IL}$         | DC Low-Level Input Voltage                  | Data Inputs                  | —                        | $V_{REF} - 150\text{mV}$ | V                |    |
| $V_{IH}$         | High-Level Input Voltage                    | $\overline{\text{RESET}}$    | 1.7                      | —                        | V                |    |
| $V_{IL}$         | Low-Level Input Voltage                     | $\overline{\text{RESET}}$    | —                        | 0.7                      | V                |    |
| $V_{ICR}$        | Common-Mode Input Range                     | CLK, $\overline{\text{CLK}}$ | 0.97                     | —                        | 1.53             | V  |
| $V_I(\text{PP})$ | Peak-to-Peak Input Voltage                  | CLK, $\overline{\text{CLK}}$ | 360                      | —                        | —                | mV |
| $I_{OH}$         | High-Level Output Current                   |                              | —                        | —                        | -20              | mA |
| $I_{OL}$         | Low-Level Output Current                    |                              | —                        | —                        | 20               |    |
| $T_A$            | Operating Free-Air Temperature              | 0                            | —                        | +70                      | $^\circ\text{C}$ |    |

NOTE:

- The  $\overline{\text{RESET}}$  input of the device must be held at  $V_{DD}$  or GND to ensure proper device operation.

## TIMING REQUIREMENTS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE

| Symbol             | Parameter  | V <sub>DD</sub> = 2.5V ± 0.2V |      | Unit |    |
|--------------------|--|-------------------------------|------|------|----|
|                    |  | Min.                          | Max. |      |    |
| CLOCK              | Clock Frequency  | —                             | 200  | MHz  |    |
| t <sub>w</sub>     | Pulse Duration, CLK, $\overline{\text{CLK}}$ HIGH or LOW | 2.5                           | —    | ns   |    |
| t <sub>ACT</sub>   | Differential Inputs Active Time <sup>(1)</sup>           | —                             | 22   | ns   |    |
| t <sub>INACT</sub> | Differential Inputs Inactive Time <sup>(2)</sup>         | —                             | 22   | ns   |    |
| t <sub>SU</sub>    | Setup Time, Fast Slew Rate <sup>(3,5)</sup>              | Data Before CLK↑, CLK↓        | 0.75 | —    | ns |
|                    | Setup Time, Slow Slew Rate <sup>(4,5)</sup>              |                               | 0.9  | —    | ns |
| t <sub>H</sub>     | Hold Time, Fast Slew Rate <sup>(3,5)</sup>               | Data Before CLK↑, CLK↓        | 0.75 | —    | ns |
|                    | Hold Time, Slow Slew Rate <sup>(2,5)</sup>               |                               | 0.9  | —    | ns |

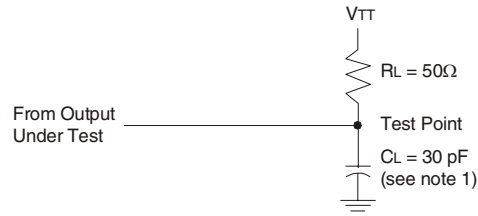
NOTES:

1. Data inputs must be low a minimum time of t<sub>ACT</sub> max., after  $\overline{\text{RESET}}$  is taken HIGH.
2. Data and clock inputs must be held at valid levels (not floating) a minimum time of t<sub>INACT</sub> max., after  $\overline{\text{RESET}}$  is taken LOW.
3. For data signal input slew rate is ≥1V/ns.
4. For data signal input slew rate is ≥0.5V/ns and <1V/ns.
5. CLK,  $\overline{\text{CLK}}$  signal input slew rates are ≥1V/ns.

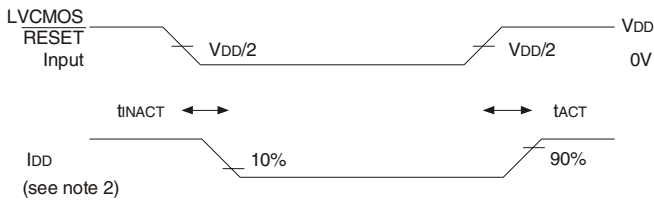
## SWITCHING CHARACTERISTICS OVER RECOMMENDED FREE-AIR OPERATING RANGE (UNLESS OTHERWISE NOTED)

| Symbol           | Parameter                            | V <sub>DD</sub> = 2.5V ± 0.2V |      | Unit |
|------------------|--------------------------------------|-------------------------------|------|------|
|                  |                                      | Min                           | Max. |      |
| f <sub>MAX</sub> |                                      | 200                           | —    | MHz  |
| t <sub>PD</sub>  | CLK and $\overline{\text{CLK}}$ to Q | 1.1                           | 2.8  | ns   |
| t <sub>PHL</sub> | $\overline{\text{RESET}}$ to Q       | —                             | 5    | ns   |

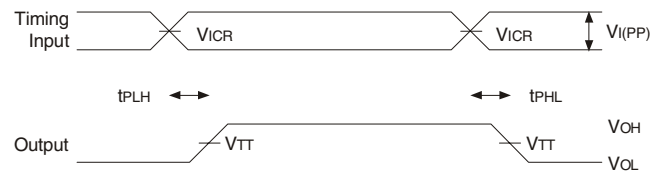
TEST CIRCUITS AND WAVEFORMS ( $V_{DD} = 2.5V \pm 0.2V$ )



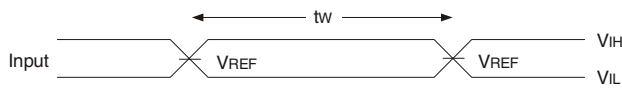
Load Circuit



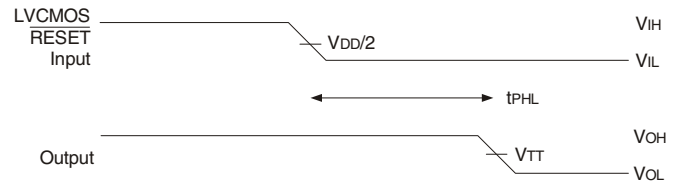
Voltage and Current Waveforms  
Inputs Active and Inactive Times



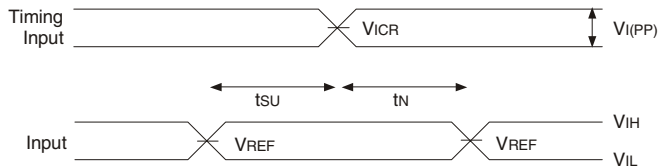
Voltage Waveforms - Propagation Delay Times



Voltage Waveforms - Pulse Duration



Voltage Waveforms - Propagation Delay Times

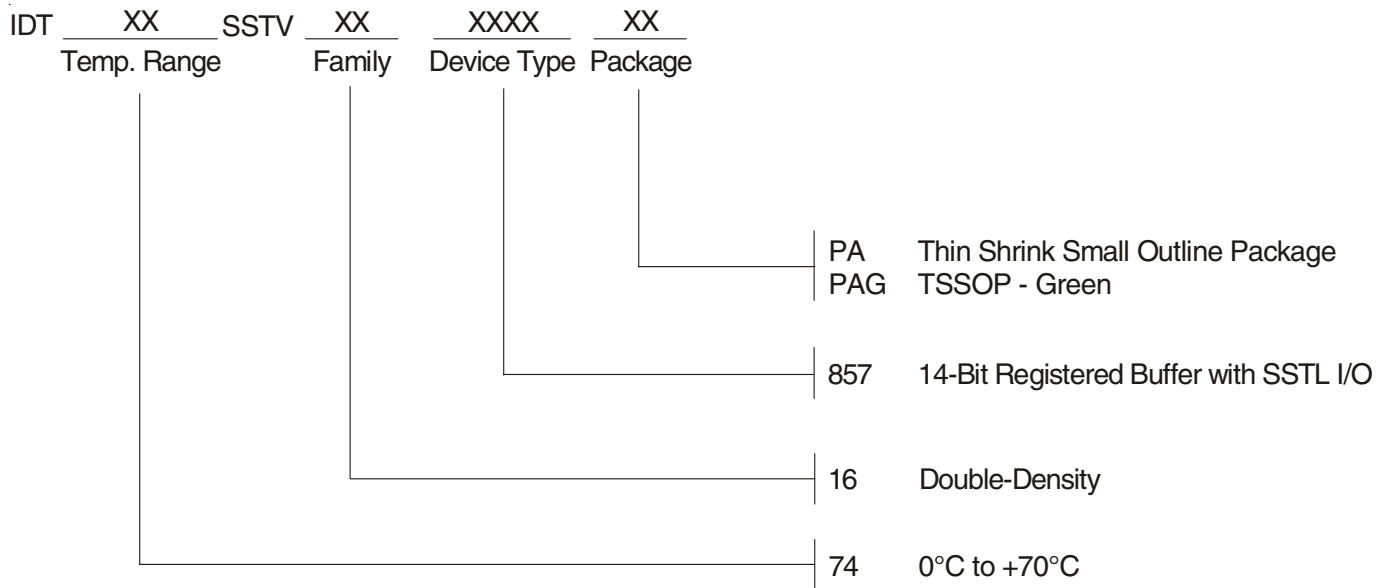


Voltage Waveforms - Setup and Hold Times

NOTES:

1.  $C_L$  includes probe and jig capacitance.
2.  $I_{DD}$  tested with clock and data inputs held at  $V_{DD}$  or GND, and  $I_o = 0\text{ mA}$ .
3. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_o = 50\Omega$ , input slew rate =  $1\text{ V/ns} \pm 20\%$  (unless otherwise specified).
4. The outputs are measured one at a time with one transition per measurement.
5.  $V_{TT} = V_{REF} = V_{DD}/2$
6.  $V_{IH} = V_{REF} + 310\text{ mV}$  (AC voltage levels) for differential inputs.  $V_{IH} = V_{DD}$  for LVC MOS input.
7.  $V_{IL} = V_{REF} - 310\text{ mV}$  (AC voltage levels) for differential inputs.  $V_{IL} = \text{GND}$  for LVC MOS input.
8.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{PD}$ .

## ORDERING INFORMATION



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### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

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