13-BIT TO 26-BIT REGISTERED BUFFER WITH SSTL I/O

IDT74SSTV16859

FEATURES:

- 2.3V to 2.7V Operation
- SSTL_2 Class II style data inputs/outputs
- Differential CLK input
- $\overline{\text{RESET}}$ control compatible with LVCMOS levels
- Latch-up performance exceeds 100mA
- ESD >2000V per MIL-STD-883, Method 3015; >200V using machine model (C = 200pF, R = 0)
- Available in 56 pin VFQFPN and 64 pin TSSOP packages

APPLICATIONS:

- Ideally suited for DIMM DDR registered applications

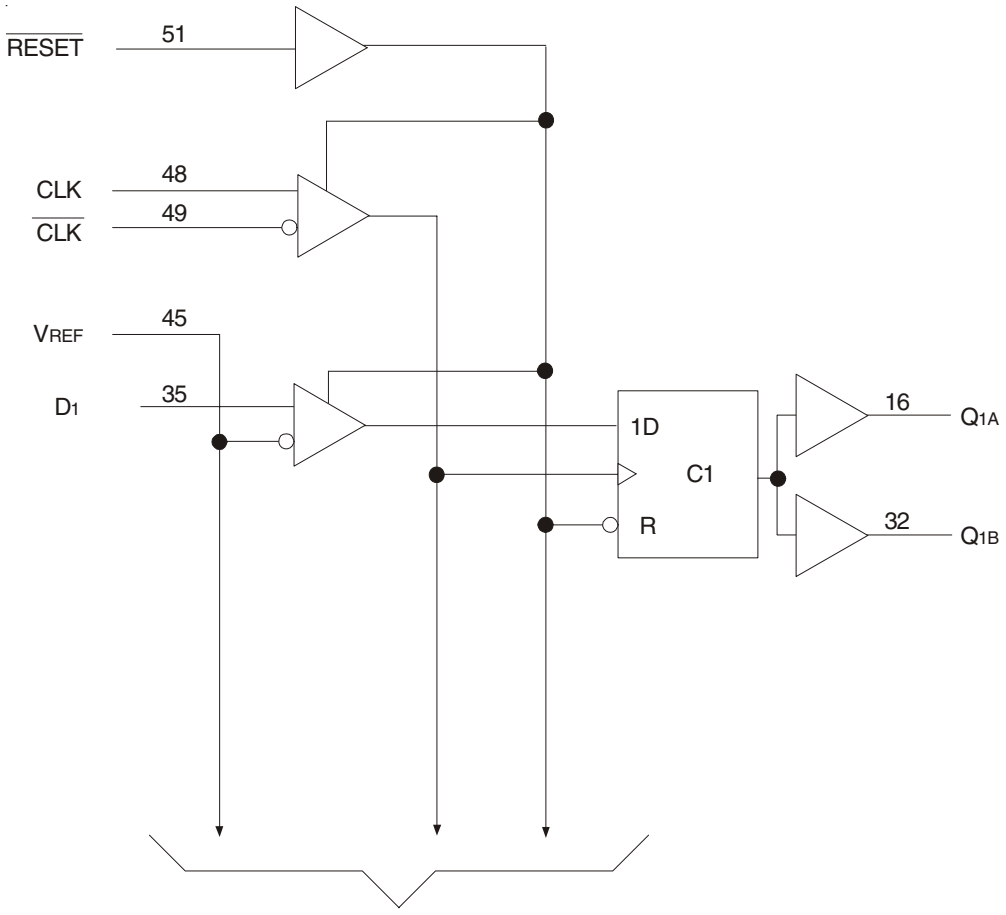
DESCRIPTION:

The SSTV16859 is a 13-bit to 26-bit registered buffer designed for 2.3V-2.7V V_{DD} and supports low standby operation. All data inputs and outputs are SSTL_2 level compatible with JEDEC standard for SSTL_2.

$\overline{\text{RESET}}$ is an LVCMOS input since it must operate predictably during the power-up phase. $\overline{\text{RESET}}$, which can be operated independent of CLK and $\overline{\text{CLK}}$, must be held in the low state during power-up in order to ensure predictable outputs (low state) before a stable clock has been applied.

$\overline{\text{RESET}}$, when in the low state, will disable all input receivers, reset all registers, and force all outputs to a low state, before a stable clock has been applied. With inputs held low and a stable clock applied, outputs will remain low during the Low-to-High transition of $\overline{\text{RESET}}$.

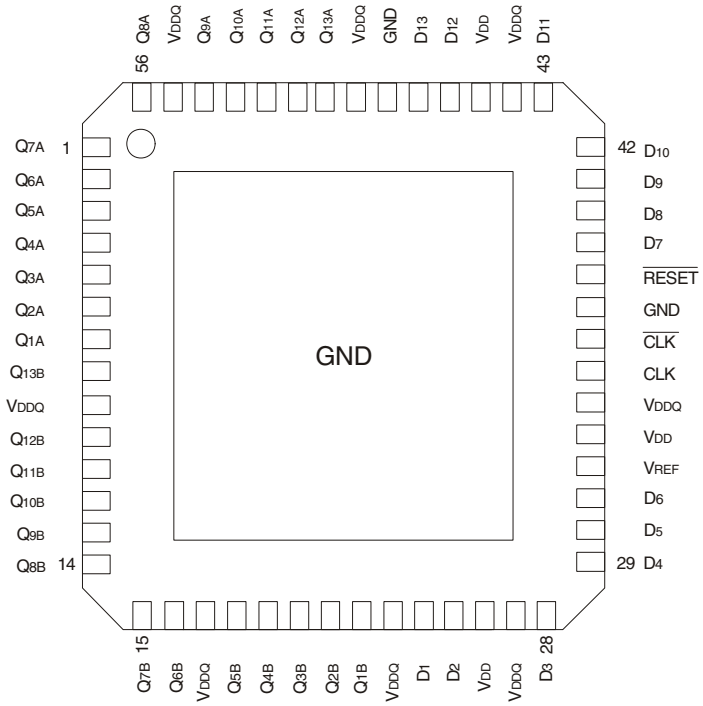
FUNCTIONAL BLOCK DIAGRAM



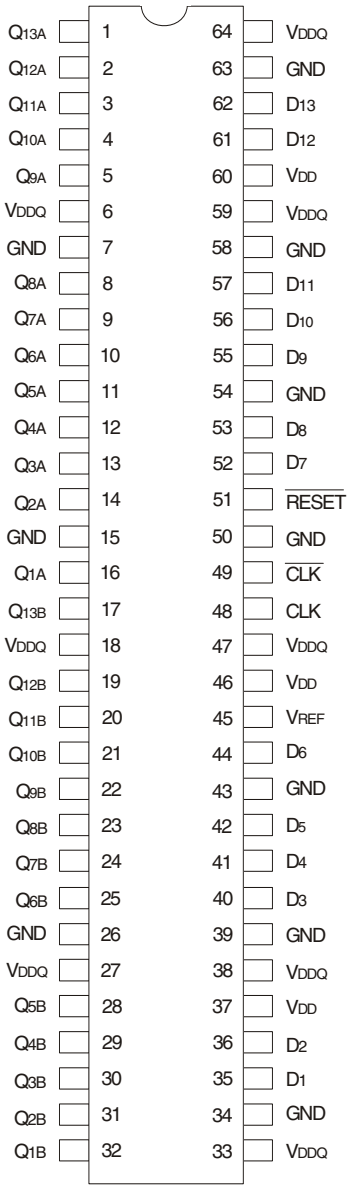
The IDT logo is a registered trademark of Integrated Device Technology, Inc.

© 2019 Renesas Electronics Corporation

PIN CONFIGURATIONS



VFQFPN
TOP VIEW



TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
V_{DD} or V_{DDQ}	Supply Voltage Range	–0.5 to 3.6	V
V_I (2)	Input Voltage Range	–0.5 to V_{DD} +0.5	V
V_O (3)	Output Voltage Range	–0.5 to V_{DDQ} +0.5	V
I_{IK}	Input Clamp Current, V_I < 0	–50	mA
I_{OK}	Output Clamp Current, V_O < 0 or V_O > V_{DDQ}	±50	mA
I_O	Continuous Output Current, V_O = 0 to V_{DDQ}	±50	mA
V_{DD}	Continuous Current through each V_{DD}, V_{DDQ} or GND	±100	mA
T_{STG}	Storage Temperature Range	–65 to +150	°C

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The input and output negative voltage ratings may be exceeded if the ratings of the I/P and O/P clamp current are observed.
3. The output current will flow if the following conditions are observed:
   a) Output in HIGH state
   b) V_O = V_{DDQ}

FUNCTION TABLE (1)

Input				Q Outputs
$\overline{\text{RESET}}$	CLK	$\overline{\text{CLK}}$	D	
H	↑	↓	L	L
H	↑	↓	H	H
H	L or H	L or H	X	Q_0 (2)
L	X	X	X	L

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW to HIGH
   ↓ = HIGH to LOW
2. Q_0 = Output level before the indicated steady-state conditions were established.

© 2019 Renesas Electronics Corporation

PIN DESCRIPTION

Pin Names	Description
Q_1 - Q_{13}	Data Output
GND	Ground
V_{DDQ}	Output-stage drain power voltage
V_{DD}	Logic power voltage
$\overline{RESET}$	Asynchronous reset input - resets registers and disables data and clock differential input recievers
V_{REF}	Input reference voltage
CLK	Positive master clock input
$\overline{CLK}$	Negative master clock input
D_1 - D_{13}	Data Input - clocked in on the crossing of the rising edge of CLK and the falling edge of $\overline{CLK}$
Center PAD	Ground (MLF package only)

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = –40°C to +85°C, V_{DD} = 2.5V ±0.2V, V_{DDQ} = 2.5V ±0.2V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IK}	Control Inputs	V_{DD} = 2.3V, I_I = –18mA	—	—	–1.2	V
V_{OH}		V_{DD} = 2.3V to 2.7V, I_{OH} = -100µA	V_{DD} – 0.2	—	—	V
		V_{DD} = 2.3V, I_{OH} = -16mA	1.95	—	—	
V_{OL}		V_{DD} = 2.3V to 2.7V, I_{OL} = 100µA	—	—	0.2	V
		V_{DD} = 2.3V, I_{OL} = 16mA	—	—	0.35	
I_I	All Inputs	V_{DD} = 2.7V, V_I = V_{DD} or GND	—	—	±5	µA
I_{DD}	Static Standby	I_O = 0, V_{DD} = 2.7V, $\overline{RESET}$ = GND	—	—	0.01	mA
	Static Operating	I_O = 0, V_{DD} = 2.7V, $\overline{RESET}$ = V_{DD}, V_I = $V_{IH\ (AC)}$ or $V_{IL\ (AC)}$	—	—	20	
I_{DDD}	Dynamic Operating (Clock Only)	I_O = 0, V_{DD} = 2.7V, $\overline{RESET}$ = V_{DD}, V_I = $V_{IH\ (AC)}$ or $V_{IL\ (AC)}$, CLK and $\overline{CLK}$ Switching 50% Duty Cycle.	—	6	—	µA/Clock MHz
	Dynamic Operating (Per Each Data Input)[1]	I_O = 0, V_{DD} = 2.7V, $\overline{RESET}$ = V_{DD}, V_I = $V_{IH\ (AC)}$ or $V_{IL\ (AC)}$, CLK and $\overline{CLK}$ Switching 50% Duty Cycle. One Data Input Switching at Half Clock Frequency, 50% Duty Cycle.	—	43	—	µA/Clock MHz/Data Input
r_{OH}	Output HIGH	V_{DD} = 2.3V to 2.7V, I_{OH} = -20mA	7	—	20	Ω
r_{OL}	Output LOW	V_{DD} = 2.3V to 2.7V, I_{OH} = 20mA	7	—	20	Ω
$r_{O(\Delta)}$	$\lvert r_{OH} - r_{OL} \rvert$ each separate bit	V_{DD} = 2.5V, T_A = 25°C, I_{OH} = -20mA	—	—	4	Ω
C_I	Data Inputs	V_{DD} = 2.5V, V_I = V_{REF} ± 310mV	2	—	3	pF
	CLK and $\overline{CLK}$	V_{ICR} = 1.25V, $V_{I\ (PP)}$ = 360mV	2	—	3	
	$\overline{RESET}$	V_I = V_{DD} or GND	2	—	3	

NOTE:
1. Power dissipation levels will allow operation at DDR333 speeds without excessive die temperature.

© 2019 Renesas Electronics Corporation

OPERATING CHARACTERISTICS, T_A = 25ºC (1)

Symbol	Parameter		Min.	Typ.(1)	Max.	Unit
V_{DD}	Supply Voltage		V_{DDQ}	—	2.7	V
V_{DDQ}	Output Supply Voltage		2.3	2.5	2.7	V
V_{REF}	Reference Voltage (V_{REF}=V_{DDQ}/2)		1.15	1.25	1.35	V
V_{TT}	Termination Voltage		V_{REF}– 40mV	V_{REF}	V_{REF}+ 40mV	V
V_I	Input Voltage		0	—	V_{DD}	V
V_{IH}	AC High-Level Input Voltage	Data Inputs	V_{REF}+ 310mV	—	—	V
V_{IL}	AC Low-Level Input Voltage	Data Inputs	—	—	V_{REF}– 310mV	V
V_{IH}	DC High-Level Input Voltage	Data Inputs	V_{REF}+ 150mV	—	—	V
V_{IL}	DC Low-Level Input Voltage	Data Inputs	—	—	V_{REF}– 150mV	V
V_{IH}	High-Level Input Voltage	$\overline{RESET}$	1.7	—	—	V
V_{IL}	Low-Level Input Voltage	$\overline{RESET}$	—	—	0.7	V
V_{ICR}	Common-Mode Input Range	CLK, $\overline{CLK}$	0.97	—	1.53	V
$V_{I(PP)}$	Peak-to-Peak Input Voltage	CLK, $\overline{CLK}$	360	—	—	mV
I_{OH}	High-Level Output Current		—	—	– 20	mA
I_{OL}	Low-Level Output Current		—	—	20	
T_A	Operating Free-Air Temperature		– 40	—	+85	°C

NOTE:

1. The $\overline{RESET}$ input of the device must be held at V_{DD} or GND to ensure proper device operation.

TIMING REQUIREMENTS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE

Symbol	Parameter		V_{DD} = 2.5V ± 0.2V		Unit
			Min.	Max.	
f_{CLOCK}	Clock Frequency		—	200	MHz
t_W	Pulse Duration, CLK, $\overline{CLK}$ HIGH or LOW		2.5	—	ns
t_{ACT}	Differential Inputs Active Time(1)		—	22	ns
t_{INACT}	Differential Inputs Inactive Time(2)		—	22	ns
t_{SU}	Setup Time, Fast Slew Rate(3, 5)	Data Before CLK↑, CLK↓	0.75	—	ns
	Setup Time, Slow Slew Rate(4, 5)		0.9	—	ns
t_H	Hold Time, Fast Slew Rate(3,5)	Data Before CLK↑, CLK ↓	0.75	—	ns
	Hold Time, Slow Slew Rate(2,5)		0.9	—	ns

NOTES:

1. Data inputs must be low a minimum time of t_{ACT} max., after $\overline{RESET}$ is taken HIGH.
2. Data and clock inputs must be held at valid levels (not floating) a minimum time of t_{INACT} max., after $\overline{RESET}$ is taken LOW.
3. For data signal input slew rate is ≥1V/ns.
4. For data signal input slew rate is ≥0.5V/ns and <1V/ns.
5. CLK, $\overline{CLK}$ signal input slew rates are ≥1V/ns.

SWITCHING CHARACTERISTICS OVER RECOMMENDED FREE-AIR OPERATING RANGE (UNLESS OTHERWISE NOTED)

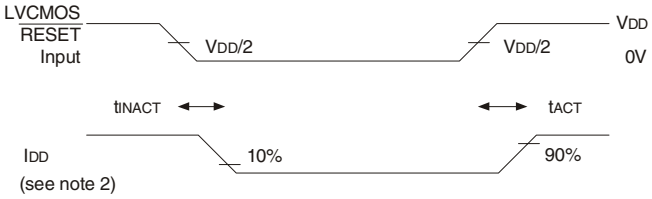
Symbol	Parameter	V_{DD} = 2.5V ± 0.2V		Unit
		Min	Max.	
f_{MAX}		200	—	MHz
t_{PD}	CLK and $\overline{CLK}$ to Q	1.1	2.8	ns
t_{PHL}	$\overline{RESET}$ to Q	—	5	ns

© 2019 Renesas Electronics Corporation

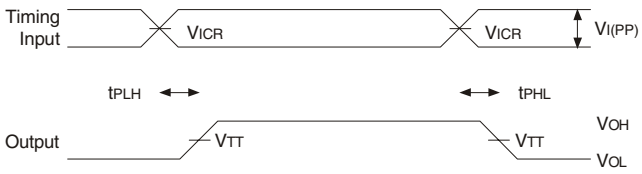
TEST CIRCUITS AND WAVEFORMS (V_{DD} = 2.5V ± 0.2V)



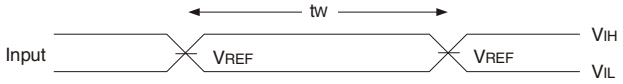
Load Circuit



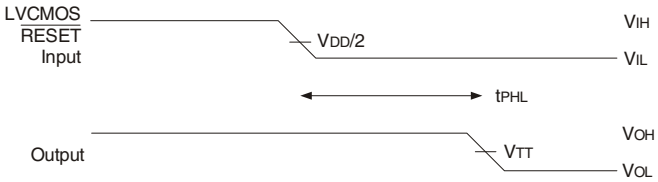
Voltage and Current Waveforms
Inputs Active and Inactive Times



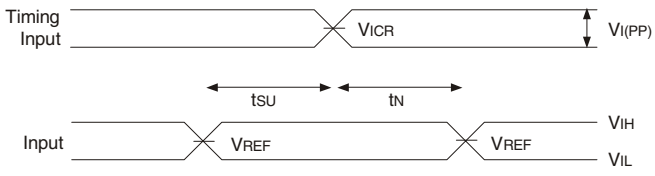
Voltage Waveforms - Propagation Delay Times



Voltage Waveforms - Pulse Duration



Voltage Waveforms - Propagation Delay Times

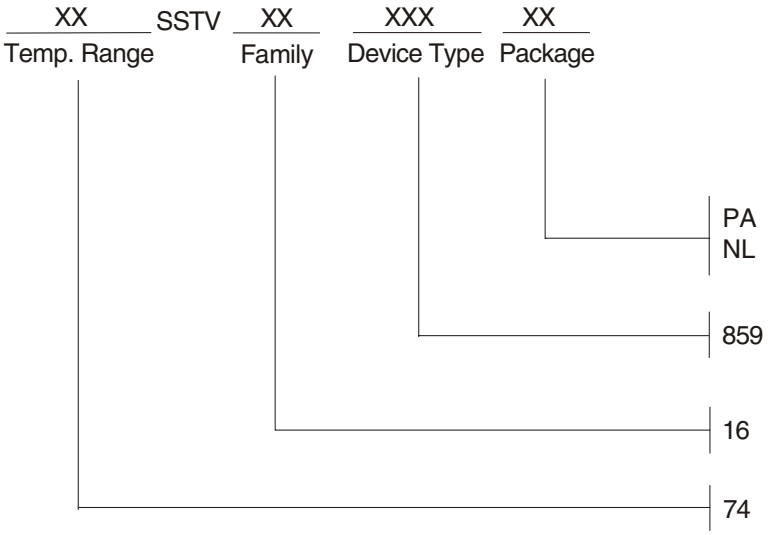


Voltage Waveforms - Setup and Hold Times

NOTES:
1. C_L includes probe and jig capacitance.
2. I_{DD} tested with clock and data inputs held at V_{DD} or GND, and I_O = 0mA.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Z_O = 50Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).
4. The outputs are measured one at a time with one transition per measurement.
5. $V_{TT} = V_{REF} = V_{DDQ}/2$
6. $V_{IH} = V_{REF}$ + 310mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS input.
7. $V_{IL} = V_{REF}$ - 310mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
8. t_{PLH} and t_{PHL} are the same as t_{PD}.

© 2019 Renesas Electronics Corporation

ORDERING INFORMATION



PA	Thin Shrink Small Outline Package
NL	Thermally Enhanced Plastic Very Fine Pitch Quad Flat No Lead Package
859	13-Bit to 26-Bit Registered Buffer with SSTL I/O
16	Double-Density
74	–40°C to +85°C

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2026 Renesas Electronics Corporation. All rights reserved.