

**FEATURES:**

- Typical  $t_{SK(o)}$  (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$ , Normal Range
- $V_{CC} = 2.7V$  to  $3.6V$ , Extended Range
- CMOS power levels ( $0.4\mu W$  typ. static)
- All inputs, outputs, and I/O are 5V tolerant
- Supports hot insertion
- Available in TSSOP package

**DRIVE FEATURES:**

- High Output Drivers:  $\pm 24mA$
- Reduced system switching noise

**APPLICATIONS:**

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

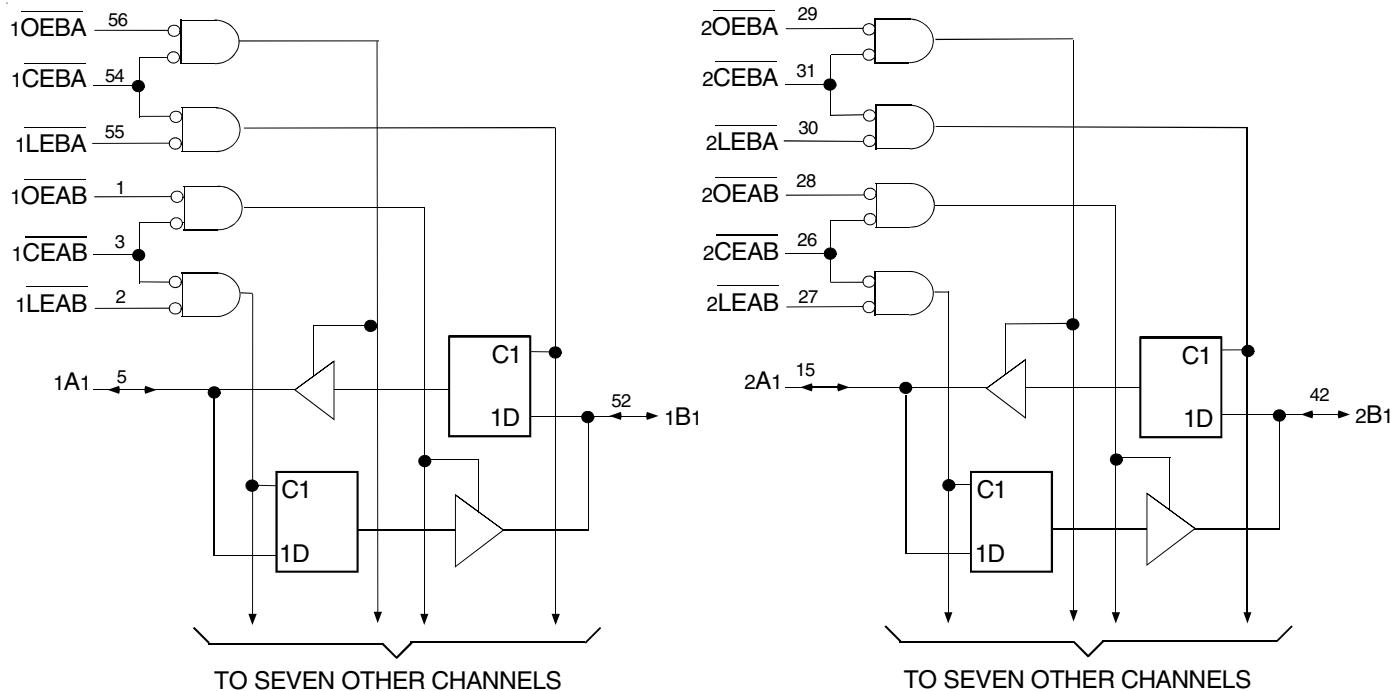
**DESCRIPTION**

The LVCH16543A 16-bit registered transceiver is built using advanced dual metal CMOS technology. The LVCH16543A can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable ( $\overline{LEAB}$  or  $\overline{LEBA}$ ) and output-enable ( $\overline{OEAB}$  or  $\overline{OEBA}$ ) inputs are provided for each register to permit independent control in either direction of data flow. The A-to-B enable ( $\overline{CEAB}$ ) input must be low in order to enter data from the A port or to output data from the B port.  $\overline{LEAB}$  controls the latch function. When  $\overline{LEAB}$  is low, the A to B latches are transparent. A subsequent low-to-high transition of  $\overline{LEAB}$  puts the A latches in the storage mode.  $\overline{OEAB}$  performs output enable function on the B port. Data flow from the B port to the A port is similar but requires using  $\overline{CEBA}$ ,  $\overline{LEBA}$ , and  $\overline{OEBA}$  inputs. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

All pins of this 16-bit registered transceiver can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVCH16543A has been designed with a  $\pm 24mA$  output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The LVCH16543A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

**FUNCTIONAL BLOCK DIAGRAM**

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**INDUSTRIAL TEMPERATURE RANGE**

## PIN CONFIGURATION

1OEAB	1	56	1OEBA
1LEAB	2	55	1LEBA
1CEAB	3	54	1CEBA
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
Vcc	7	50	Vcc
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
Vcc	22	35	Vcc
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2CEAB	26	31	2CEBA
2LEAB	27	30	2LEBA
2OEAB	28	29	2OEBA

TSSOP  
TOP VIEWABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +6.5	V
TSTG	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	DC Output Current	-50 to +50	mA
I <sub>IK</sub>	Continuous Clamp Current, V <sub>I</sub> < 0 or V <sub>O</sub> < 0	-50	mA
I <sub>CC</sub>	Continuous Current through each V <sub>CC</sub> or GND	±100	mA
I <sub>SS</sub>			

## NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## PIN DESCRIPTION

Pin Names	Description
x <sub>OEAB</sub>	A-to-B Output Enable Input (Active LOW)
x <sub>OEBA</sub>	B-to-A Output Enable Input (Active LOW)
x <sub>CEAB</sub>	A-to-B Enable Input (Active LOW)
x <sub>CEBA</sub>	B-to-A Enable Input (Active LOW)
x <sub>LEAB</sub>	A-to-B Latch Enable Input (Active LOW)
x <sub>LEBA</sub>	B-to-A Latch Enable Input (Active LOW)
x <sub>Ax</sub>	A-to-B Data Inputs or B-to-A 3-State Outputs <sup>(1)</sup>
x <sub>Bx</sub>	B-to-A Data Inputs or A-to-B 3-State Outputs <sup>(1)</sup>

## NOTE:

1. These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLE (EACH 8-BIT SECTION)<sup>(1,2)</sup>

Inputs			Latch Status	Output Buffers
x <sub>CEAB</sub>	x <sub>LEAB</sub>	x <sub>OEAB</sub>	x <sub>Ax</sub> to x <sub>Bx</sub>	x <sub>Bx</sub>
H	X	X	Storing	High Z
X	X	H	Storing	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous <sup>(3)</sup> A Inputs
L	L	H	Transparent	High Z
L	H	H	Storing	High Z
X	H	X	Storing	Not Recommended

## NOTES:

1. H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High-Impedance
2. A-to-B data flow is shown. B-to-A data flow is similar but uses x<sub>CEBA</sub>, x<sub>LEBA</sub>, and x<sub>OEBA</sub>.
3. Before x<sub>LEAB</sub> LOW-to-HIGH transition.

CAPACITANCE (T<sub>A</sub> = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	6.5	8	pF
C <sub>I/O</sub>	I/O Port Capacitance	V <sub>IN</sub> = 0V	6.5	8	pF

## NOTE:

1. As applicable to the device type.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $TA = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
VIH	Input HIGH Voltage Level	V <sub>CC</sub> = 2.3V to 2.7V		1.7	—	—	V
		V <sub>CC</sub> = 2.7V to 3.6V		2	—	—	
VIL	Input LOW Voltage Level	V <sub>CC</sub> = 2.3V to 2.7V		—	—	0.7	V
		V <sub>CC</sub> = 2.7V to 3.6V		—	—	0.8	
I <sub>IH</sub> I <sub>IL</sub>	Input Leakage Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = 0 to 5.5V	—	—	$\pm 5$	$\mu\text{A}$
I <sub>OZH</sub> I <sub>OZL</sub>	High Impedance Output Current (3-State Output pins)	V <sub>CC</sub> = 3.6V	V <sub>O</sub> = 0 to 5.5V	—	—	$\pm 10$	$\mu\text{A}$
I <sub>OFF</sub>	Input/Output Power Off Leakage	V <sub>CC</sub> = 0V, V <sub>IN</sub> or V <sub>O</sub> $\leq$ 5.5V		—	—	$\pm 50$	$\mu\text{A}$
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>CC</sub> = 2.3V, I <sub>IN</sub> = $-18\text{mA}$		—	-0.7	-1.2	V
V <sub>H</sub>	Input Hysteresis	V <sub>CC</sub> = 3.3V		—	100	—	mV
I <sub>ICL</sub> I <sub>ICCH</sub> I <sub>ICCZ</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = 3.6V	V <sub>IN</sub> = GND or V <sub>CC</sub>	—	—	10	$\mu\text{A}$
			3.6 $\leq$ V <sub>IN</sub> $\leq$ 5.5V <sup>(2)</sup>	—	—	10	
$\Delta I_{CC}$	Quiescent Power Supply Current Variation	One input at V <sub>CC</sub> - 0.6V, other inputs at V <sub>CC</sub> or GND		—	—	500	$\mu\text{A}$

NOTES:

1. Typical values are at V<sub>CC</sub> = 3.3V,  $+25^{\circ}\text{C}$  ambient.

2. This applies in the disabled state only.

## BUS-HOLD CHARACTERISTICS

Symbol	Parameter <sup>(1)</sup>	Test Conditions		Min.	Typ. <sup>(2)</sup>	Max.	Unit
I <sub>BHH</sub> I <sub>BHL</sub>	Bus-Hold Input Sustain Current	V <sub>CC</sub> = 3V	V <sub>I</sub> = 2V	-75	—	—	$\mu\text{A}$
			V <sub>I</sub> = 0.8V	75	—	—	
I <sub>BHH</sub> I <sub>BHL</sub>	Bus-Hold Input Sustain Current	V <sub>CC</sub> = 2.3V	V <sub>I</sub> = 1.7V	—	—	—	$\mu\text{A}$
			V <sub>I</sub> = 0.7V	—	—	—	
I <sub>BHHO</sub> I <sub>BHLO</sub>	Bus-Hold Input Overdrive Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = 0 to 3.6V	—	—	$\pm 500$	$\mu\text{A}$

NOTES:

1. Pins with Bus-Hold are identified in the pin description.

2. Typical values are at V<sub>CC</sub> = 3.3V,  $+25^{\circ}\text{C}$  ambient.

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
VOH	Output HIGH Voltage	Vcc = 2.3V to 3.6V	IOH = - 0.1mA	Vcc - 0.2	—	V
		Vcc = 2.3V	IOH = - 6mA	2	—	
		Vcc = 2.3V	IOH = - 12mA	1.7	—	
		Vcc = 2.7V		2.2	—	
		Vcc = 3V	IOH = - 24mA	2.4	—	
		Vcc = 3V		2	—	
VOL	Output LOW Voltage	Vcc = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		Vcc = 2.3V	IOL = 6mA	—	0.4	
		Vcc = 2.7V	IOL = 12mA	—	0.7	
		Vcc = 3V	IOL = 12mA	—	0.4	
		Vcc = 3V	IOL = 24mA	—	0.55	

## NOTE:

1.  $V_{IH}$  and  $V_{IL}$  must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate  $V_{cc}$  range.  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

## OPERATING CHARACTERISTICS, $V_{cc} = 3.3\text{V} \pm 0.3\text{V}$ , $T_A = 25^\circ\text{C}$

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per Transceiver Outputs enabled	$CL = 0\text{pF}$ , $f = 10\text{MHz}$	44	$\text{pF}$
CPD	Power Dissipation Capacitance per Transceiver Outputs disabled		4	

## SWITCHING CHARACTERISTICS<sup>(1)</sup>

Symbol	Parameter	$V_{cc} = 2.7\text{V}$		$V_{cc} = 3.3\text{V} \pm 0.3\text{V}$		Unit
		Min.	Max.	Min.	Max.	
$t_{PLH}$	Propagation Delay, Transparent Mode $x_{Ax}$ to $x_{Bx}$ or $x_{Bx}$ to $x_{Ax}$	—	6.1	1.2	5.4	ns
$t_{PHL}$	Propagation Delay $x_{LEB\bar{A}}$ to $x_{Ax}$ , $x_{LEA\bar{B}}$ to $x_{Bx}$	—	7.4	1.5	6.1	ns
$t_{PZH}$	Output Enable Time $x_{CEB\bar{A}}$ or $x_{CEA\bar{B}}$ to $x_{Ax}$ or $x_{Bx}$	—	7.9	1.2	6.6	ns
$t_{PZL}$	Output Enable Time $x_{OE\bar{B}A}$ or $x_{OE\bar{A}B}$ to $x_{Ax}$ or $x_{Bx}$	—	7.6	1	6.3	ns
$t_{PHZ}$	Output Disable Time $x_{CEB\bar{A}}$ or $x_{CEA\bar{B}}$ to $x_{Ax}$ or $x_{Bx}$	—	7.1	1.5	6.6	ns
$t_{PLZ}$	Output Disable Time $x_{OE\bar{B}A}$ or $x_{OE\bar{A}B}$ to $x_{Ax}$ or $x_{Bx}$	—	6.9	1.5	6.3	ns
$t_{SU}$	Set-up Time, data before $\bar{CE} \uparrow$	1.1	—	1.1	—	ns
$t_{SU}$	Set-up Time, data before $\bar{LE} \uparrow$ , $\bar{CE}$ LOW	1.1	—	1.1	—	ns
$t_H$	Hold Time, data after $\bar{CE} \uparrow$	1.9	—	1.9	—	ns
$t_H$	Hold Time, data after $\bar{LE} \uparrow$ , $\bar{CE}$ LOW	1.9	—	1.9	—	ns
$t_W$	Pulse Duration, $x_{LEB\bar{A}}$ or $x_{LEA\bar{B}}$ , $x_{CEB\bar{A}}$ or $x_{CEA\bar{B}}$ LOW	3.3	—	3.3	—	ns
$t_{sk(o)}$	Output Skew <sup>(2)</sup>	—	—	—	500	ps

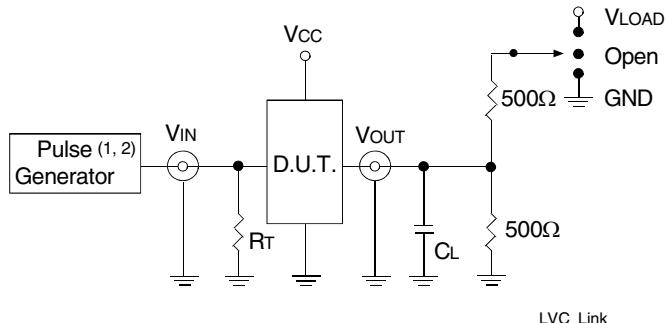
## NOTES:

1. See TEST CIRCUITS AND WAVEFORMS.  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .
2. Skew between any two outputs of the same package and switching in the same direction.

## TEST CIRCUITS AND WAVEFORMS

### TEST CONDITIONS

Symbol	$V_{CC}^{(1)} = 3.3V \pm 0.3V$	$V_{CC}^{(1)} = 2.7V$	$V_{CC}^{(2)} = 2.5V \pm 0.2V$	Unit
$V_{LOAD}$	6	6	$2 \times V_{CC}$	V
$V_{IH}$	2.7	2.7	$V_{CC}$	V
$V_T$	1.5	1.5	$V_{CC} / 2$	V
$V_{LZ}$	300	300	150	mV
$V_{HZ}$	300	300	150	mV
$C_L$	50	50	30	pF



Test Circuit for All Outputs

#### DEFINITIONS:

$C_L$  = Load capacitance: includes jig and probe capacitance.

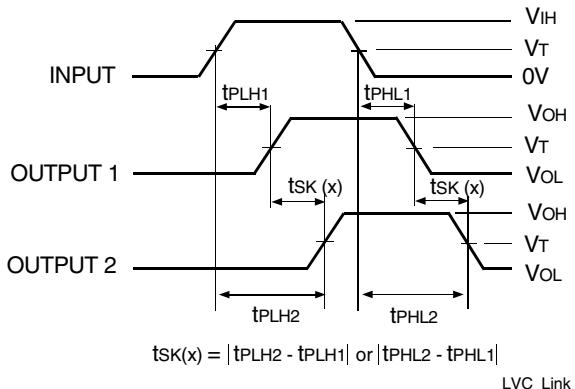
$R_T$  = Termination resistance: should be equal to  $Z_{OUT}$  of the Pulse Generator.

#### NOTES:

1. Pulse Generator for All Pulses: Rate  $\leq 10MHz$ ;  $t_f \leq 2.5ns$ ;  $t_r \leq 2.5ns$ .
2. Pulse Generator for All Pulses: Rate  $\leq 10MHz$ ;  $t_f \leq 2ns$ ;  $t_r \leq 2ns$ .

## SWITCH POSITION

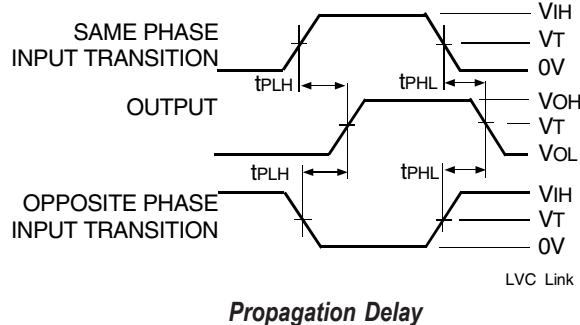
Test	Switch
Open Drain	
Disable Low	$V_{LOAD}$
Enable Low	
Disable High	$GND$
All Other Tests	Open



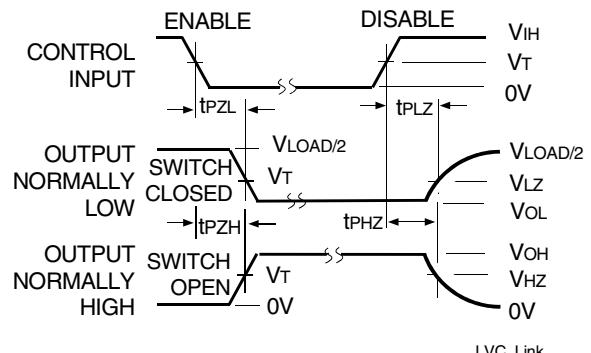
Output Skew -  $tsk(x)$

#### NOTES:

1. For  $tsk(o)$  OUTPUT1 and OUTPUT2 are any two outputs.
2. For  $tsk(b)$  OUTPUT1 and OUTPUT2 are in the same bank.



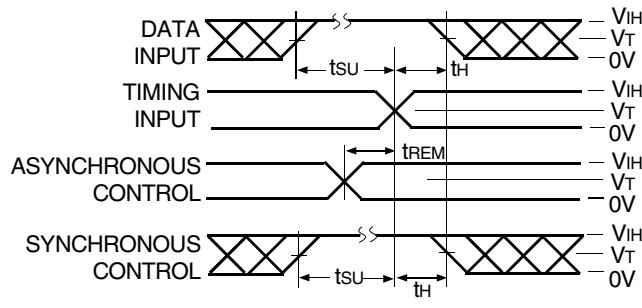
Propagation Delay



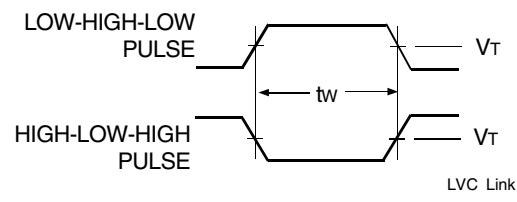
Enable and Disable Times

#### NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

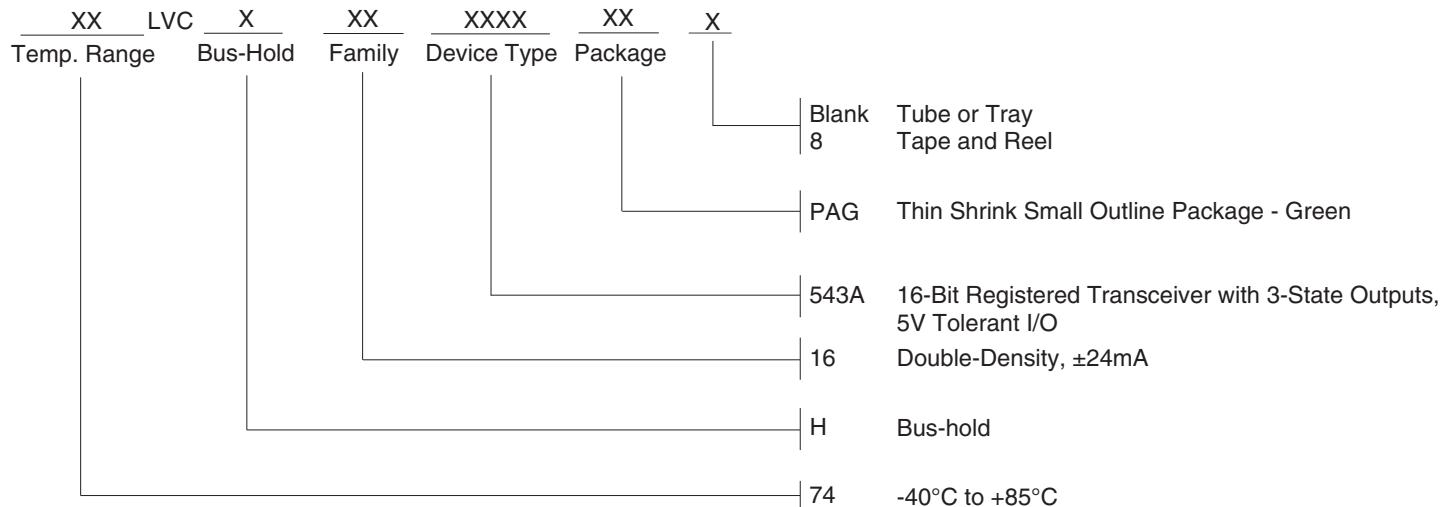


Set-up, Hold, and Release Times



Pulse Width

## ORDERING INFORMATION



## DATASHEET DOCUMENT HISTORY

01/21/2016 Pg. 6

Updated the ordering information by removing IDT notation and adding Tape and Reel information.

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