## FEATURES:

- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- **ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)**
- **$V_{CC}$ = 3.3V ± 0.3V, Normal Range**
- **$V_{CC}$ = 2.7V to 3.6V, Extended Range**
- **CMOS power levels (0.4µ W typ. static)**
- **All inputs, outputs, and I/O are 5V tolerant**
- **Supports hot insertion**
- **Available in SSOP and TSSOP packages**

## DRIVE FEATURES:

- **High Output Drivers: ±24mA**
- **Reduced system switching noise**

## APPLICATIONS:

- **5V and 3.3V mixed voltage systems**
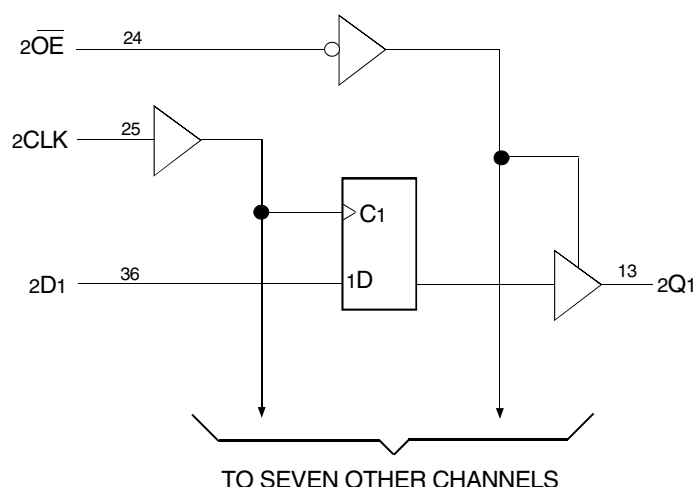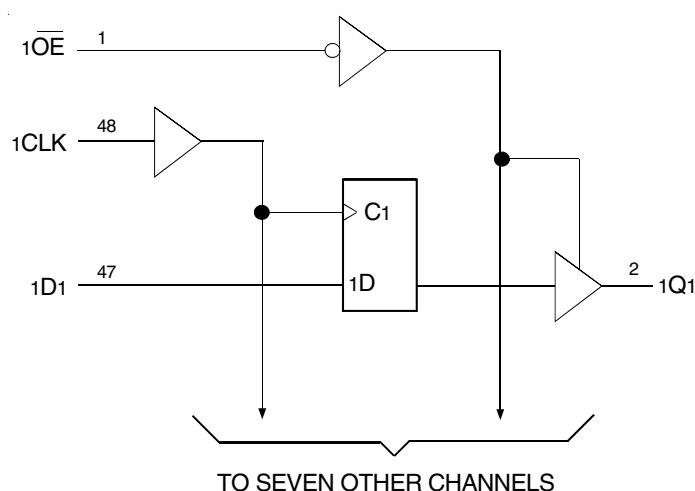- **Data communication and telecommunication systems**

## DESCRIPTION

The LVCH16374A 16-bit edge-triggered D-type register is built using advanced dual metal CMOS technology. This high-speed, low-power register is ideal for use as a buffer register for data synchronization and storage. The Output Enable ($\overline{OE}$) and clock (CLK) controls are organized to operate each device as two 8-bit registers or one 16-bit register with common clock. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.
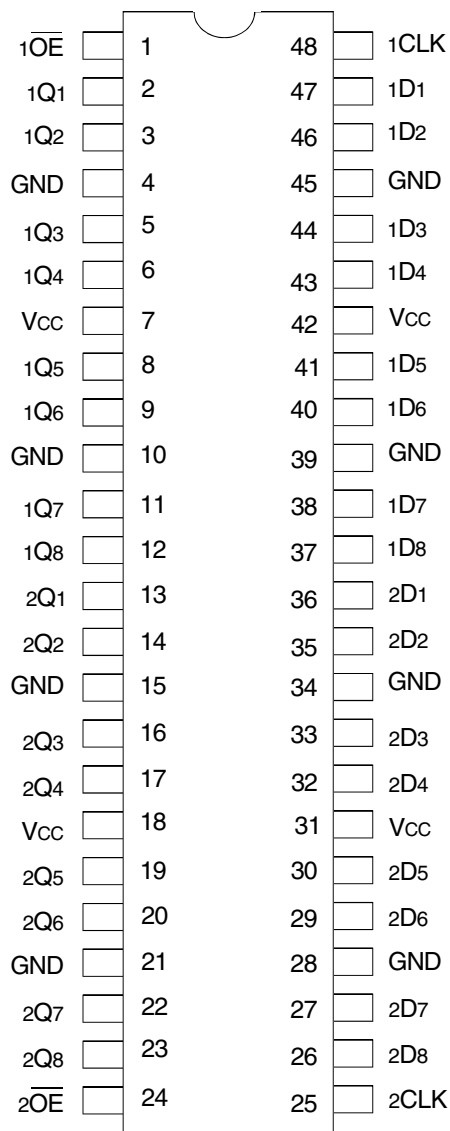
All pins of the LVCH16374A can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVCH16374A has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The LVCH16374A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

## FUNCTIONAL BLOCK DIAGRAM



TO SEVEN OTHER CHANNELS          TO SEVEN OTHER CHANNELS

**INDUSTRIAL TEMPERATURE RANGE**                    **OCTOBER 2015**

DSC-4643/5

## PIN CONFIGURATION

| | | | |
|---|---|---|---|
| 1$\overline{\text{OE}}$ | 1 | 48 | 1CLK |
| 1Q1 | 2 | 47 | 1D1 |
| 1Q2 | 3 | 46 | 1D2 |
| GND | 4 | 45 | GND |
| 1Q3 | 5 | 44 | 1D3 |
| 1Q4 | 6 | 43 | 1D4 |
| V$_{CC}$ | 7 | 42 | V$_{CC}$ |
| 1Q5 | 8 | 41 | 1D5 |
| 1Q6 | 9 | 40 | 1D6 |
| GND | 10 | 39 | GND |
| 1Q7 | 11 | 38 | 1D7 |
| 1Q8 | 12 | 37 | 1D8 |
| 2Q1 | 13 | 36 | 2D1 |
| 2Q2 | 14 | 35 | 2D2 |
| GND | 15 | 34 | GND |
| 2Q3 | 16 | 33 | 2D3 |
| 2Q4 | 17 | 32 | 2D4 |
| V$_{CC}$ | 18 | 31 | V$_{CC}$ |
| 2Q5 | 19 | 30 | 2D5 |
| 2Q6 | 20 | 29 | 2D6 |
| GND | 21 | 28 | GND |
| 2Q7 | 22 | 27 | 2D7 |
| 2Q8 | 23 | 26 | 2D8 |
| 2$\overline{\text{OE}}$ | 24 | 25 | 2CLK |

**SSOP / TSSOP**
**TOP VIEW**

## ABSOLUTE MAXIMUM RATINGS[1]

| Symbol | Description | Max | Unit |
|---|---|---|---|
| V$_{TERM}$ | Terminal Voltage with Respect to GND | –0.5 to +6.5 | V |
| T$_{STG}$ | Storage Temperature | –65 to +150 | °C |
| I$_{OUT}$ | DC Output Current | –50 to +50 | mA |
| I$_{IK}$ I$_{OK}$ | Continuous Clamp Current, V$_I$ < 0 or V$_O$ < 0 | –50 | mA |
| I$_{CC}$ I$_{SS}$ | Continuous Current through each V$_{CC}$ or GND | ±100 | mA |

**NOTE:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE (T$_A$ = +25°C, F = 1.0MHz)

| Symbol | Parameter[1] | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| C$_{IN}$ | Input Capacitance | V$_{IN}$ = 0V | 4.5 | 6 | pF |
| C$_{OUT}$ | Output Capacitance | V$_{OUT}$ = 0V | 6.5 | 8 | pF |
| C$_{I/O}$ | I/O Port Capacitance | V$_{IN}$ = 0V | 6.5 | 8 | pF |

**NOTE:**
1. As applicable to the device type.

## PIN DESCRIPTION

| Pin Names | Description |
|---|---|
| xDx | Data Inputs[1] |
| xCLK | Clock Inputs |
| x$\overline{\text{OE}}$ | Output Enable Inputs (Active LOW) |
| xQx | 3-State Outputs |

**NOTE:**
1. These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

## FUNCTION TABLE (EACH FLIP-FLOP)[1]

| Inputs | | | Outputs |
|---|---|---|---|
| xDx | xCLK | x$\overline{\text{OE}}$ | xQx |
| H | ↑ | L | H |
| L | ↑ | L | L |
| X | H or L | L | Q[2] |
| X | X | H | Z |

**NOTES:**
1. H = HIGH Voltage Level
   X = Don't Care
   L = LOW Voltage Level
   Z = High-Impedance
   ↑ = LOW-to-HIGH transition
2. Output level before the indicated steady-state input conditions were established.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: $T_A$ = –40°C to +85°C

| Symbol | Parameter | Test Conditions | | Min. | Typ.[1] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage Level | $V_{CC}$ = 2.3V to 2.7V | | 1.7 | — | — | V |
| | | $V_{CC}$ = 2.7V to 3.6V | | 2 | — | — | |
| $V_{IL}$ | Input LOW Voltage Level | $V_{CC}$ = 2.3V to 2.7V | | — | — | 0.7 | V |
| | | $V_{CC}$ = 2.7V to 3.6V | | — | — | 0.8 | |
| $I_{IH}$ $I_{IL}$ | Input Leakage Current | $V_{CC}$ = 3.6V | $V_I$ = 0 to 5.5V | — | — | ±5 | µA |
| $I_{OZH}$ $I_{OZL}$ | High Impedance Output Current (3-State Output pins) | $V_{CC}$ = 3.6V | $V_O$ = 0 to 5.5V | — | — | ±10 | µA |
| $I_{OFF}$ | Input/Output Power Off Leakage | $V_{CC}$ = 0V, $V_{IN}$ or $V_O$ ≤ 5.5V | | — | — | ±50 | µA |
| $V_{IK}$ | Clamp Diode Voltage | $V_{CC}$ = 2.3V, $I_{IN}$ = –18mA | | — | –0.7 | –1.2 | V |
| $V_H$ | Input Hysteresis | $V_{CC}$ = 3.3V | | — | 100 | — | mV |
| $I_{CCL}$ $I_{CCH}$ $I_{CCZ}$ | Quiescent Power Supply Current | $V_{CC}$ = 3.6V | $V_{IN}$ = GND or $V_{CC}$ | — | — | 10 | µA |
| | | | 3.6 ≤ $V_{IN}$ ≤ 5.5V[2] | — | — | 10 | |
| $\Delta I_{CC}$ | Quiescent Power Supply Current Variation | One input at $V_{CC}$ - 0.6V, other inputs at $V_{CC}$ or GND | | — | — | 500 | µA |

**NOTES:**
1. Typical values are at $V_{CC}$ = 3.3V, +25°C ambient.
2. This applies in the disabled state only.

## BUS-HOLD CHARACTERISTICS

| Symbol | Parameter[1] | Test Conditions | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{BHH}$ | Bus-Hold Input Sustain Current | $V_{CC}$ = 3V | $V_I$ = 2V | –75 | — | — | µA |
| $I_{BHL}$ | | | $V_I$ = 0.8V | 75 | — | — | |
| $I_{BHH}$ | Bus-Hold Input Sustain Current | $V_{CC}$ = 2.3V | $V_I$ = 1.7V | — | — | — | µA |
| $I_{BHL}$ | | | $V_I$ = 0.7V | — | — | — | |
| $I_{BHHO}$ $I_{BHLO}$ | Bus-Hold Input Overdrive Current | $V_{CC}$ = 3.6V | $V_I$ = 0 to 3.6V | — | — | ±500 | µA |

**NOTES:**
1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at $V_{CC}$ = 3.3V, +25°C ambient.

## OUTPUT DRIVE CHARACTERISTICS

| Symbol | Parameter | Test Conditions[1] | | Min. | Max. | Unit |
|--------|-----------|--------------------|---|------|------|------|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = 2.3V to 3.6V | $I_{OH}$ = – 0.1mA | $V_{CC}$ – 0.2 | — | V |
| | | $V_{CC}$ = 2.3V | $I_{OH}$ = – 6mA | 2 | — | |
| | | $V_{CC}$ = 2.3V | $I_{OH}$ = – 12mA | 1.7 | — | |
| | | $V_{CC}$ = 2.7V | | 2.2 | — | |
| | | $V_{CC}$ = 3V | | 2.4 | — | |
| | | $V_{CC}$ = 3V | $I_{OH}$ = – 24mA | 2.2 | — | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = 2.3V to 3.6V | $I_{OL}$ = 0.1mA | — | 0.2 | V |
| | | $V_{CC}$ = 2.3V | $I_{OL}$ = 6mA | — | 0.4 | |
| | | | $I_{OL}$ = 12mA | — | 0.7 | |
| | | $V_{CC}$ = 2.7V | $I_{OL}$ = 12mA | — | 0.4 | |
| | | $V_{CC}$ = 3V | $I_{OL}$ = 24mA | — | 0.55 | |

**NOTE:**
1. $V_{IH}$ and $V_{IL}$ must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate $V_{CC}$ range. $T_A$ = – 40°C to + 85°C.

## OPERATING CHARACTERISTICS, $V_{CC}$ = 3.3V ± 0.3V, $T_A$ = 25°C

| Symbol | Parameter | Test Conditions | Typical | Unit |
|--------|-----------|-----------------|---------|------|
| $C_{PD}$ | Power Dissipation Capacitance per Flip-Flop Outputs enabled | $C_L$ = 0pF, f = 10Mhz | 58 | pF |
| $C_{PD}$ | Power Dissipation Capacitance per Flip-Flop Outputs disabled | | 24 | |

## SWITCHING CHARACTERISTICS[1]

| Symbol | Parameter | $V_{CC}$ = 2.7V | | $V_{CC}$ = 3.3V ± 0.3V | | Unit |
|--------|-----------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | |
| $f_{MAX}$ | | 150 | — | 150 | — | MHz |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay xCLK to xQx | — | 4.9 | 1.5 | 4.5 | ns |
| $t_{PZH}$ $t_{PZL}$ | Output Enable Time x$\overline{OE}$ to xQx | — | 5.3 | 1.5 | 4.6 | ns |
| $t_{PHZ}$ $t_{PLZ}$ | Output Disable Time x$\overline{OE}$ to xQx | — | 6.1 | 1.5 | 5.5 | ns |
| $t_{SU}$ | Set-up Time HIGH or LOW, data before CLK↑ | 1.9 | — | 1.9 | — | ns |
| $t_H$ | Hold Time HIGH or LOW, data after CLK↑ | 1.1 | — | 1.1 | — | ns |
| $t_W$ | Pulse duration, CLK HIGH or LOW | 3.3 | — | 3.3 | — | ns |
| $t_{SK(o)}$ | Output Skew[2] | — | — | — | 500 | ps |

**NOTES:**
1. See TEST CIRCUITS AND WAVEFORMS. $T_A$ = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

## TEST CIRCUITS AND WAVEFORMS
## TEST CONDITIONS

| Symbol | $V_{CC}^{(1)}$=3.3V±0.3V | $V_{CC}^{(1)}$=2.7V | $V_{CC}^{(2)}$=2.5V±0.2V | Unit |
|--------|------------|------------|--------------|------|
| $V_{LOAD}$ | 6 | 6 | 2 x Vcc | V |
| $V_{IH}$ | 2.7 | 2.7 | Vcc | V |
| $V_T$ | 1.5 | 1.5 | Vcc / 2 | V |
| $V_{LZ}$ | 300 | 300 | 150 | mV |
| $V_{HZ}$ | 300 | 300 | 150 | mV |
| $C_L$ | 50 | 50 | 30 | pF |



*Test Circuit for All Outputs*       LVC Link
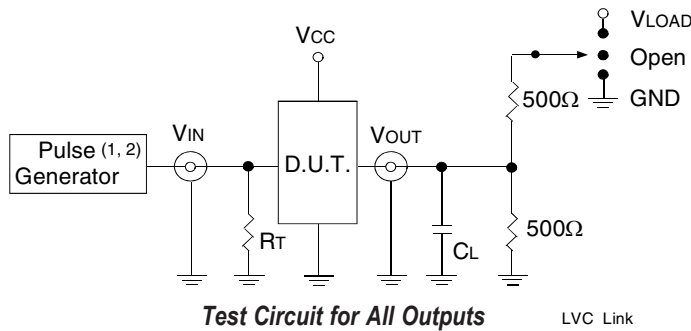
**DEFINITIONS:**
$C_L$ = Load capacitance: includes jig and probe capacitance.
$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator.

**NOTES:**
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; $t_F$ ≤ 2.5ns; $t_R$ ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; $t_F$ ≤ 2ns; $t_R$ ≤ 2ns.

## SWITCH POSITION

| Test | Switch |
|------|--------|
| Open Drain Disable Low Enable Low | $V_{LOAD}$ |
| Disable High Enable High | GND |
| All Other Tests | Open |
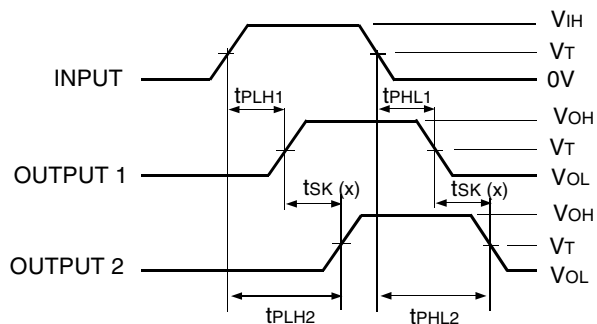


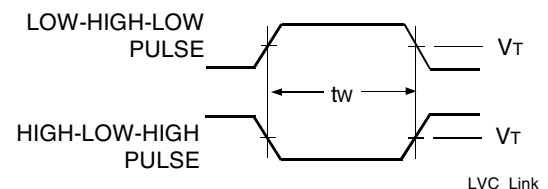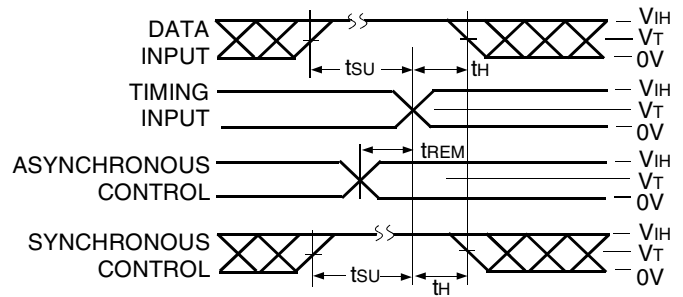$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

*Output Skew - $t_{SK}(x)$*       LVC Link

**NOTES:**
1. For $t_{SK}(o)$ OUTPUT1 and OUTPUT2 are any two outputs.
2. For $t_{SK}(b)$ OUTPUT1 and OUTPUT2 are in the same bank.



*Propagation Delay*



*Enable and Disable Times*
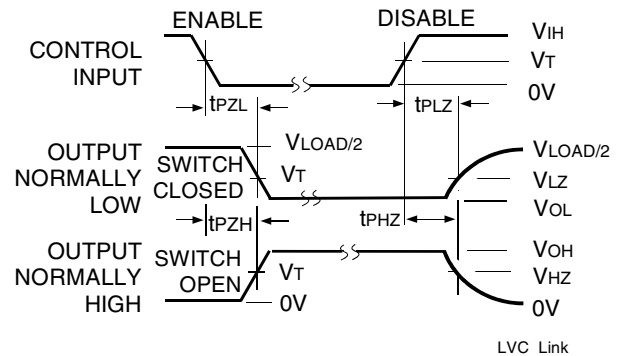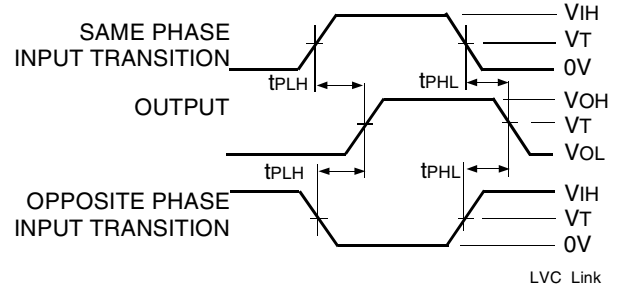
**NOTE:**
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



*Set-up, Hold, and Release Times*



*Pulse Width*

## ORDERING INFORMATION

XX LVC X XX XXXX XX X
Temp. Range  Bus-Hold  Family  Device Type  Package

| | |
|---|---|
| Blank | Tube or Tray |
| 8 | Tape and Reel |
| | |
| PVG | Shrink Small Outline Package - Green |
| PAG | Thin Shrink Small Outline Package - Green |
| | |
| 374A | 16-Bit Edge-Triggered D-Type Flip-Flop with 3-State Outputs |
| | |
| 16 | Double-Density, ±24mA |
| | |
| H | Bus-hold |
| | |
| 74 | -40°C to +85°C |

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