

FEATURES:

- Typical t_{sk(o)} (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- V_{CC} = 3.3V ± 0.3V, Normal Range
- V_{CC} = 2.7V to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- All inputs, outputs, and I/O are 5V tolerant
- Supports hot insertion
- Available in TSSOP package

DRIVE FEATURES:

- High Output Drivers: $\pm 24\text{mA}$
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

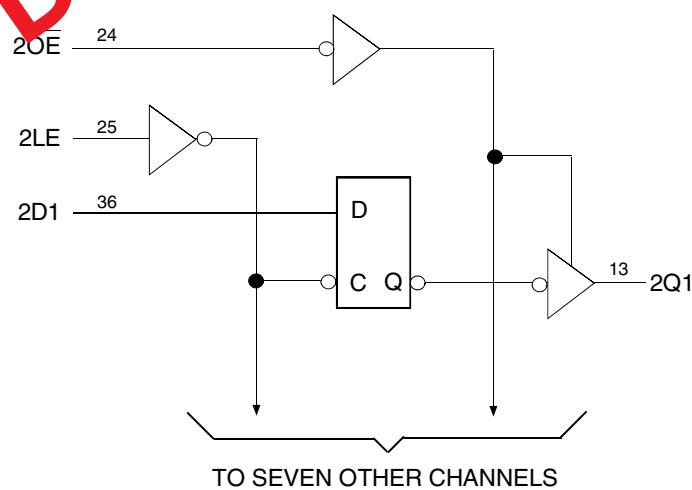
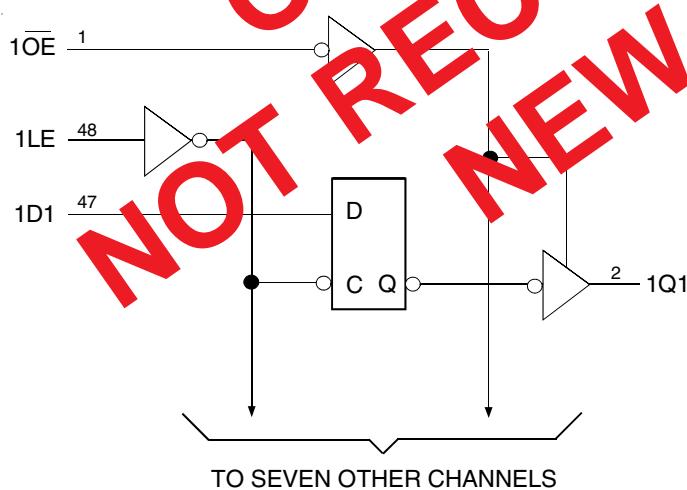
FUNCTIONAL BLOCK DIAGRAM

DESCRIPTION

The LVCH16373A 16-bit transparent D-type latch is built using advanced dual metal CMOS technology. This high-speed, low-power latch is ideal for temporary storage of data. The LVCH16373A can be used for implementing memory address latches, I/O ports, and bus drivers. The Output Enable and Latch Enable controls are organized to operate each device as two 8-bit latches or one 16-bit latch. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

All pins of the LVCH1373A can be driven from either 3.3V or 5V devices. This feature allows the use of the device as a translator in a mixed 3.3V/5V supply system.

The LMCH 6373A has "bus hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.



INDUSTRIAL TEMPERATURE RANGE

MARCH 2006

PIN CONFIGURATION

1 \bar{OE}	1	48	1LE
1Q1	2	47	1D1
1Q2	3	46	1D2
GND	4	45	GND
1Q3	5	44	1D3
1Q4	6	43	1D4
Vcc	7	42	Vcc
1Q5	8	41	1D5
1Q6	9	40	1D6
GND	10	39	GND
1Q7	11	38	1D7
1Q8	12	37	1D8
2Q1	13	36	2D1
2Q2	14	35	2D2
GND	15	34	GND
2Q3	16	33	2D3
2Q4	17	32	2D4
Vcc	18	31	Vcc
2Q5	19	30	2D5
2Q6	20	29	2D6
GND	21	28	GND
2Q7	22	27	2D7
2Q8	23	26	2D8
2 \bar{OE}	24	25	2LE

TSSOP
TOP VIEWABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +6.5	V
TSTG	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-50 to +50	mA
I _{IK}	Continuous Clamp Current, $V_I < 0$ or $V_O < 0$	-50	mA
I _{CC}	Continuous Current through each Vcc or GND	±100	mA
I _{SS}			

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE ($T_A = +25^\circ\text{C}$, $F = 1.0\text{MHz}$)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	4.5	6	pF
C _{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$	6.5	8	pF
C _{I/O}	I/O Port Capacitance	$V_{IN} = 0\text{V}$	6.5	8	pF

NOTE:

1. As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
x _D x	Data Inputs ⁽¹⁾
x _{LE}	Latch Enable Input
x _{OE}	Output Enable Inputs (Active LOW)
x _Q x	3-State Outputs

NOTE:

1. These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLE⁽¹⁾

Inputs		Outputs	
x _D x	x _{LE}	x _{OE}	x _Q x
H	H	L	H
L	H	L	L
X	L	L	Q ⁽²⁾
X	X	H	Z

NOTES:

1. H = HIGH Voltage Level

X = Don't Care

L = LOW Voltage Level

Z = High-Impedance

2. Output level before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $TA = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
VIH	Input HIGH Voltage Level	V _{CC} = 2.3V to 2.7V		1.7	—	—	V
		V _{CC} = 2.7V to 3.6V		2	—	—	
VIL	Input LOW Voltage Level	V _{CC} = 2.3V to 2.7V		—	—	0.7	V
		V _{CC} = 2.7V to 3.6V		—	—	0.8	
I _{IH} I _{IL}	Input Leakage Current	V _{CC} = 3.6V	V _I = 0 to 5.5V	—	—	± 5	μA
I _{OZH} I _{OZL}	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V	V _O = 0 to 5.5V	—	—	± 10	μA
I _{OFF}	Input/Output Power Off Leakage	V _{CC} = 0V, V _{IN} or V _O \leq 5.5V		—	—	± 50	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = -18mA		—	-0.7	-1.2	V
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{CCL} I _{CCH} I _{CCZ}	Quiescent Power Supply Current	V _{CC} = 3.6V	V _{IN} = GND or V _{CC}	—	—	10	μA
			3.6 \leq V _{IN} \leq 5.5V ⁽²⁾	—	—	10	
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V _{CC} - 0.6V, other inputs at V _{CC} or GND		—	—	500	μA

NOTES:

1. Typical values are at V_{CC} = 3.3V, $+25^{\circ}\text{C}$ ambient.
2. This applies in the disabled state only.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
I _{BHH} I _{BHL}	Bus-Hold Input Sustain Current	V _{CC} = 3V	V _I = 2V	-75	—	—	μA
			V _I = 0.8V	75	—	—	
I _{BHH} I _{BHL}	Bus-Hold Input Sustain Current	V _{CC} = 2.3V	V _I = 1.7V	—	—	—	μA
			V _I = 0.7V	—	—	—	
I _{BHHO} I _{BHLO}	Bus-Hold Input Overdrive Current	V _{CC} = 3.6V	V _I = 0 to 3.6V	—	—	± 500	μA

NOTES:

1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, $+25^{\circ}\text{C}$ ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = - 0.1mA	VCC - 0.2	—	V
		VCC = 2.3V	IOH = - 6mA	2	—	
		VCC = 2.3V	IOH = - 12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3V		2.4	—	
		VCC = 3V	IOH = - 24mA	2.2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 6mA	—	0.4	
			IOL = 12mA	—	0.7	
		VCC = 2.7V	IOL = 12mA	—	0.4	
		VCC = 3V	IOL = 24mA	—	0.55	

NOTE:

1. VIH and Vil must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate Vcc range.
TA = - 40°C to + 85°C.

OPERATING CHARACTERISTICS, VCC = 3.3V ± 0.3V, TA = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per Latch Outputs enabled	CL = 0pF, f = 10Mhz	39	pF
	Power Dissipation Capacitance per Latch Outputs disabled		6	

SWITCHING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	Vcc = 2.7V		Vcc = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	
tPLH	Propagation Delay xDx to xQx	—	4.9	1.6	4.2	ns
tPHL	Propagation Delay xLE to xQx	—	5.3	2.1	4.6	ns
tPZH	Output Enable Time xOE to xQx	—	5.7	1.3	4.7	ns
tPLZ	Output Disable Time xOE to xQx	—	6.3	2.5	5.9	ns
tsu	Set-up Time, data before LE↓ HIGH or LOW	1.7	—	1.7	—	ns
tH	Hold Time, data after LE↓ HIGH or LOW	1.2	—	1.2	—	ns
tw	Pulse Width xLE HIGH	3.3	—	3.3	—	ns
tsk(o)	Output Skew ⁽²⁾	—	—	—	500	ps

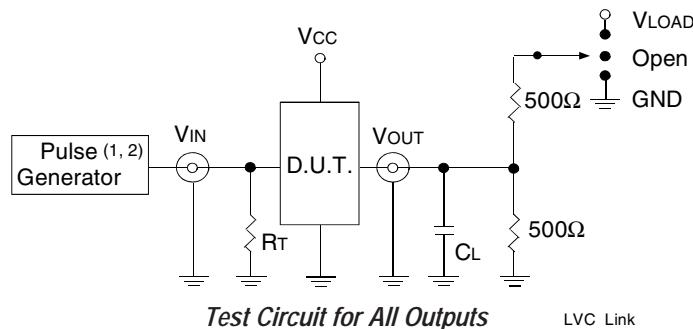
NOTES:

1. See TEST CIRCUITS AND WAVEFORMS. TA = - 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)} = 3.3V \pm 0.3V$	$V_{CC}^{(1)} = 2.7V$	$V_{CC}^{(2)} = 2.5V \pm 0.2V$	Unit
V_{LOAD}	6	6	$2 \times V_{CC}$	V
V_{IH}	2.7	2.7	V_{CC}	V
V_T	1.5	1.5	$V_{CC} / 2$	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF



DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

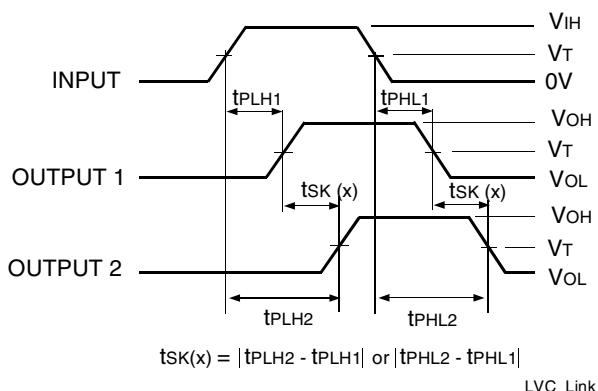
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate $\leq 10\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$.
2. Pulse Generator for All Pulses: Rate $\leq 10\text{MHz}$; $t_f \leq 2\text{ns}$; $t_r \leq 2\text{ns}$.

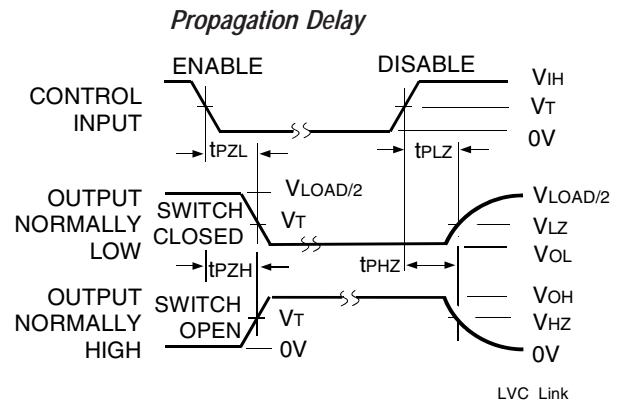
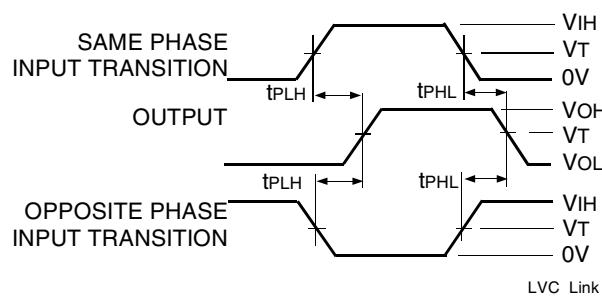
SWITCH POSITION

Test	Switch
Open Drain	
Disable Low	V_{LOAD}
Enable Low	
Disable High	GND
Enable High	
All Other Tests	Open



NOTES:

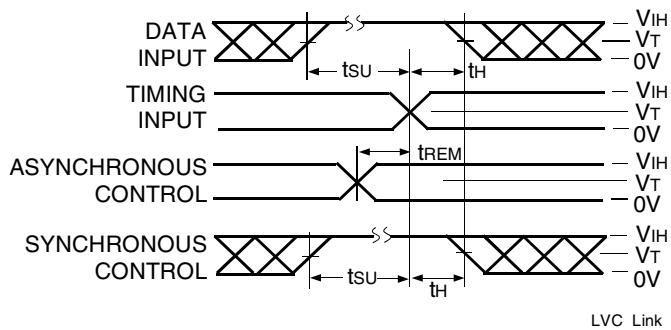
1. For $tsk(o)$ OUTPUT1 and OUTPUT2 are any two outputs.
2. For $tsk(b)$ OUTPUT1 and OUTPUT2 are in the same bank.



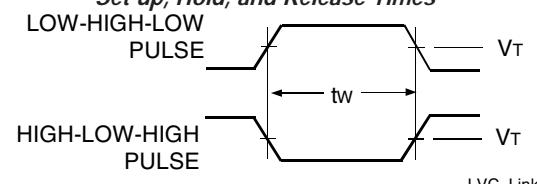
Enable and Disable Times

NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

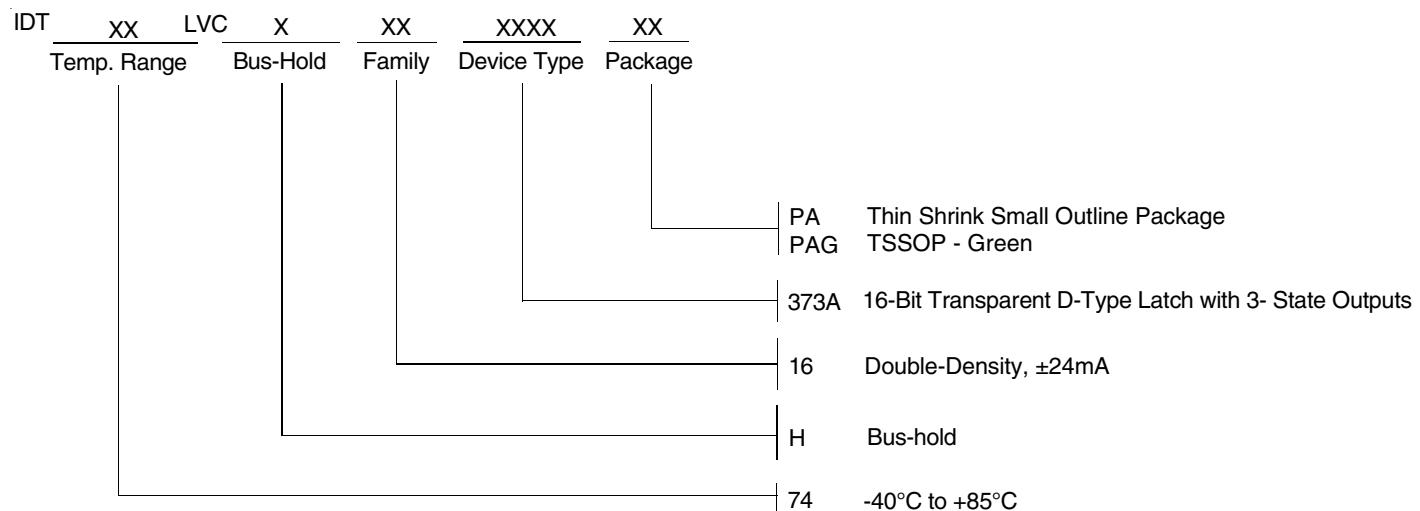


Set-up, Hold, and Release Times



Pulse Width

ORDERING INFORMATION



DATASHEET DOCUMENT HISTORY

07/13/2015 PDN# CQ-14-05 issued. See IDT.com for PDN specifics.
09/06/2019 Datasheet changed to Obsolete Status.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.