

## FEATURES:

- Typical  $t_{sk(o)}$  (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$ , Normal Range
- $V_{CC} = 2.7V$  to  $3.6V$ , Extended Range
- CMOS power levels (0.4μW typ. static)
- All inputs, outputs, and I/O are 5V tolerant
- Supports hot insertion
- Available in SSOP package

## DRIVE FEATURES:

- High Output Drivers:  $\pm 24mA$
- Reduced system switching noise

## APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

## DESCRIPTION:

The LVC16601A 18-bit universal bus transceiver is built using advanced dual metal CMOS technology. This 18-bit universal bus transceiver combines D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes.

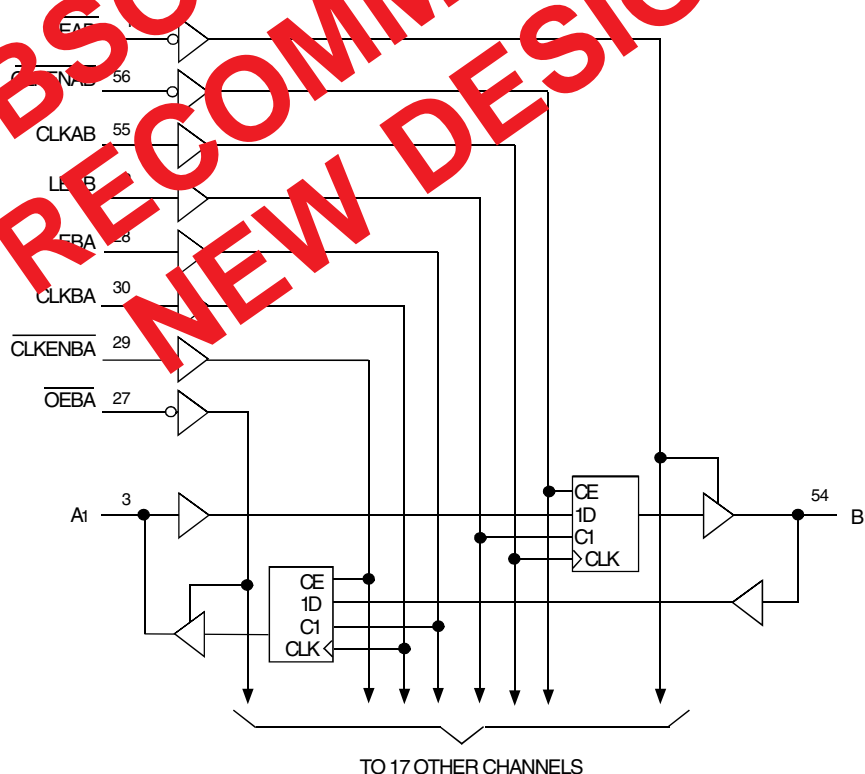
Data flow in each direction is controlled by output-enable ( $\overline{OEAB}$  and  $\overline{OEBA}$ ), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ( $\overline{CLKENAB}$  and  $\overline{CLKENBA}$ ) inputs.

For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched. CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CLKAB. Output enable  $\overline{OEAB}$  is active low. When  $\overline{OEAB}$  is low, the outputs are active. When  $\overline{OEAB}$  is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses  $\overline{OEBA}$ , LEBA, CLKBA and  $\overline{CLKENBA}$ .

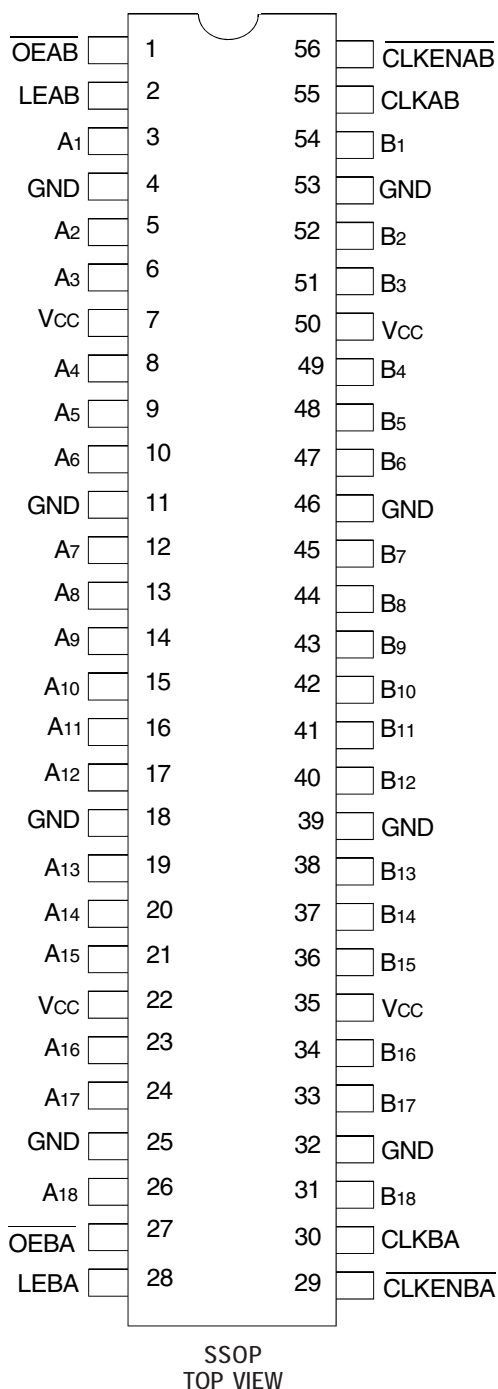
All pins can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVC16601A has been designed with a  $\pm 24mA$  output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +6.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-50 to +50	mA
I <sub>IK</sub> I <sub>OK</sub>	Continuous Clamp Current, V <sub>I</sub> < 0 or V <sub>O</sub> < 0	-50	mA
I <sub>CC</sub> I <sub>SS</sub>	Continuous Current through each V <sub>CC</sub> or GND	±100	mA

### NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## PIN DESCRIPTION

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A <sub>x</sub>	A-to-B Data Inputs or B-to-A 3-State Outputs
B <sub>x</sub>	B-to-A Data Inputs or A-to-B 3-State Outputs
$\overline{CLKENAB}$	A-to-B Clock Enable Input (Active LOW)
$\overline{CLKENBA}$	B-to-A Clock Enable Input (Active LOW)

## FUNCTION TABLE<sup>(1,2)</sup>

Inputs				Outputs	
$\overline{CLKENAB}$	$\overline{OEAB}$	LEAB	CLKAB	A <sub>x</sub>	B <sub>x</sub>
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B <sup>(3)</sup>
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B <sup>(3)</sup>
L	L	L	H	X	B <sup>(4)</sup>

### NOTES:

- H = HIGH Voltage Level  
X = Don't Care  
L = LOW Voltage Level  
Z = High-Impedance  
↑ = LOW-to-HIGH transition
- A-to-B data flow is shown. B-to-A data flow is similar but uses  $\overline{OEBA}$ , LEBA, CLKBA, and  $\overline{CLKENBA}$ .
- Output level before the indicated steady-state input conditions were established.
- Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.

## CAPACITANCE (T<sub>A</sub> = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	6.5	8	pF
C <sub>I/O</sub>	I/O Port Capacitance	V <sub>IN</sub> = 0V	6.5	8	pF

### NOTE:

- As applicable to the device type.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V}$ to $2.7\text{V}$		1.7	—	—	V
		$V_{CC} = 2.7\text{V}$ to $3.6\text{V}$		2	—	—	
$V_{IL}$	Input LOW Voltage Level	$V_{CC} = 2.3\text{V}$ to $2.7\text{V}$		—	—	0.7	V
		$V_{CC} = 2.7\text{V}$ to $3.6\text{V}$		—	—	0.8	
$I_{IH}$ $I_{IL}$	Input Leakage Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to $5.5\text{V}$	—	—	$\pm 5$	$\mu\text{A}$
$I_{OZH}$ $I_{OZL}$	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = 0$ to $5.5\text{V}$	—	—	$\pm 10$	$\mu\text{A}$
$I_{OFF}$	Input/Output Power Off Leakage	$V_{CC} = 0\text{V}$ , $V_{IN}$ or $V_O \leq 5.5\text{V}$		—	—	$\pm 50$	$\mu\text{A}$
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$ , $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
$V_H$	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
$I_{CCL}$ $I_{CCH}$ $I_{CCZ}$	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$	$V_{IN} = \text{GND}$ or $V_{CC}$	—	—	10	$\mu\text{A}$
			$3.6 \leq V_{IN} \leq 5.5\text{V}^{(2)}$	—	—	10	
$\Delta I_{CC}$	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$ , other inputs at $V_{CC}$ or GND		—	—	500	$\mu\text{A}$

### NOTES:

1. Typical values are at  $V_{CC} = 3.3\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
2. This applies in the disabled state only.

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$V_{CC} = 2.3\text{V}$ to $3.6\text{V}$	$I_{OH} = -0.1\text{mA}$	$V_{CC} - 0.2$	—	V
		$V_{CC} = 2.3\text{V}$	$I_{OH} = -6\text{mA}$	2	—	
		$V_{CC} = 2.3\text{V}$	$I_{OH} = -12\text{mA}$	1.7	—	
		$V_{CC} = 2.7\text{V}$		2.2	—	
		$V_{CC} = 3\text{V}$		2.4	—	
		$V_{CC} = 3\text{V}$	$I_{OH} = -24\text{mA}$	2.2	—	
$V_{OL}$	Output LOW Voltage	$V_{CC} = 2.3\text{V}$ to $3.6\text{V}$	$I_{OL} = 0.1\text{mA}$	—	0.2	V
		$V_{CC} = 2.3\text{V}$	$I_{OL} = 6\text{mA}$	—	0.4	
			$I_{OL} = 12\text{mA}$	—	0.7	
		$V_{CC} = 2.7\text{V}$	$I_{OL} = 12\text{mA}$	—	0.4	
		$V_{CC} = 3\text{V}$	$I_{OL} = 24\text{mA}$	—	0.55	

### NOTE:

1.  $V_{IH}$  and  $V_{IL}$  must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate  $V_{CC}$  range.  
 $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

# OPERATING CHARACTERISTICS, $V_{CC} = 3.3V \pm 0.3V$ , $T_A = 25^\circ C$

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per Transceiver Outputs enabled	$C_L = 0pF$ , $f = 10MHz$		pF
CPD	Power Dissipation Capacitance per Transceiver Outputs disabled			

## SWITCHING CHARACTERISTICS<sup>(1)</sup>

Symbol	Parameter	$V_{CC} = 2.7V$		$V_{CC} = 3.3V \pm 0.3V$		Unit
		Min.	Max.	Min.	Max.	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Ax to Bx or Bx to Ax	—	5.4	—	4.6	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay LEBA to Ax, LEAB to Bx	—	6.2	—	5.2	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay CLKBA to Ax, CLKAB to Bx	—	6.3	—	5.3	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time $\overline{OEBA}$ to Ax, $\overline{OEAB}$ to Bx	—	6.8	—	5.6	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $\overline{OEBA}$ to Ax, $\overline{OEAB}$ to Bx	—	6	—	5.2	ns
$t_{SU}$	Set-up Time HIGH or LOW, Ax to CLKAB, Bx to CLKBA	1.5	—	1.5	—	ns
$t_H$	Hold Time HIGH or LOW, Ax to CLKAB, Bx to CLKBA	0.8	—	0.8	—	ns
$t_{SU}$	Set-up Time HIGH or LOW Ax to LEAB, Bx to LEBA	Clock LOW	1	—	1	ns
		Clock HIGH	1	—	1	
$t_{SU}$	Set-up Time, $\overline{CLKENAB}$ to CLKAB	2.1	—	2.1	—	ns
$t_{SU}$	Set-up Time, $\overline{CLKENBA}$ to CLKBA	2.1	—	2.1	—	ns
$t_H$	Hold Time HIGH or LOW, Ax after LEAB, Bx after LEBA	1.8	—	1.8	—	ns
$t_H$	Hold Time, $\overline{CLKENAB}$ after CLKAB	0.5	—	0.5	—	ns
$t_H$	Hold Time, $\overline{CLKENBA}$ after CLKBA	0.5	—	0.5	—	ns
$t_W$	LEAB or LEBA Pulse Width HIGH	3	—	3	—	ns
$t_W$	CLKAB or CLKBA Pulse Width HIGH or LOW	3	—	3	—	ns
$t_{SK(O)}$	Output Skew <sup>(2)</sup>	—	—	—	500	ps

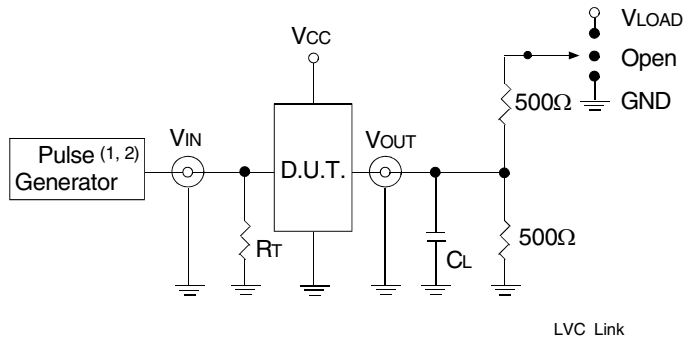
### NOTES:

- See TEST CIRCUITS AND WAVEFORMS.  $T_A = -40^\circ C$  to  $+85^\circ C$ .
- Skew between any two outputs of the same package and switching in the same direction.

## TEST CIRCUITS AND WAVEFORMS

### TEST CONDITIONS

Symbol	$V_{CC}^{(1)} = 3.3V \pm 0.3V$	$V_{CC}^{(1)} = 2.7V$	$V_{CC}^{(2)} = 2.5V \pm 0.2V$	Unit
$V_{LOAD}$	6	6	$2 \times V_{CC}$	V
$V_{IH}$	2.7	2.7	$V_{CC}$	V
$V_T$	1.5	1.5	$V_{CC} / 2$	V
$V_{LZ}$	300	300	150	mV
$V_{HZ}$	300	300	150	mV
$C_L$	50	50	30	pF



Test Circuit for All Outputs

#### DEFINITIONS:

$C_L$  = Load capacitance: includes jig and probe capacitance.

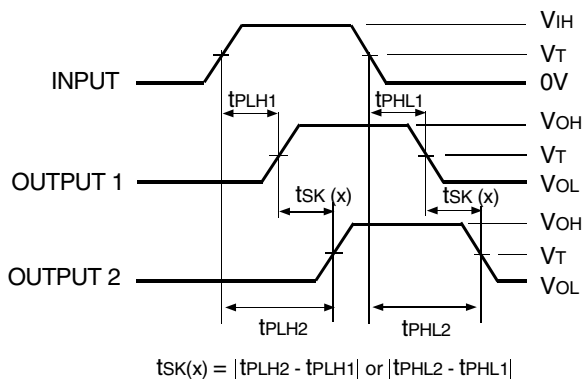
$R_T$  = Termination resistance: should be equal to  $Z_{OUT}$  of the Pulse Generator.

#### NOTES:

1. Pulse Generator for All Pulses: Rate  $\leq 10\text{MHz}$ ;  $t_r \leq 2.5\text{ns}$ ;  $t_f \leq 2.5\text{ns}$ .
2. Pulse Generator for All Pulses: Rate  $\leq 10\text{MHz}$ ;  $t_r \leq 2\text{ns}$ ;  $t_f \leq 2\text{ns}$ .

### SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	$V_{LOAD}$
Disable High Enable High	GND
All Other Tests	Open

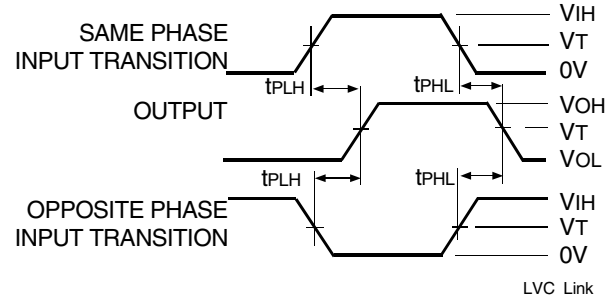


$$tsK(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

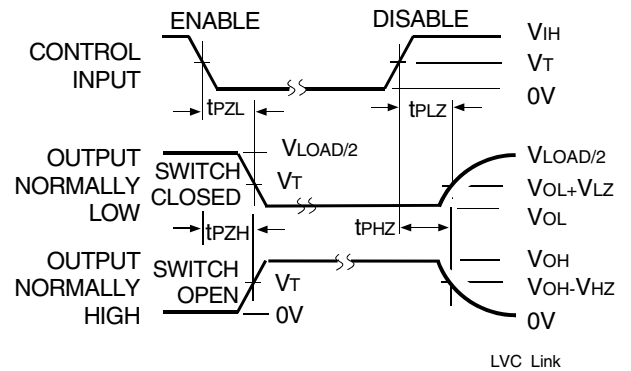
Output Skew -  $tsK(x)$

#### NOTES:

1. For  $tsK(o)$  OUTPUT1 and OUTPUT2 are any two outputs.
2. For  $tsK(b)$  OUTPUT1 and OUTPUT2 are in the same bank.



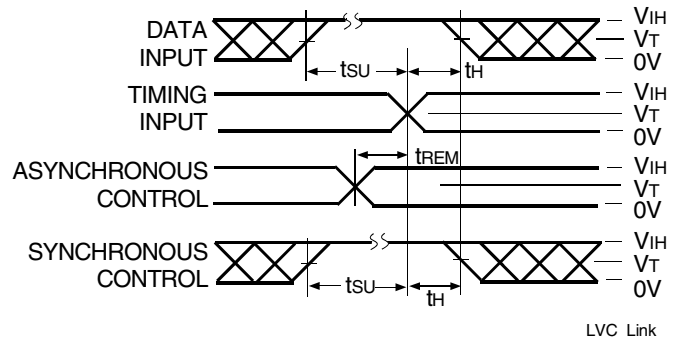
Propagation Delay



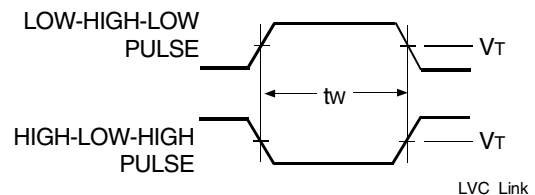
Enable and Disable Times

#### NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



Set-up, Hold, and Release Times



Pulse Width

## ORDERING INFORMATION

XX	LVC	X	XX	XXXX	XX	X		
Temp. Range	Bus-Hold	Family	Device Type	Package				
							Blank 8	Tube or Tray Tape and Reel
							PVG	Shrink Small Outline Package - Green
							601A	18-Bit Universal Bus Transceiver
							16	Double-Density, $\pm 24\text{mA}$
							Blank	No Bus-hold
							74	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

## DATASHEET DOCUMENT HISTORY

07/28/2015	Pg. 6	Updated the ordering information by removing non RoHS parts and adding Tape and Reel information.
07/31/2015	Pg. 1-6	PDN# CQ-14-05 issued. See IDT.com for PDN specifics.
09/09/2015	Pg. 1-6	Datasheet changed to Obsolete Status.

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.