

FEATURES:

- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model ($C = 200\text{pF}$, $R = 0$)
- $V_{cc} = 3.3V \pm 0.3V$, Normal Range
- $V_{cc} = 2.7V$ to $3.6V$, Extended Range
- CMOS power levels ($0.4\mu\text{W}$ typ. static)
- All inputs, outputs, and I/O are 5V tolerant
- Supports hot insertion
- Available in SSOP package

DRIVE FEATURES:

- High Output Drivers: $\pm 24\text{mA}$
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

DESCRIPTION:

The LVC16601A 18-bit universal bus transceiver is built using advanced dual metal CMOS technology. This 18-bit universal bus transceiver combines D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes.

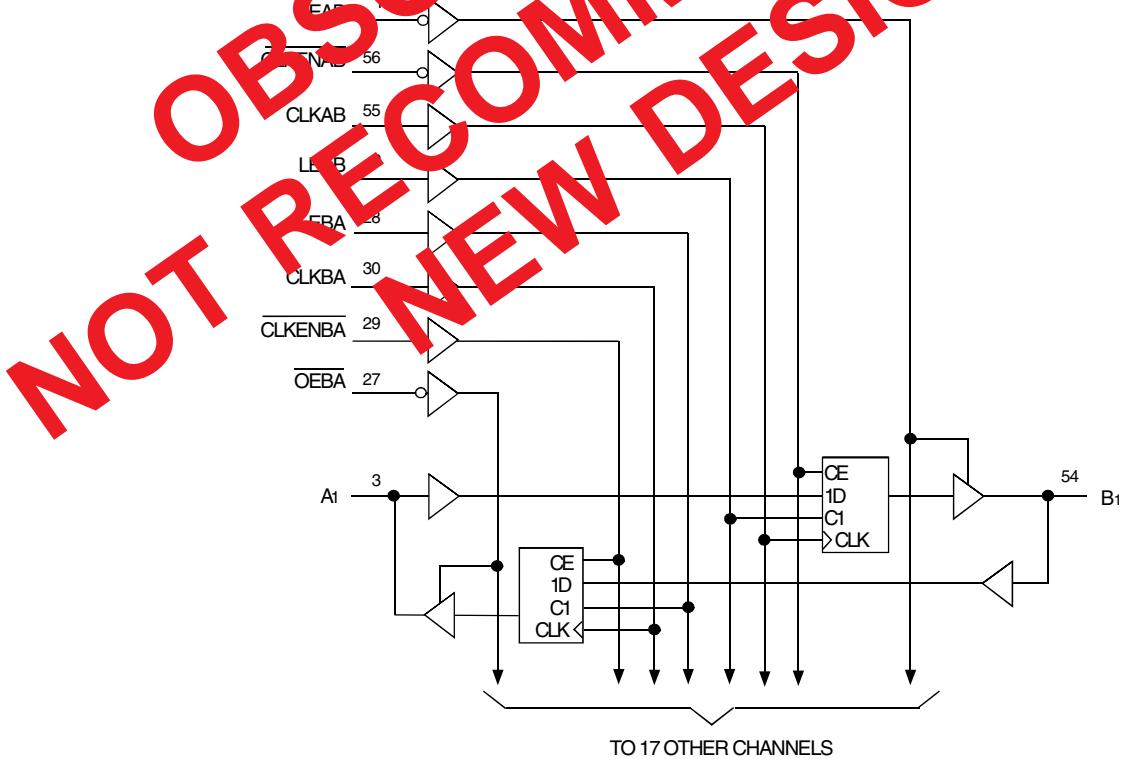
Data flow in each direction is controlled by output-enable (\overline{OEAB} and \overline{OEB}), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable (CLKENAB and CLKENBA) inputs.

For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched. CLKAB is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the LEAB \rightarrow HIGH transition. CLKAB output enable \overline{OEAB} is active low. When CLKAB is low, the outputs are active. When \overline{OEAB} is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses \overline{OEB} , LEBA, CLKBA and CLKENBA.

All pins can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVC16601A has been designed with a $\pm 24\text{mA}$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

OEAB	1	56	CLKENAB
LEAB	2	55	CLKAB
A ₁	3	54	B ₁
GND	4	53	GND
A ₂	5	52	B ₂
A ₃	6	51	B ₃
V _{CC}	7	50	V _{CC}
A ₄	8	49	B ₄
A ₅	9	48	B ₅
A ₆	10	47	B ₆
GND	11	46	GND
A ₇	12	45	B ₇
A ₈	13	44	B ₈
A ₉	14	43	B ₉
A ₁₀	15	42	B ₁₀
A ₁₁	16	41	B ₁₁
A ₁₂	17	40	B ₁₂
GND	18	39	GND
A ₁₃	19	38	B ₁₃
A ₁₄	20	37	B ₁₄
A ₁₅	21	36	B ₁₅
V _{CC}	22	35	V _{CC}
A ₁₆	23	34	B ₁₆
A ₁₇	24	33	B ₁₇
GND	25	32	GND
A ₁₈	26	31	B ₁₈
OEBA	27	30	CLKBA
LEBA	28	29	CLKENBA

SSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to +6.5	V
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-50 to +50	mA
I _{IK}	Continuous Clamp Current, V _I < 0 or V _O < 0	-50	mA
I _{OK}			
I _{CC}	Continuous Current through each V _{CC} or GND	±100	mA
I _{SS}			

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PIN DESCRIPTION

Pin Names	Description
OEAB	A-to-B Output Enable Input (Active LOW)
OEBA	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A _x	A-to-B Data Inputs or B-to-A 3-State Outputs
B _x	B-to-A Data Inputs or A-to-B 3-State Outputs
CLKENAB	A-to-B Clock Enable Input (Active LOW)
CLKENBA	B-to-A Clock Enable Input (Active LOW)

FUNCTION TABLE^(1,2)

Inputs					Outputs
CLKENAB	OEAB	LEAB	CLKAB	A _x	B _x
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B ⁽³⁾
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B ⁽³⁾
L	L	L	H	X	B ⁽⁴⁾

NOTES:

1. H = HIGH Voltage Level
X = Don't Care
L = LOW Voltage Level
Z = High-Impedance
↑ = LOW-to-HIGH transition
2. A-to-B data flow is shown. B-to-A data flow is similar but uses OEBA, LEBA, CLKBA, and CLKENBA.
3. Output level before the indicated steady-state input conditions were established.
4. Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	6.5	8	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	6.5	8	pF

NOTE:

1. As applicable to the device type.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
VIH	Input HIGH Voltage Level	Vcc = 2.3V to 2.7V		1.7	—	—	V
		Vcc = 2.7V to 3.6V		2	—	—	
VIL	Input LOW Voltage Level	Vcc = 2.3V to 2.7V		—	—	0.7	V
		Vcc = 2.7V to 3.6V		—	—	0.8	
I _{IH} I _{IL}	Input Leakage Current	Vcc = 3.6V	V _I = 0 to 5.5V	—	—	± 5	μA
I _{OZH} I _{OZL}	High Impedance Output Current (3-State Output pins)	Vcc = 3.6V	V _O = 0 to 5.5V	—	—	± 10	μA
I _{OFF}	Input/Output Power Off Leakage	Vcc = 0V, V _{IN} or V _O \leq 5.5V		—	—	± 50	μA
V _{IK}	Clamp Diode Voltage	Vcc = 2.3V, I _{IN} = -18mA		—	-0.7	-1.2	V
V _H	Input Hysteresis	Vcc = 3.3V		—	100	—	mV
I _{CCL} I _{CCH} I _{CCZ}	Quiescent Power Supply Current	Vcc = 3.6V	V _{IN} = GND or Vcc	—	—	10	μA
			3.6 \leq V _{IN} \leq 5.5V ⁽²⁾	—	—	10	
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at Vcc - 0.6V, other inputs at Vcc or GND		—	—	500	μA

NOTES:

1. Typical values are at Vcc = 3.3V, $+25^\circ\text{C}$ ambient.
2. This applies in the disabled state only.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	Vcc = 2.3V to 3.6V	I _{OH} = -0.1mA	Vcc - 0.2	—	V
		Vcc = 2.3V	I _{OH} = -6mA	2	—	
		Vcc = 2.3V	I _{OH} = -12mA	1.7	—	
		Vcc = 2.7V		2.2	—	
		Vcc = 3V		2.4	—	
		Vcc = 3V	I _{OH} = -24mA	2.2	—	
V _{OL}	Output LOW Voltage	Vcc = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		Vcc = 2.3V	I _{OL} = 6mA	—	0.4	
			I _{OL} = 12mA	—	0.7	
		Vcc = 2.7V	I _{OL} = 12mA	—	0.4	
		Vcc = 3V	I _{OL} = 24mA	—	0.55	

NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate Vcc range. $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

OPERATING CHARACTERISTICS, $V_{CC} = 3.3V \pm 0.3V$, $T_A = 25^\circ C$

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per Transceiver Outputs enabled	$CL = 0pF, f = 10Mhz$		pF
CPD	Power Dissipation Capacitance per Transceiver Outputs disabled			

SWITCHING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	$V_{CC} = 2.7V$		$V_{CC} = 3.3V \pm 0.3V$		Unit
		Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay Ax to Bx or Bx to Ax	—	5.4	—	4.6	ns
t_{PLH}	Propagation Delay LEBA to Ax, LEAB to Bx	—	6.2	—	5.2	ns
t_{PLH}	Propagation Delay CLKBA to Ax, CLKAB to Bx	—	6.3	—	5.3	ns
t_{PZH}	Output Enable Time \overline{OEBA} to Ax, \overline{OEAB} to Bx	—	6.8	—	5.6	ns
t_{PHZ}	Output Disable Time \overline{OEBA} to Ax, \overline{OEAB} to Bx	—	6	—	5.2	ns
t_{SU}	Set-up Time HIGH or LOW, Ax to CLKAB, Bx to CLKBA	1.5	—	1.5	—	ns
t_H	Hold Time HIGH or LOW, Ax to CLKAB, Bx to CLKBA	0.8	—	0.8	—	ns
t_{SU}	Set-up Time HIGH or LOW Ax to LEAB, Bx to LEBA	Clock LOW	1	—	1	ns
		Clock HIGH	1	—	1	
t_{SU}	Set-up Time, $\overline{CLKENAB}$ to CLKAB	2.1	—	2.1	—	ns
t_{SU}	Set-up Time, $\overline{CLKENBA}$ to CLKBA	2.1	—	2.1	—	ns
t_H	Hold Time HIGH or LOW, Ax after LEAB, Bx after LEBA	1.8	—	1.8	—	ns
t_H	Hold Time, $\overline{CLKENAB}$ after CLKAB	0.5	—	0.5	—	ns
t_H	Hold Time, $\overline{CLKENBA}$ after CLKBA	0.5	—	0.5	—	ns
t_W	LEAB or LEBA Pulse Width HIGH	3	—	3	—	ns
t_W	CLKAB or CLKBA Pulse Width HIGH or LOW	3	—	3	—	ns
$t_{SK(o)}$	Output Skew ⁽²⁾	—	—	—	500	ps

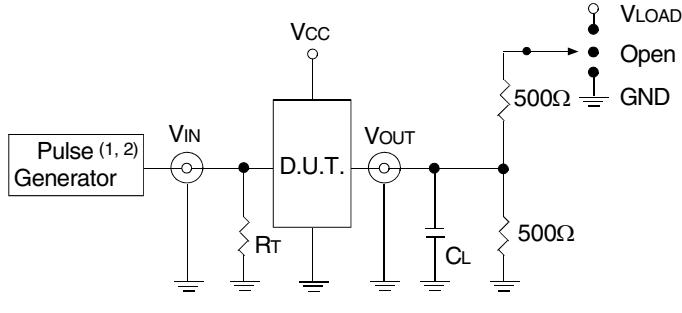
NOTES:

1. See TEST CIRCUITS AND WAVEFORMS. $T_A = -40^\circ C$ to $+85^\circ C$.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)} = 3.3V \pm 0.3V$	$V_{CC}^{(1)} = 2.7V$	$V_{CC}^{(2)} = 2.5V \pm 0.2V$	Unit
V_{LOAD}	6	6	$2 \times V_{CC}$	V
V_{IH}	2.7	2.7	V_{CC}	V
V_T	1.5	1.5	$V_{CC} / 2$	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF



Test Circuit for All Outputs

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

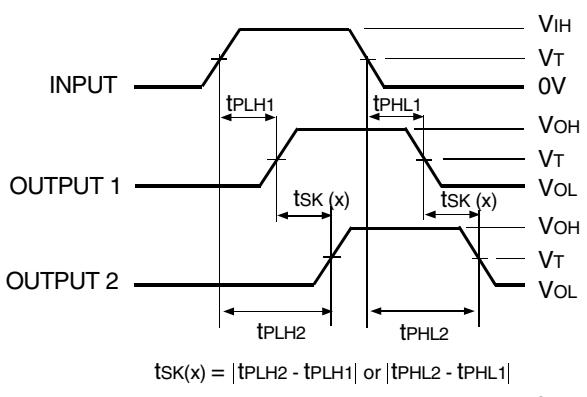
R_T = Termination resistance; should be equal to Z_{OUT} of the Pulse Generator

NOTES:

NOTES:
1. Pulse Generator for All Pulses: Rate \leq 10MHz; $t_f \leq 2.5\text{ns}$; $t_R \leq 2.5\text{ns}$.
2. Pulse Generator for All Pulses: Rate \leq 10MHz; $t_f \leq 2\text{ns}$; $t_R \leq 2\text{ns}$.

SWITCH POSITION

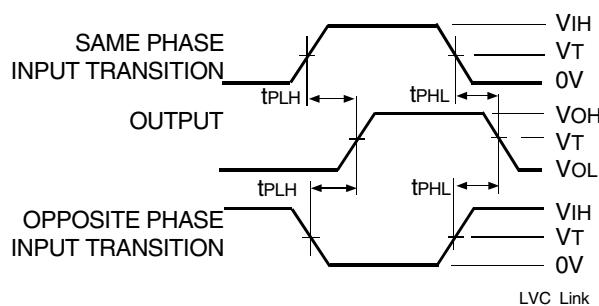
Test	Switch
Open Drain	
Disable Low	V_{LOAD}
Enable Low	
Disable High	GND
Enable High	
All Other Tests	Open



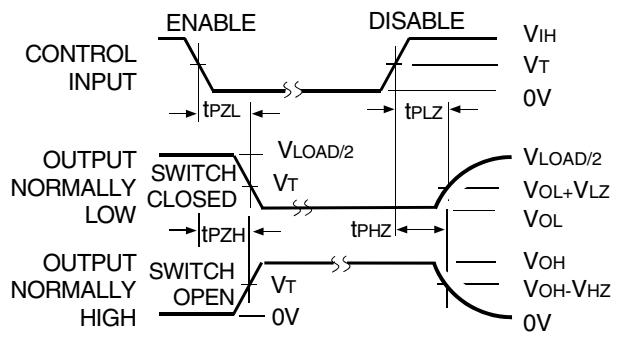
Output Skew - $tsk(x)$

NOTES:

1. For tsk(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.



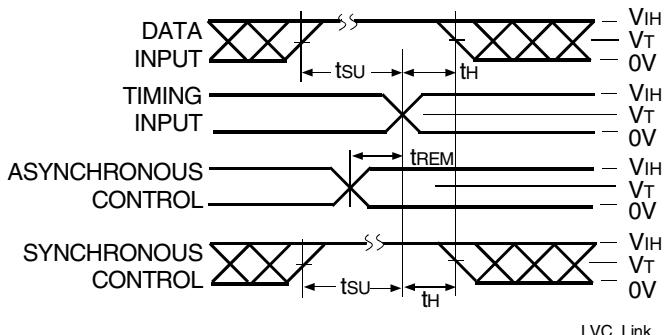
Propagation Delay



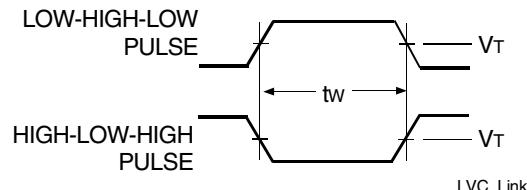
Enable and Disable Times

NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

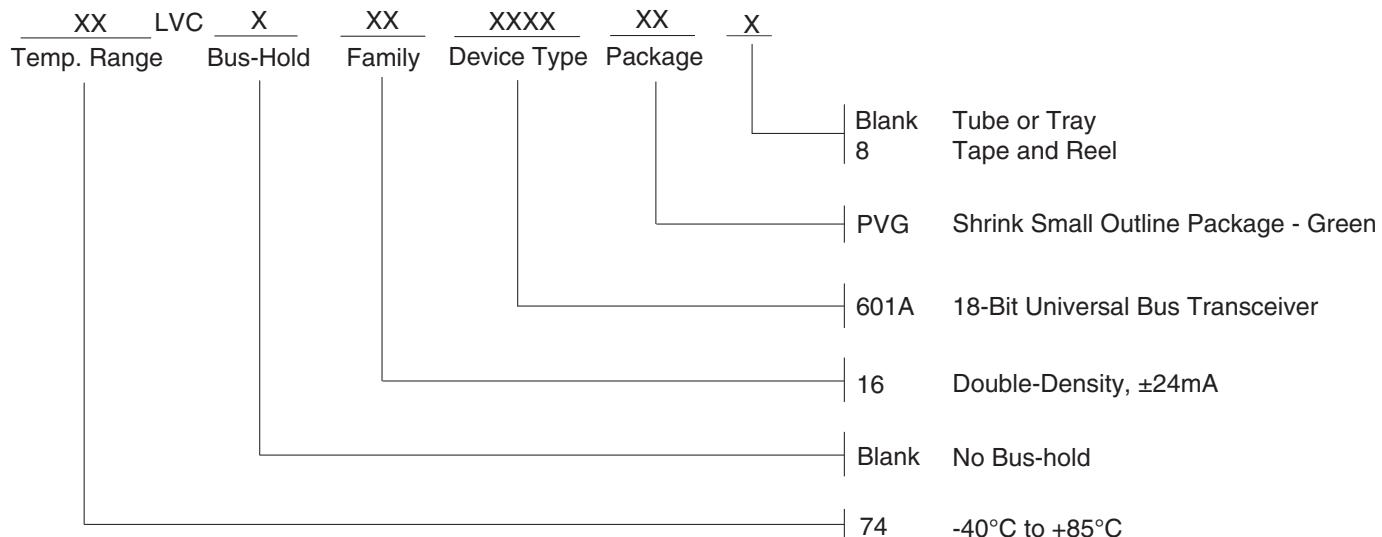


Set-up, Hold, and Release Times



Pulse Width

ORDERING INFORMATION



DATASHEET DOCUMENT HISTORY

07/28/2015	Pg. 6	Updated the ordering information by removing non RoHS parts and adding Tape and Reel information.
07/31/2015	Pg. 1-6	PDN# CQ-14-05 issued. See IDT.com for PDN specifics.
09/09/2015	Pg. 1-6	Datasheet changed to Obsolete Status.

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