

FEATURES:

- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model ($C = 200\text{pF}$, $R = 0$)
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to $3.6V$, Extended Range
- CMOS power levels ($0.4\mu\text{W}$ typ. static)
- All inputs, outputs, and I/O are 5V tolerant
- Supports hot insertion
- Available in SSOP and TSSOP packages

DRIVE FEATURES:

- High Output Drivers: $\pm 24\text{mA}$
- Reduced system switching noise

APPLICATIONS:

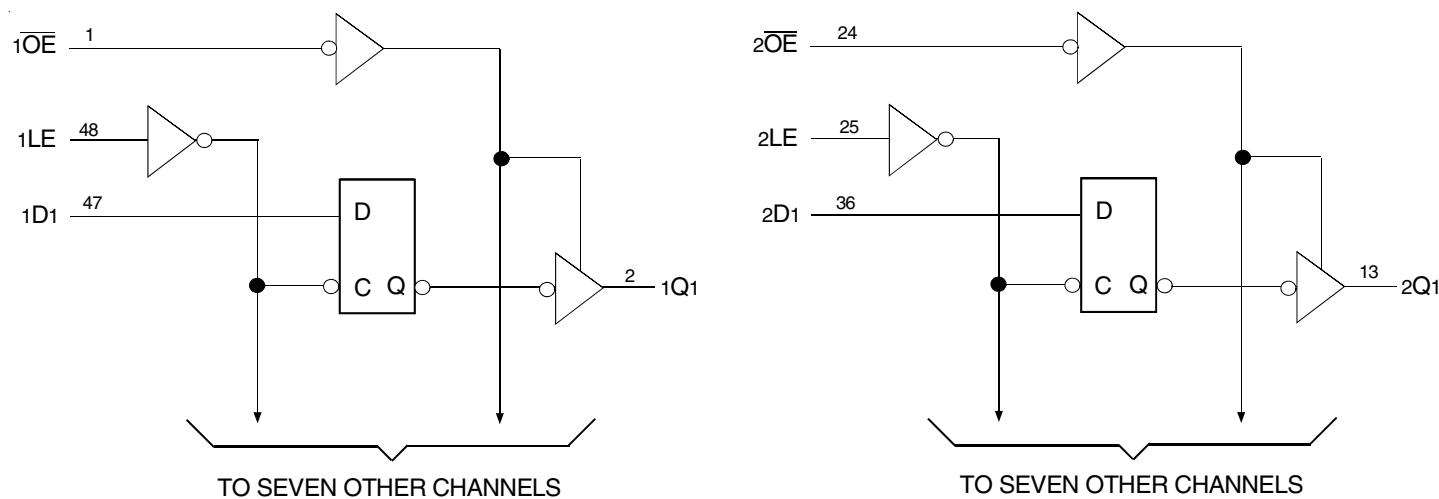
- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

DESCRIPTION:

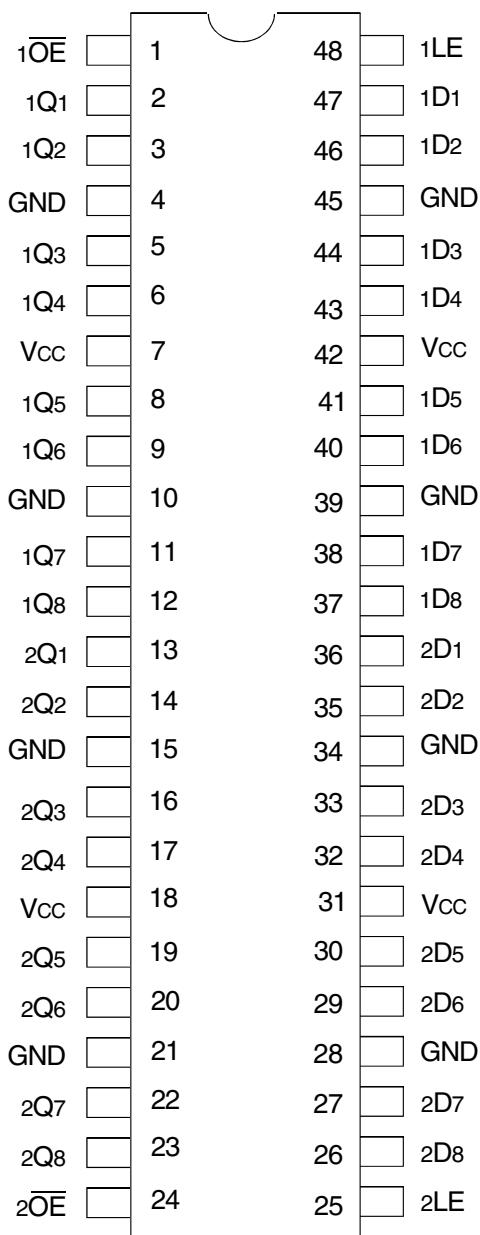
The LVC16373A 16-bit transparent D-type latch is built using advanced dual metal CMOS technology. This high-speed, low-power latch is ideal for temporary storage of data. The LVC16373A can be used for implementing memory address latches, I/O ports, and bus drivers. The Output Enable and Latch Enable controls are organized to operate each device as two 8-bit latches or one 16-bit latch. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

All pins of the LVC16373A can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVC16373A has been designed with a $\pm 24\text{mA}$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

FUNCTIONAL BLOCK DIAGRAM

PIN CONFIGURATION



SSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +6.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-50 to +50	mA
I _{IK}	Continuous Clamp Current, V _I < 0 or V _O < 0	-50	mA
I _{OK}			
I _{CC}	Continuous Current through each V _{CC} or GND	±100	mA
I _{SS}			

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	6.5	8	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	6.5	8	pF

NOTE:

1. As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
x _D	Data Inputs
x _{LE}	Latch Enable Input (Active HIGH)
x _{OE}	Output Enable Inputs (Active LOW)
x _Q	3-State Outputs

FUNCTION TABLE⁽¹⁾

Inputs			Outputs
x _D	x _{LE}	x _{OE}	x _Q
H	H	L	H
L	H	L	L
X	L	L	Q ⁽²⁾
X	X	H	Z

NOTES:

1. H = HIGH Voltage Level

X = Don't Care

L = LOW Voltage Level

Z = High-Impedance

2. Output level before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $TA = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
VIH	Input HIGH Voltage Level	Vcc = 2.3V to 2.7V		1.7	—	—	V
		Vcc = 2.7V to 3.6V		2	—	—	
VIL	Input LOW Voltage Level	Vcc = 2.3V to 2.7V		—	—	0.7	V
		Vcc = 2.7V to 3.6V		—	—	0.8	
IIH IIL	Input Leakage Current	Vcc = 3.6V	VI = 0 to 5.5V	—	—	± 5	μA
IOZH IOZL	High Impedance Output Current (3-State Output pins)	Vcc = 3.6V	VO = 0 to 5.5V	—	—	± 10	μA
IOFF	Input/Output Power Off Leakage	Vcc = 0V, VIN or VO \leq 5.5V		—	—	± 50	μA
VIK	Clamp Diode Voltage	Vcc = 2.3V, IIN = -18mA		—	-0.7	-1.2	V
VH	Input Hysteresis	Vcc = 3.3V		—	100	—	mV
IcCL IcCH IcCZ	Quiescent Power Supply Current	Vcc = 3.6V		—	—	10	μA
		VIN = GND or Vcc $3.6 \leq VIN \leq 5.5\text{V}^{(2)}$		—	—	10	
ΔIcc	Quiescent Power Supply Current Variation	One input at Vcc - 0.6V, other inputs at Vcc or GND		—	—	500	μA

NOTES:

1. Typical values are at Vcc = 3.3V, $+25^{\circ}\text{C}$ ambient.

2. This applies in the disabled state only.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	Vcc = 2.3V to 3.6V	I _{OH} = -0.1mA	Vcc - 0.2	—	V
		Vcc = 2.3V	I _{OH} = -6mA	2	—	
		Vcc = 2.3V	I _{OH} = -12mA	1.7	—	
		Vcc = 2.7V		2.2	—	
		Vcc = 3V	I _{OH} = -24mA	2.4	—	
		Vcc = 3V		2.2	—	
VOL	Output LOW Voltage	Vcc = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		Vcc = 2.3V	I _{OL} = 6mA	—	0.4	
			I _{OL} = 12mA	—	0.7	
		Vcc = 2.7V	I _{OL} = 12mA	—	0.4	
		Vcc = 3V	I _{OL} = 24mA	—	0.55	

NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate Vcc range.
 $TA = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$.

OPERATING CHARACTERISTICS, $V_{CC} = 3.3V \pm 0.3V$, $T_A = 25^\circ C$

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per Latch Outputs enabled	$CL = 0pF, f = 10MHz$	39	pF
CPD	Power Dissipation Capacitance per Latch Outputs disabled		6	

SWITCHING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	$V_{CC} = 2.7V$		$V_{CC} = 3.3V \pm 0.3V$		Unit
		Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay x_{Dx} to x_{Qx}	—	4.9	1.6	4.2	ns
t_{PHL}	Propagation Delay x_{LE} to x_{Qx}	—	5.3	2.1	4.6	ns
t_{PZH}	Output Enable Time $x_{\overline{OE}}$ to x_{Qx}	—	5.7	1.3	4.7	ns
t_{PLZ}	Output Disable Time $x_{\overline{OE}}$ to x_{Qx}	—	6.3	2.5	5.9	ns
t_{SU}	Set-up Time, data before $LE \downarrow$ HIGH or LOW	1.7	—	1.7	—	ns
t_H	Hold Time, data after $LE \downarrow$ HIGH or LOW	1.2	—	1.2	—	ns
t_W	Pulse Width LE HIGH	3.3	—	3.3	—	ns
$t_{SK(o)}$	Output Skew ⁽²⁾	—	—	—	500	ps

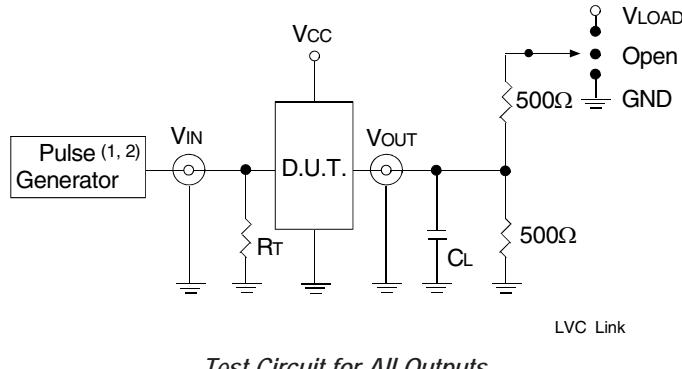
NOTES:

1. See TEST CIRCUITS AND WAVEFORMS. $T_A = -40^\circ C$ to $+85^\circ C$.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)} = 3.3V \pm 0.3V$	$V_{CC}^{(1)} = 2.7V$	$V_{CC}^{(2)} = 2.5V \pm 0.2V$	Unit
V_{LOAD}	6	6	$2 \times V_{CC}$	V
V_{IH}	2.7	2.7	V_{CC}	V
V_T	1.5	1.5	$V_{CC} / 2$	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF



DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

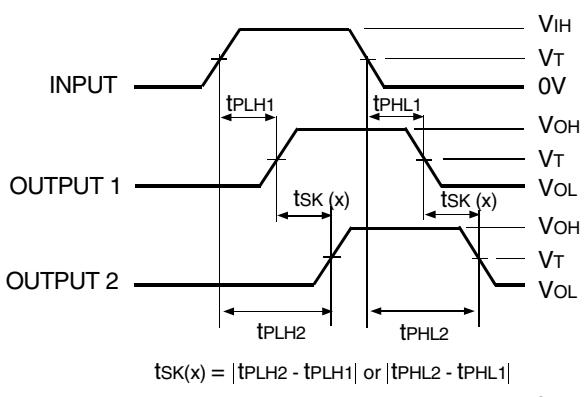
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate $\leq 10MHz$; $t_f \leq 2.5ns$; $t_r \leq 2.5ns$.
2. Pulse Generator for All Pulses: Rate $\leq 10MHz$; $t_f \leq 2ns$; $t_r \leq 2ns$.

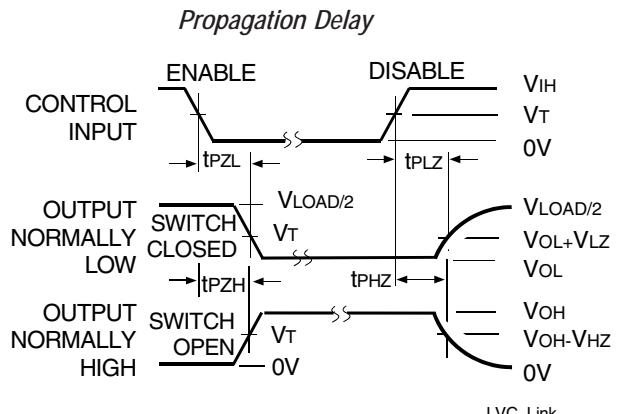
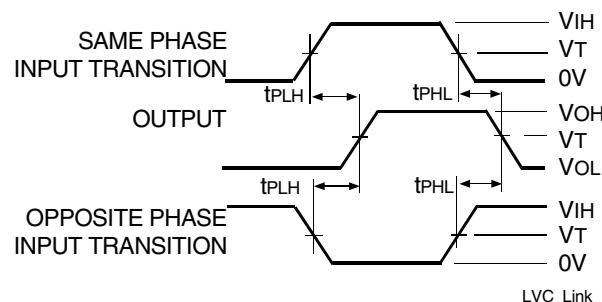
SWITCH POSITION

Test	Switch
Open Drain	
Disable Low	V_{LOAD}
Enable Low	
Disable High	GND
Enable High	
All Other Tests	Open



NOTES:

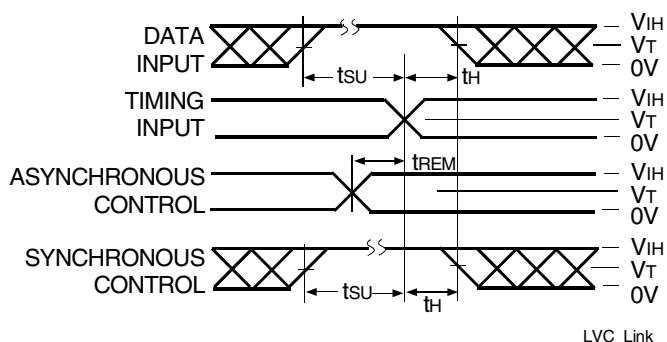
1. For $tsk(o)$ OUTPUT1 and OUTPUT2 are any two outputs.
2. For $tsk(b)$ OUTPUT1 and OUTPUT2 are in the same bank.



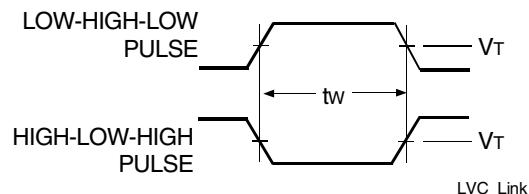
Enable and Disable Times

NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

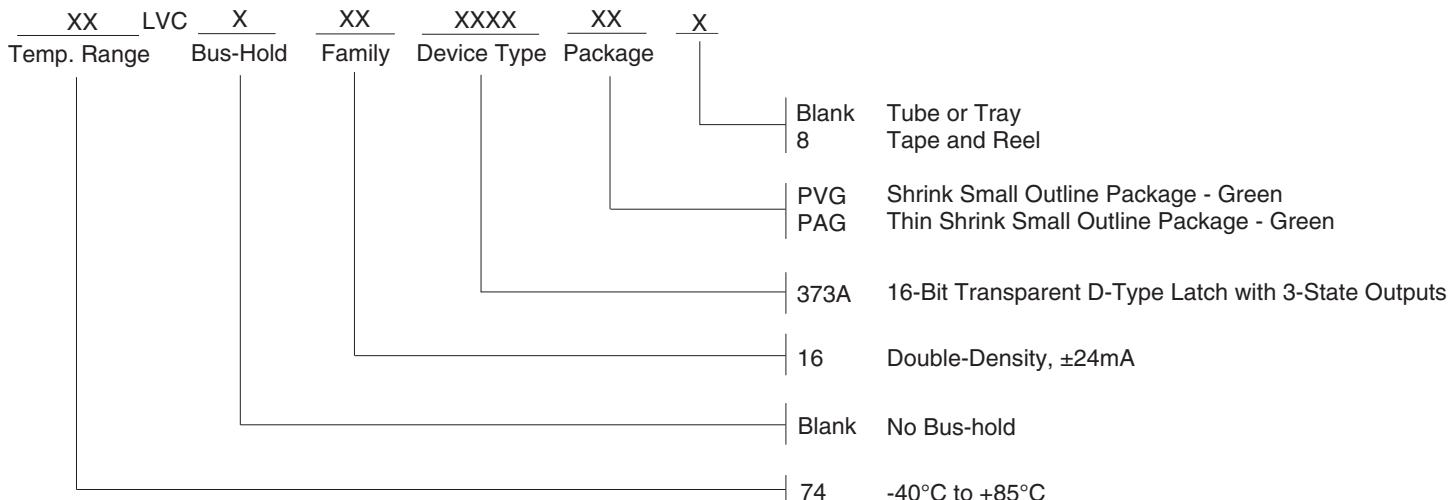


Set-up, Hold, and Release Times



Pulse Width

ORDERING INFORMATION



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