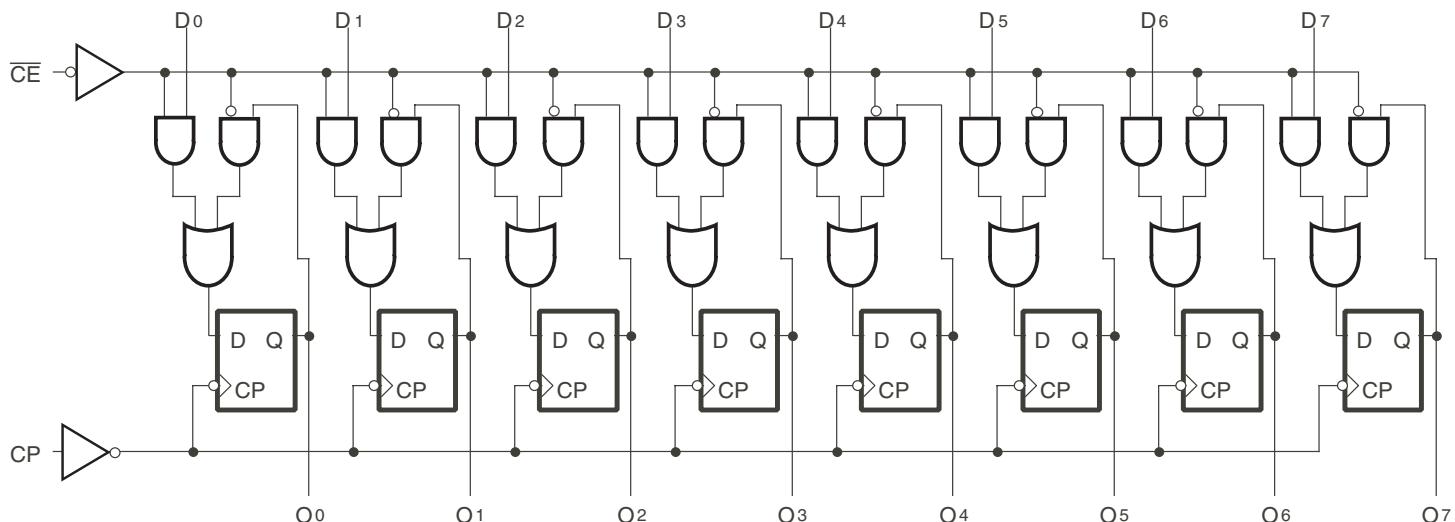


FEATURES:

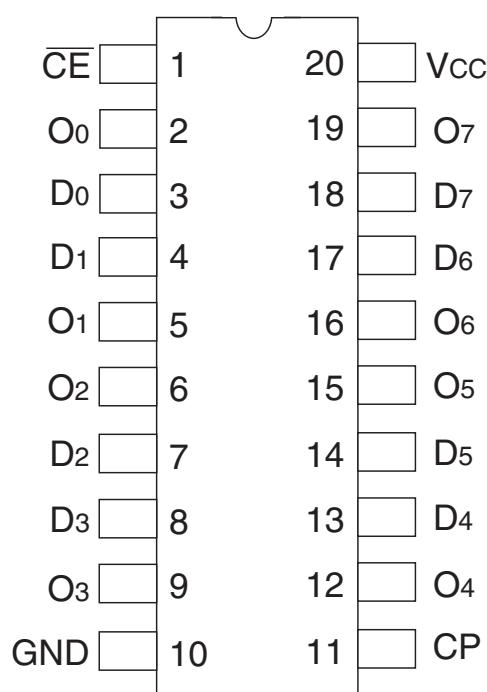
- A, C, and D grades
- Low input and output leakage $\leq 1\mu\text{A}$ (max.)
- CMOS power levels
- True TTL input and output compatibility:
 - $V_{OH} = 3.3\text{V}$ (typ.)
 - $V_{OL} = 0.3\text{V}$ (typ.)
- High Drive outputs (-15mA I_{OH} , 48mA I_{OL})
- Meets or exceeds JEDEC standard 18 specifications
- Power off disable outputs permit "live insertion"
- Available in SOIC and QSOP packages

DESCRIPTION:

The IDT74FCT377T is an octal D flip-flop built using an advanced dual metal CMOS technology. The IDT74FCT377T has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Clock Enable (\overline{CE}) is low. The register is fully edge-triggered. The state of each D input, one set-up time before the low-to-high clock transition, is transferred to the corresponding flip-flop's Q output. The \overline{CE} input must be stable only one set-up time prior to the low-to-high transition for predictable operation.

FUNCTIONAL BLOCK DIAGRAM

PIN CONFIGURATION



SOIC/ QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-60 to +120	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Output and I/O terminals only.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
Do – D7	Data Inputs
CE	Clock Enable (Active LOW)
O0 – O7	Data Outputs
CP	Clock Pulse Input

FUNCTION TABLE⁽¹⁾

Operating Mode	Inputs			Outputs
	CP	CE	D	
Load "1"	↑	I	h	H
Load "0"	↑	I	I	L
Hold	↑	h	X	No Change
	H	H	X	No Change

NOTE:

1. H = HIGH Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
L = LOW Voltage Level
I = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
X = Don't Care
↑ = LOW-to-HIGH Clock Transition

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial : $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_I = 2.7\text{V}$	—	—	± 1	μA
I_{IL}	Input LOW Current ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_I = 0.5\text{V}$	—	—	± 1	μA
I_I	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}$, $V_I = V_{CC}$ (Max.)		—	—	± 1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}$, $I_N = -18\text{mA}$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}$, $V_O = \text{GND}$		-60	-120	-225	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$	$I_{OH} = -8\text{mA}$	2.4	3.3	—	V
		$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -12\text{mA}$	2	3	—	
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$	$I_{OL} = 48\text{mA}$	—	0.3	0.5	V
I_{OFF}	Input/Output Power Off Leakage ⁽⁵⁾	$V_{CC} = 0\text{V}$, V_{IN} or $V_O = 4.5\text{V}$		—	—	± 1	μA
		$V_{IN} = V_{IH}$ or V_{IL}		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND}$ or V_{CC}		—	0.01	1	mA

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0\text{V}$, $+25^\circ\text{C}$ ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^\circ\text{C}$.
5. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$, Outputs Open $\overline{CE} = \text{GND}$ One Input Toggling 50% Duty Cycle		$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.15	0.25
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$, Outputs Open $f_{CP} = 10\text{MHz}$ $\overline{CE} = \text{GND}$ One Bit Toggling $f_i = 5\text{MHz}$ 50% Duty Cycle		$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	1.5	3.5
		$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$		—	2	5.5	mA
		$V_{CC} = \text{Max.}$, Outputs Open $f_{CP} = 10\text{MHz}$, 50% Duty Cycle $\overline{CE} = \text{GND}$ Eight Bits Toggling $f_i = 2.5\text{MHz}$ 50% Duty Cycle		$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.8	7.3 ⁽⁵⁾
		$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$		—	6	16.3 ⁽⁵⁾	

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.

3. Per TTL driven input; ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND.

4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.

5. Values for these conditions are examples of ΔI_{CC} formula. These limits are guaranteed but not tested.

6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$$I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP}/2 + f_i N_i)$$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)

D_H = Duty Cycle for TTL Inputs High

N_t = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Output Frequency

N_i = Number of Outputs at f_i

All currents are in millamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

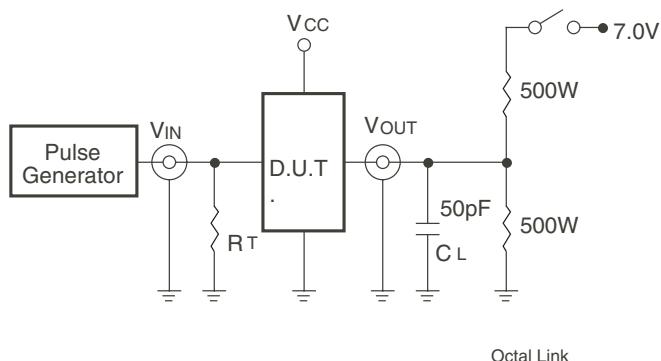
Symbol	Parameter	Condition ⁽¹⁾	74FCT377AT		74FCT377CT		74FCT377DT		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t_{PLH}	Propagation Delay CP to Qx	$CL = 50\text{pF}$ $RL = 500\Omega$	2	7.2	2	5.2	2	4.4	ns
t_{SUS}	Set-up Time HIGH or LOW D _x to CP		2	—	2	—	2	—	ns
t_H	Hold Time HIGH or LOW D _x to CP		1.5	—	1.5	—	1	—	ns
t_{SUS}	Set-up Time HIGH or LOW \overline{CE} to CP		3.5	—	3.5	—	3	—	ns
t_H	Hold Time HIGH or LOW \overline{CE} to CP		1.5	—	1.5	—	0	—	ns
t_W	CP Pulse Width HIGH or LOW		8	—	6	—	3	—	ns

NOTES:

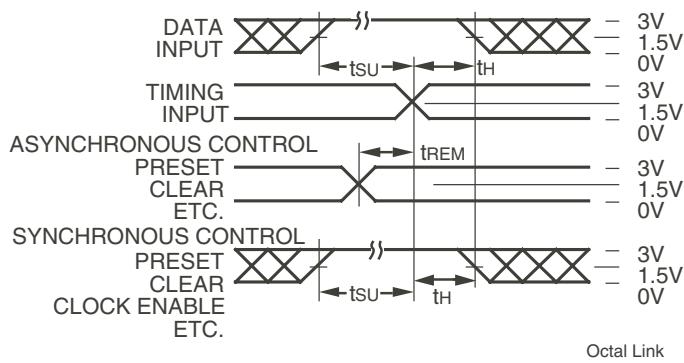
1. See test circuit and waveforms.

2. Minimum limits are guaranteed but not tested on Propagation Delays.

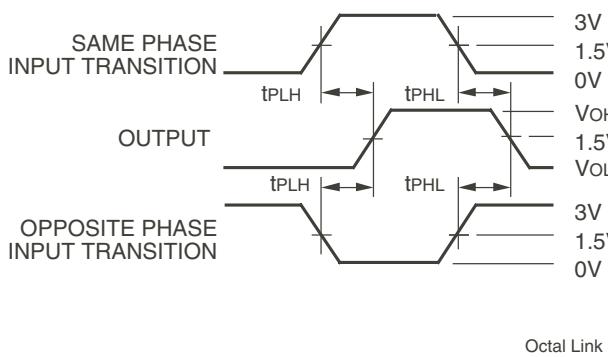
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-Up, Hold, and Release Times



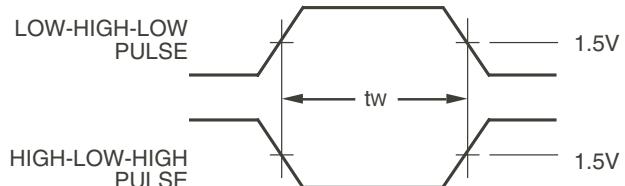
Propagation Delay

SWITCH POSITION

Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

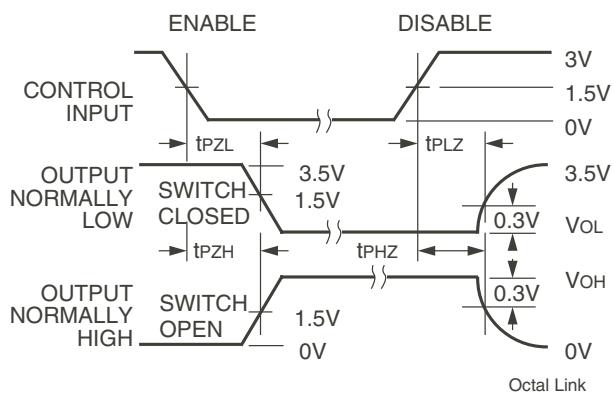
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

Octal Link

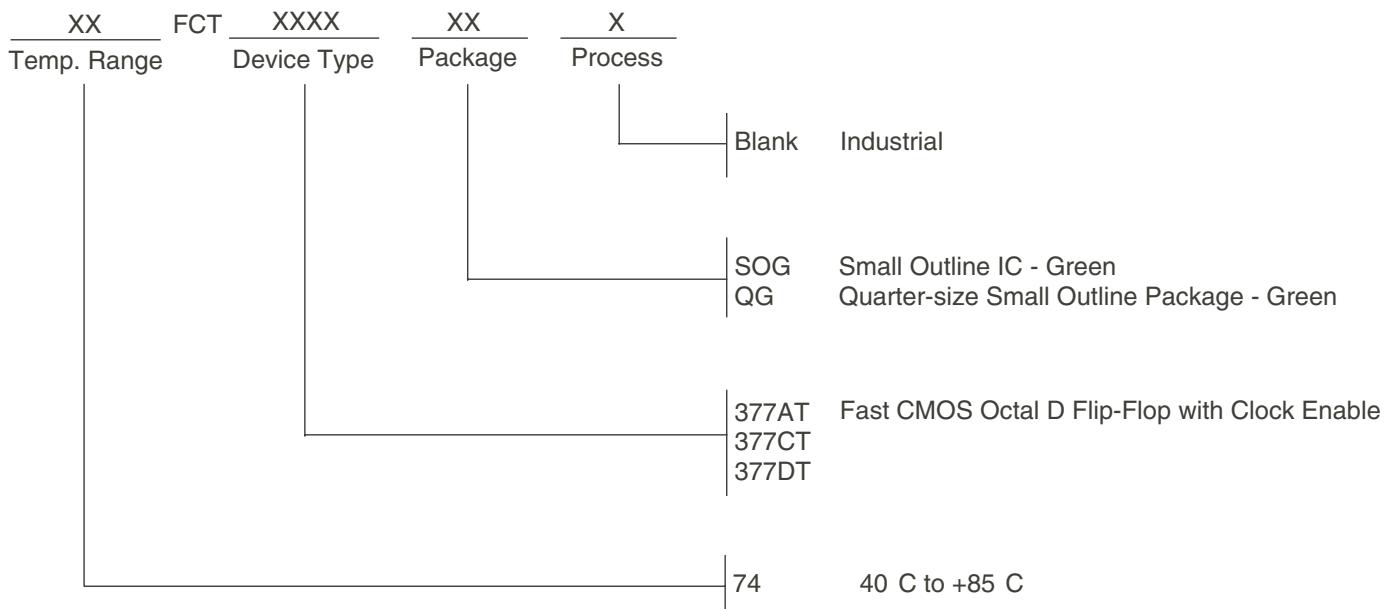


Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$.

ORDERING INFORMATION



Datasheet Document History

10/03/09 Pg. 6 Updated the ordering information by removing the "IDT" notation and non RoHS part.

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