

FEATURES:

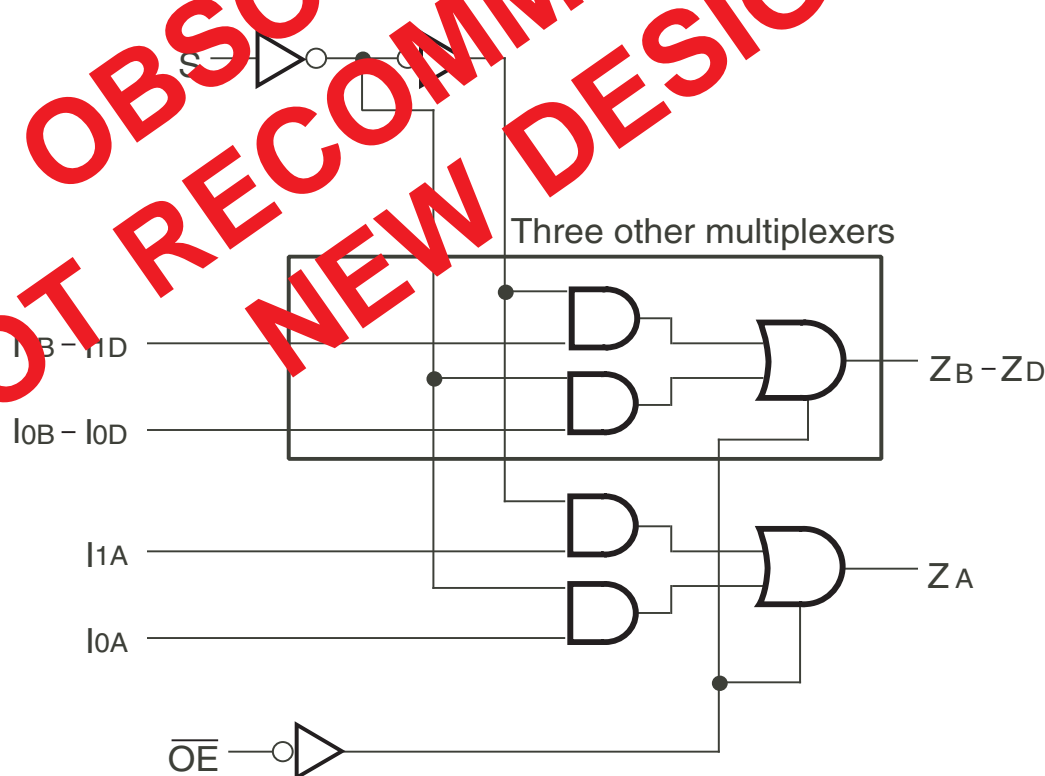
- A, C, and D grades
- Low input and output leakage $\leq 1\mu\text{A}$ (max.)
- CMOS power levels
- True TTL input and output compatibility:
 - $V_{OH} = 3.3V$ (typ.)
 - $V_{OL} = 0.3V$ (typ.)
- High Drive outputs (-15mA I_{OH} , 48mA I_{OL})
- Meets or exceeds JEDEC standard 18 specifications
- Power off disable outputs permit "live insertion"
- Available in SOIC and QSOP packages

DESCRIPTION:

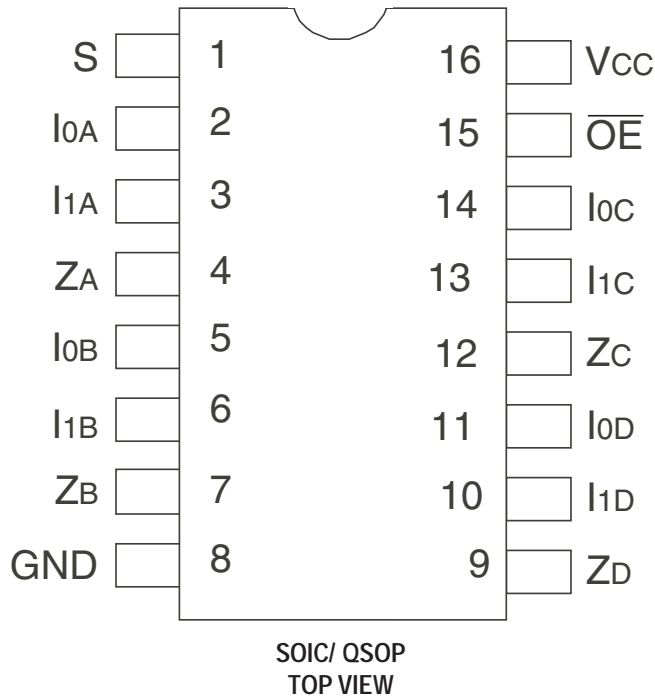
The FCT257T is a high-speed quad 2-input multiplexer built using an advanced dual metal CMOS technology. Four bits of data from two sources can be selected using the common select input. The four buffered outputs present the selected data in the true (non-inverting) form.

The FCT257T has a common Output Enable (\overline{OE}) input. When \overline{OE} is high, all outputs are switched to a high-impedance state allowing the outputs to interface directly with bus-oriented systems.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Description | Max | Unit |
|----------------------|--------------------------------------|-----------------|------|
| VTERM ⁽²⁾ | Terminal Voltage with Respect to GND | -0.5 to +7 | V |
| VTERM ⁽³⁾ | Terminal Voltage with Respect to GND | -0.5 to VCC+0.5 | V |
| TSTG | Storage Temperature | -65 to +150 | °C |
| IOUT | DC Output Current | -60 to +120 | mA |

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed VCC by +0.5V unless otherwise noted.
- Inputs and VCC terminals only.
- Output and I/O terminals only.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Typ. | Max. | Unit |
|--------|--------------------------|------------|------|------|------|
| CIN | Input Capacitance | VIN = 0V | 6 | 10 | pF |
| COUT | Output Capacitance | VOUT = 0V | 8 | 12 | pF |

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

| Pin Names | Description |
|-----------|----------------------------|
| I0A-I0D | Source 0 Data Inputs |
| I1A-I1D | Source 1 Data Inputs |
| OE | Output Enable (Active LOW) |
| S | Select Input |
| ZA-ZD | Outputs |

FUNCTION TABLE⁽¹⁾

| Inputs | | | | Output Zx |
|--------|---|----|----|-----------|
| OE | S | I0 | I1 | |
| H | X | X | X | Z |
| L | H | X | L | L |
| L | H | X | H | H |
| L | L | L | X | L |
| L | L | H | X | H |

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Typ. ⁽²⁾ | Max. | Unit |
|-----------|---|--|---------------------|------|---------------------|---------|---------------|
| V_{IH} | Input HIGH Level | Guaranteed Logic HIGH Level | | 2 | — | — | V |
| V_{IL} | Input LOW Level | Guaranteed Logic LOW Level | | — | — | 0.8 | V |
| I_{IH} | Input HIGH Current ⁽⁴⁾ | $V_{CC} = \text{Max.}$ | $V_I = 2.7\text{V}$ | — | — | ± 1 | μA |
| I_{IL} | Input LOW Current ⁽⁴⁾ | $V_{CC} = \text{Max.}$ | $V_I = 0.5\text{V}$ | — | — | ± 1 | μA |
| I_{OZH} | High Impedance Output Current (3-State output pins) ⁽⁴⁾ | $V_{CC} = \text{Max.}$ | $V_O = 2.7\text{V}$ | — | — | ± 1 | μA |
| I_{OZL} | | | $V_O = 0.5\text{V}$ | — | — | ± 1 | |
| I_I | Input HIGH Current ⁽⁴⁾ | $V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$ | | — | — | ± 1 | μA |
| V_{IK} | Clamp Diode Voltage | $V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$ | | — | -0.7 | -1.2 | V |
| V_H | Input Hysteresis | — | | — | 200 | — | mV |
| I_{CC} | Quiescent Power Supply Current | $V_{CC} = \text{Max.}, V_{IN} = \text{GND or } V_{CC}$ | | — | 0.01 | 1 | mA |

OUTPUT DRIVE CHARACTERISTICS

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Typ. ⁽²⁾ | Max. | Unit |
|-----------|---|--|-------------------------|------|---------------------|---------|---------------|
| V_{OH} | Output HIGH Voltage | $V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ | $I_{OH} = -8\text{mA}$ | 2.4 | 3.3 | — | V |
| | | | $I_{OH} = -15\text{mA}$ | 2 | 3 | — | |
| V_{OL} | Output LOW Voltage | $V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ | $I_{OL} = 48\text{mA}$ | — | 0.3 | 0.5 | V |
| | | | | | | | |
| I_{OS} | Short Circuit Current | $V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$ | | -60 | -120 | -225 | mA |
| I_{OFF} | Input/Output Power Off Leakage ⁽⁵⁾ | $V_{CC} = 0\text{V}, V_{IN} \text{ or } V_O \leq 4.5\text{V}$ | | — | — | ± 1 | μA |

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.
5. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Typ. ⁽²⁾ | Max. | Unit |
|-----------------|---|---|--|------|---------------------|--------------------|------------|
| ΔI_{CC} | Quiescent Power Supply Current TTL Inputs HIGH | $V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$ | | — | 0.5 | 2 | mA |
| I_{CCD} | Dynamic Power Supply Current ⁽⁴⁾ | $V_{CC} = \text{Max.}$ Outputs Open $\overline{OE} = \text{GND}$ One Input Toggling 50% Duty Cycle | $V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$ | — | 0.15 | 0.25 | mA/ MHz |
| I_C | Total Power Supply Current ⁽⁶⁾ | $V_{CC} = \text{Max.}$ Outputs Open $f_o = 10\text{MHz}$ 50% Duty Cycle $\overline{OE} = \text{GND}$ One Bit Toggling | $V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$ | — | 1.5 | 3.5 | mA |
| | | | $V_{IN} = 3.4V$ $V_{IN} = \text{GND}$ | — | 1.8 | 4.5 | |
| | | $V_{CC} = \text{Max.}$ Outputs Open $f_o = 2.5\text{MHz}$ 50% Duty Cycle $\overline{OE} = \text{GND}$ Four Bits Toggling | $V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$ | — | 1.5 | 3.5 ⁽⁵⁾ | |
| | | | $V_{IN} = 3.4V$ $V_{IN} = \text{GND}$ | — | 2.5 | 7.5 ⁽⁵⁾ | |

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
 - Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
 - Per TTL driven input; ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
 - This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
 - Values for these conditions are examples of ΔI_{CC} formula. These limits are guaranteed but not tested.
 - $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} \text{ DHNT} + I_{CCD} (f_o \text{No})$
 $I_{CC} = \text{Quiescent Current}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$
 $\text{DH} = \text{Duty Cycle for TTL Inputs High}$
 $\text{Nr} = \text{Number of TTL Inputs at DH}$
 $I_{CCD} = \text{Dynamic Current caused by an Input Transition Pair (HLH or LHL)}$
 $f_o = \text{Output Frequency}$
 $\text{No} = \text{Number of Outputs at } f_o$
- All currents are in milliamps and all frequencies are in megahertz.

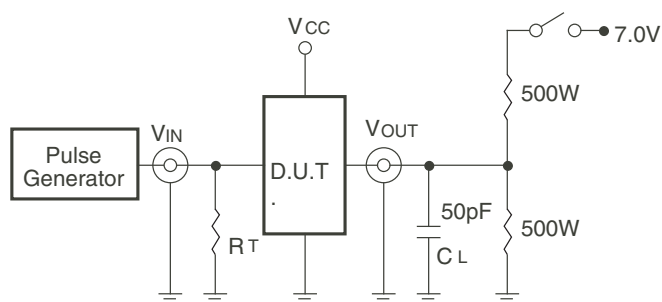
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| Symbol | Parameter | Condition ⁽¹⁾ | FCT257AT | | FCT275CT | | FCT275DT | | Unit |
|------------------------|-------------------------------|--|---------------------|------|---------------------|------|---------------------|------|------|
| | | | Min. ⁽²⁾ | Max. | Min. ⁽²⁾ | Max. | Min. ⁽²⁾ | Max. | |
| t_{PLH} t_{PHL} | Propagation Delay Ix to Zx | $C_L = 50\text{pF}$ $R_L = 500\Omega$ | 1.5 | 5 | 1.5 | 4.3 | 1.5 | 3.9 | ns |
| t_{PLH} t_{PHL} | Propagation Delay S to Zx | | 1.5 | 7 | 1.5 | 5.2 | 1.5 | 4.4 | ns |
| t_{PZH} t_{PZL} | Output Enable Time | | 1.5 | 7 | 1.5 | 6 | 1.5 | 4.4 | ns |
| t_{PHZ} t_{PLZ} | Output Disable Time | | 1.5 | 5.5 | 1.5 | 5 | 1.5 | 4.4 | ns |

NOTES:

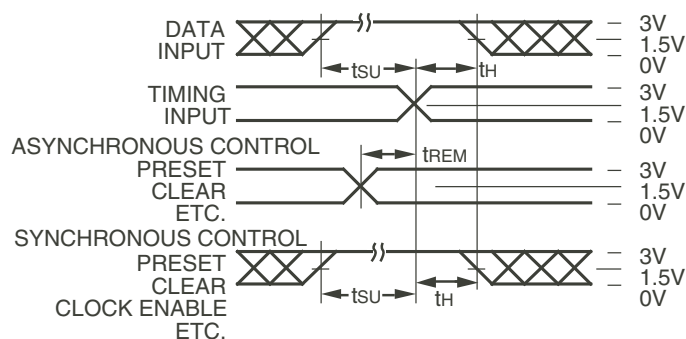
- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS



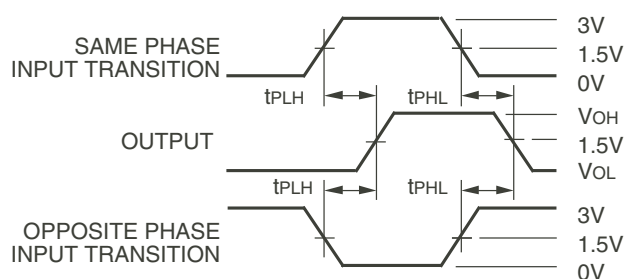
Octal Link

Test Circuits for All Outputs



Octal Link

Set-Up, Hold, and Release Times



Octal Link

Propagation Delay

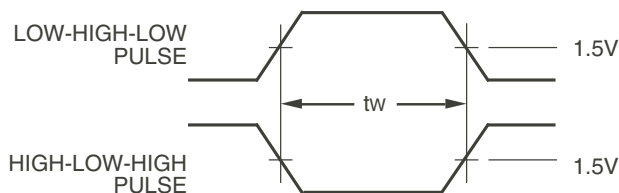
SWITCH POSITION

| Test | Switch |
|---|--------|
| Open Drain Disable Low Enable Low | Closed |
| All Other Tests | Open |

DEFINITIONS:

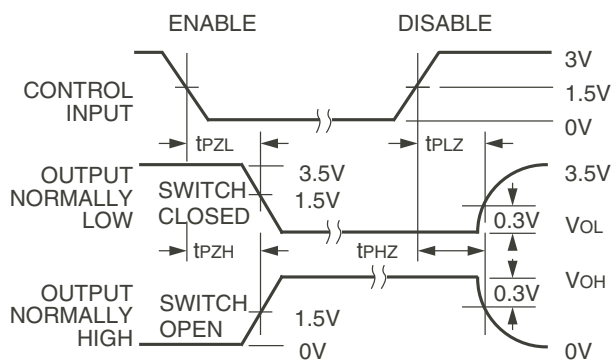
CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

Octal Link



Octal Link

Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.

ORDERING INFORMATION

| XX | FCT | XXXX | XX | X | | |
|-------------|-----|-------------|---------|-------------------------|--|--|
| Temp. Range | | Device Type | Package | Process | | |
| | | | | Blank | Industrial | |
| | | | | SOG | Small Outline IC (300 mil) - Green | |
| | | | | QG | Quarter-size Small Outline Package - Green | |
| | | | | 257AT 257CT 257DT | Quad 2-Input Multiplexer (3-State) | |
| | | | | 74 | □ 40°C to +85°C | |

Datasheet Document History

| | |
|------------|--|
| 09/29/2009 | Pg. 6 Updated the ordering information by removing the "IDT" notation and non RoHS part. |
| 08/14/2015 | PDN# CQ-15-04 issued. See IDT.com for PDN specifics. |
| 09/03/2019 | Datasheet changed to Obsolete Status. |

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