

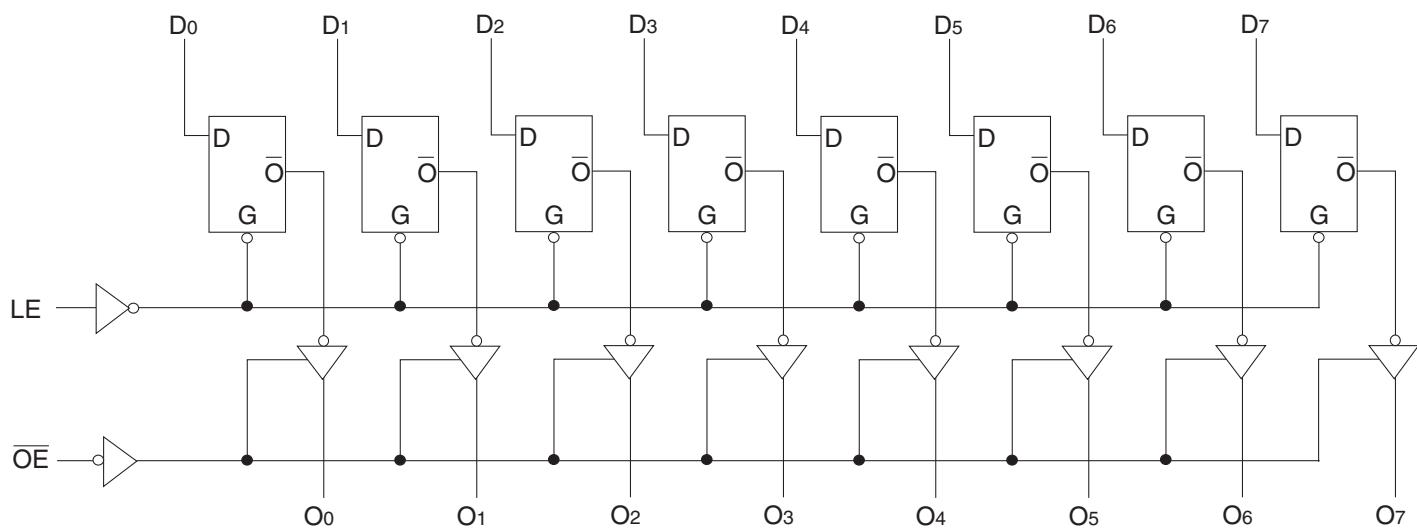
FEATURES:

- A and C grades
- Low input and output leakage $\leq 1\mu\text{A}$ (max.)
- CMOS power levels
- True TTL input and output compatibility:
 - $V_{OH} = 3.3\text{V}$ (typ.)
 - $V_{OL} = 0.3\text{V}$ (typ.)
- Meets or exceeds JEDEC standard 18 specifications
- Resistor outputs -15mA I_{OH} , 12mA I_{OL}
- Reduced system switching noise
- Available in QSOP package

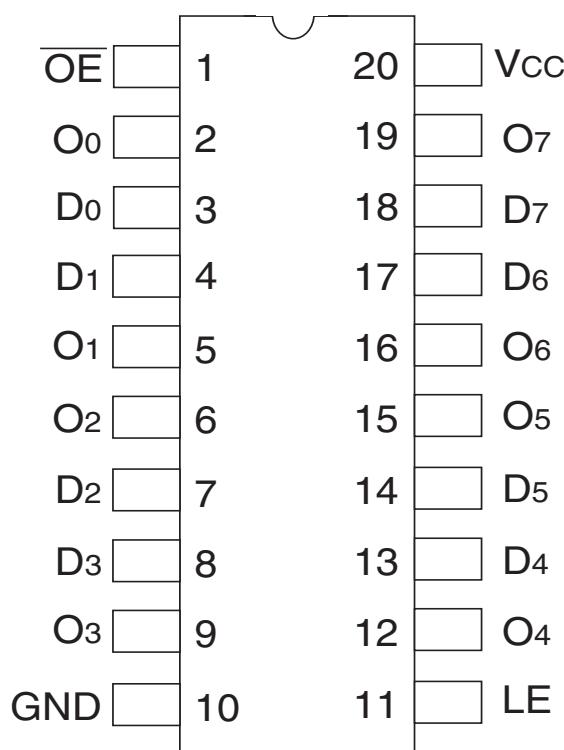
DESCRIPTION:

The FCT2373T is an octal transparent latch built using an advanced dual metal CMOS technology. These octal latches have 3-state outputs and are intended for bus oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is high. When LE is low, the data that meets the set-up time is latched. Data appears on the bus when the Output Enable (\overline{OE}) is low. When \overline{OE} is high, the bus output is in the high-impedance state.

The FCT2373T has balanced drive outputs with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times-reducing the need for external series terminating resistors. The FCT2373T parts are plug-in replacements for FCT373T parts.

FUNCTIONAL BLOCK DIAGRAM

PIN CONFIGURATION



QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-60 to +120	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Output and I/O terminals only.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
D _x	Data Inputs
LE	Latch Enable Input (Active HIGH)
OE	Output Enable Input (Active LOW)
O _x	3-State Outputs

FUNCTION TABLE⁽¹⁾

Inputs			Outputs
D _x	LE	OE	O _x
L	H	L	L
H	H	L	H
X	X	H	Z

NOTE:

1. H = HIGH Voltage Level
X = Don't Care
L = LOW Voltage Level
Z = High Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: TA = -40°C to +85°C, VCC = 5.0V ±5%

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
VIH	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
VIL	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I _{IH}	Input HIGH Current ⁽⁴⁾	V _{CC} = Max.	VI = 2.7V	—	—	±1	µA
I _{IL}	Input LOW Current ⁽⁴⁾	V _{CC} = Max.	VI = 0.5V	—	—	±1	µA
I _{OZH}	High Impedance Output Current (3-State Output Pins) ⁽⁴⁾	V _{CC} = Max.	VI = 2.7V	—	—	±1	µA
I _{OZL}			VI = 0.5V	—	—	±1	
I _I	Input HIGH Current ⁽⁴⁾	V _{CC} = Max., VI = V _{CC} (Max.)		—	—	±1	µA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18mA		—	-0.7	-1.2	V
V _H	Input Hysteresis	—		—	200	—	mV
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max. VIN = GND or V _{CC}		—	0.01	1	mA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _{ODL}	Output LOW Current	V _{CC} = 5V, VIN = VIH or VIL, V _{OUT} = 1.5V ⁽³⁾		16	48	—	mA
I _{ODH}	Output HIGH Current	V _{CC} = 5V, VIN = VIH or VIL, V _{OUT} = 1.5V ⁽³⁾		-16	-48	—	mA
V _{OH}	Output HIGH Voltage	V _{CC} = Min VIN = VIH or VIL	I _{OH} = -15mA	2.4	3.3	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min VIN = VIH or VIL	I _{OL} = 12mA	—	0.3	0.5	V

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. The test limit for this parameter is ±5µA at TA = -55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾		—	0.5	2	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max. Outputs Open \overline{OE} = GND One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	—	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle \overline{OE} = GND LE = V _{CC} One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND	—	0.6	2.2	mA
		V _{IN} = 3.4V V _{IN} = GND	—	0.9	3.2		
		V _{IN} = V _{CC} V _{IN} = GND	—	1.2	3.4 ⁽⁵⁾		
		V _{IN} = 3.4V V _{IN} = GND	—	3.2	11.4 ⁽⁵⁾		

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input: (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of ΔI_{CC} formula. These limits are guaranteed but not tested.

6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$$I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP}/2 + f_i N_i)$$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current caused by an Input Transition Pair (H_LH or L_HL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Output Frequency

N_i = Number of Outputs at f_i

All currents are in millamps and all frequencies are in megahertz.

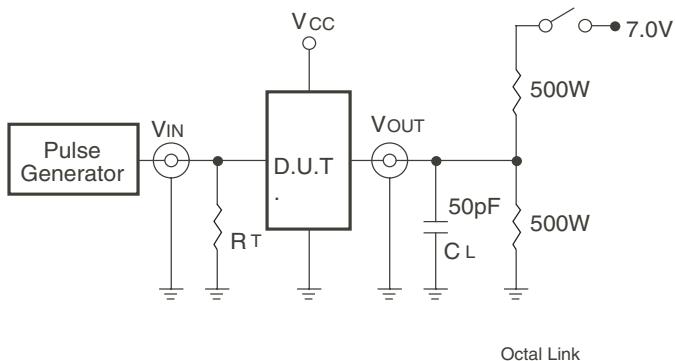
SWITCHING CHARACTERISTICS OVER OPERATING RANGE⁽¹⁾

Symbol	Parameter	Condition ⁽¹⁾	74FCT2373AT		74FCT2373CT		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t_{PLH}	Propagation Delay Dx to Ox	$C_L = 50 \text{ pF}$ $R_L = 500\Omega$	1.5	5.2	1.5	4.2	ns
t_{PHL}	Propagation Delay LE to Ox		2	8.5	2	5.5	ns
t_{PZH}	Output Enable Time		1.5	6.5	1.5	5.5	ns
t_{PZL}	Output Disable Time		1.5	5.5	1.5	5	ns
t_{SU}	Set-up Time HIGH or LOW, Dx to LE		2	—	2	—	ns
t_H	Hold Time HIGH or LOW, Dx to LE		1.5	—	1.5	—	ns
t_W	LE Pulse Width HIGH ⁽³⁾		5	—	5	—	ns

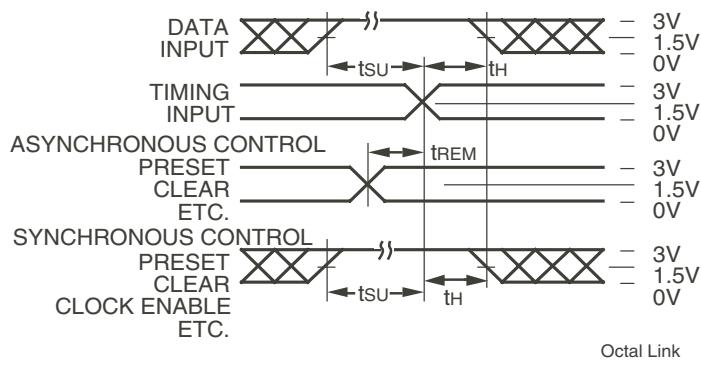
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

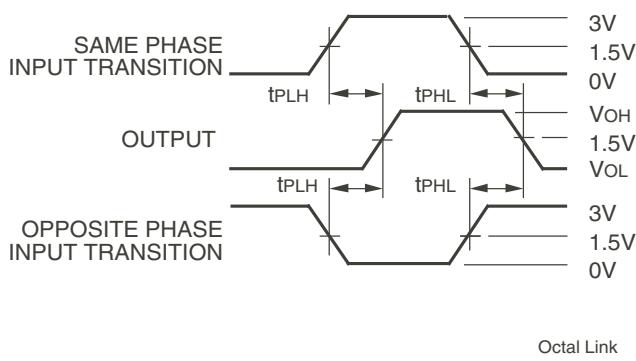
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-Up, Hold, and Release Times



Propagation Delay

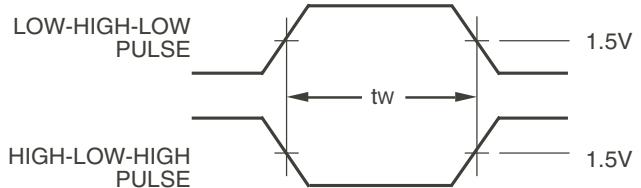
SWITCH POSITION

Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

DEFINITIONS:

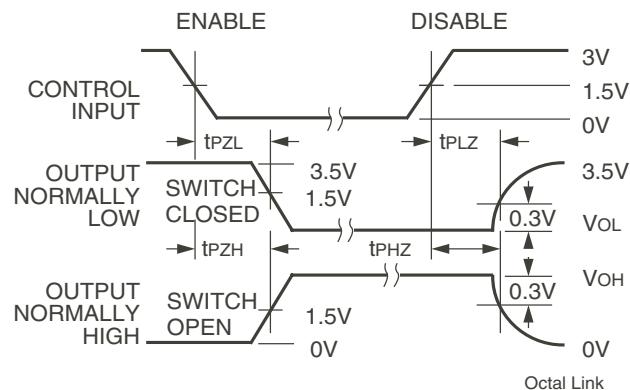
CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

Octal Link

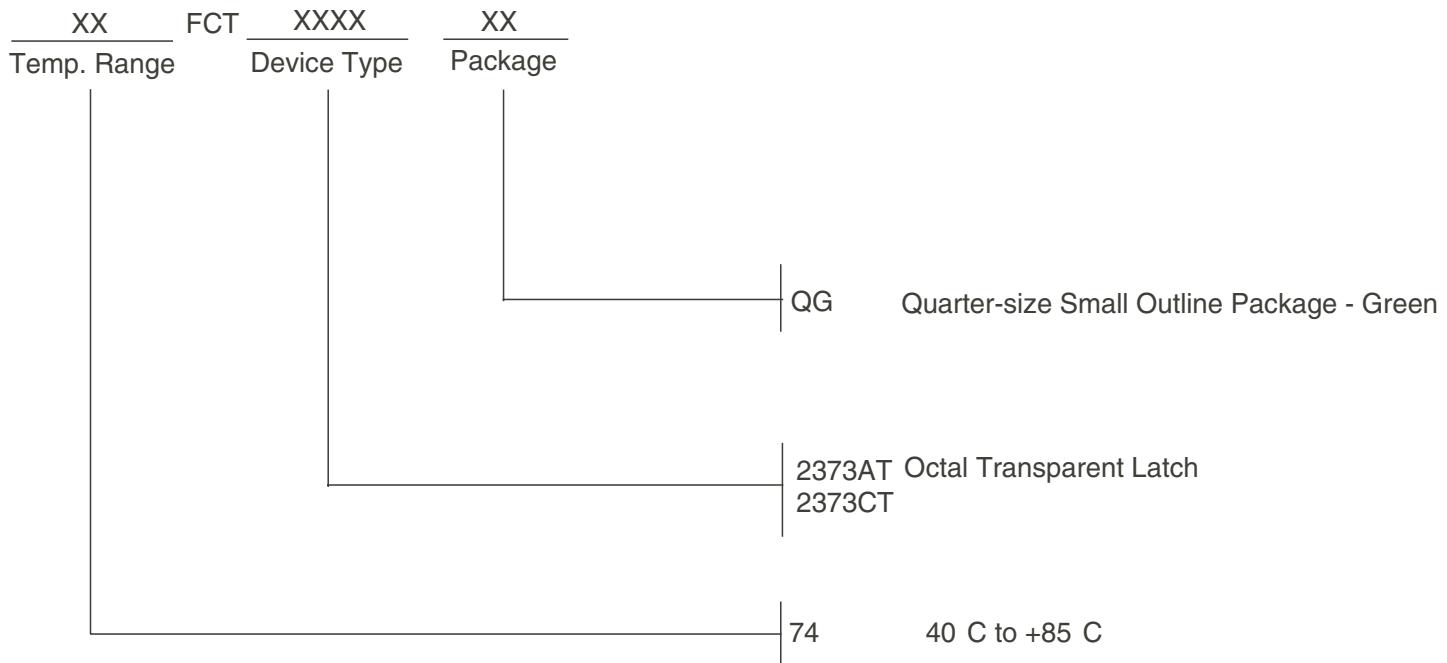


Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$.

ORDERING INFORMATION



Datasheet Document History

09/29/09 Pg. 7 Updated the ordering information by removing the "IDT" notation and non RoHS part.

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