

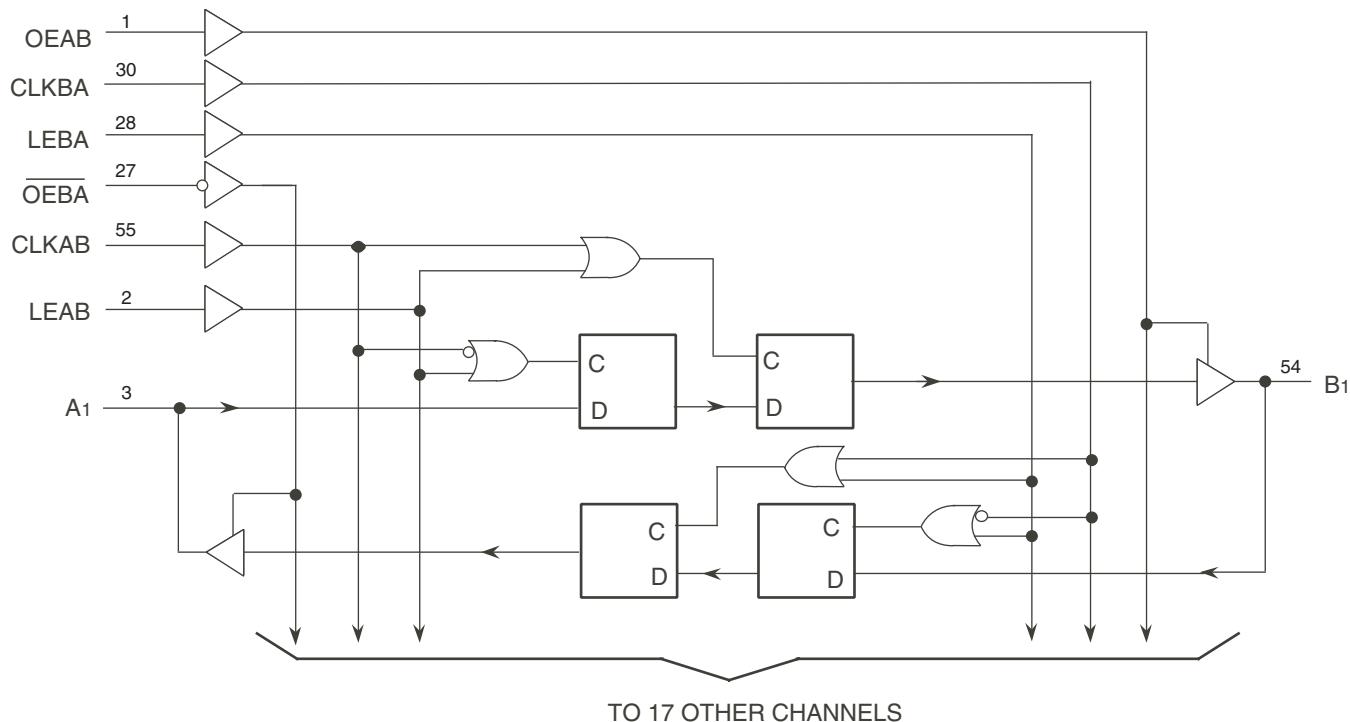
**FEATURES:**

- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical  $t_{sk(o)}$  (Output Skew) < 250ps
- Low input and output leakage  $\leq 1\mu\text{A}$  (max.)
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model ( $C = 200\text{pF}$ ,  $R = 0$ )
- High drive outputs ( $-32\text{mA}$   $I_{OH}$ ,  $64\text{mA}$   $I_{OL}$ )
- Power off disable outputs permit "live insertion"
- Typical  $\text{V}_{OLP}$  (Output Ground Bounce) < 1.0V at  $V_{CC} = 5\text{V}$ ,  $TA = 25^\circ\text{C}$
- Available in TSSOP package

**DESCRIPTION:**

The FCT16501T 18-bit registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power 18-bit registered bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes. Data flow in each direction is controlled by output-enable ( $OEAB$  and  $\overline{OEBA}$ ), latch enable ( $LEAB$  and  $LEBA$ ) and clock ( $CLKAB$  and  $CLKBA$ ) inputs. For A-to-B data flow, the device operates in transparent mode when  $LEAB$  is high. When  $LEAB$  is low, the A bus data is latched if  $CLKAB$  is held at a high or low logic level. If  $LEAB$  is low, the A bus data is stored in the latch/flip-flop on the low-to-high transition of  $CLKAB$ .  $OEAB$  is the output enable for the B port. Data flow from the B port to the A port is similar but requires using  $\overline{OEBA}$ ,  $LEBA$  and  $CLKBA$ . Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT16501T are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

**FUNCTIONAL BLOCK DIAGRAM**

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**INDUSTRIAL TEMPERATURE RANGE**

**SEPTEMBER 2009**

## PIN CONFIGURATION

OEAB	1	56	GND
LEAB	2	55	CLKAB
A1	3	54	B1
GND	4	53	GND
A2	5	52	B2
A3	6	51	B3
Vcc	7	50	Vcc
A4	8	49	B4
A5	9	48	B5
A6	10	47	B6
GND	11	46	GND
A7	12	45	B7
A8	13	44	B8
A9	14	43	B9
A10	15	42	B10
A11	16	41	B11
A12	17	40	B12
GND	18	39	GND
A13	19	38	B13
A14	20	37	B14
A15	21	36	B15
Vcc	22	35	Vcc
A16	23	34	B16
A17	24	33	B17
GND	25	32	GND
A18	26	31	B18
OEBA	27	30	CLKBA
LEBA	28	29	GND

TSSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to 7	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-60 to +120	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXX Output and I/O terminals.
3. Output and I/O terminals for FCT162XXX.

## CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	3.5	6	pF
COUT	Output Capacitance	VOUT = 0V	3.5	8	pF

NOTE:

1. This parameter is measured at characterization but not tested.

## FUNCTION TABLE<sup>(1, 4)</sup>

Inputs				Outputs
OEAB	LEAB	CLKAB	Ax	Bx
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	L	X	B <sup>(2)</sup>
H	L	H	X	B <sup>(3)</sup>

NOTES:

1. A-to-B data flow is shown. B-to-A data flow is similar but uses  $\bar{OEBA}$ ,  $LEBA$ , and  $CLKBA$ .
2. Output level before the indicated steady-state input conditions were established.
3. Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
4. H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High-impedance  
↑ = LOW-to-HIGH Transition

## PIN DESCRIPTION

Pin Names	Description
OEAB	A-to-B Output Enable Input
$\bar{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs

**DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE**

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$ 

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
$I_{IH}$	Input HIGH Current (Input pins) <sup>(5)</sup>	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	$\pm 1$	$\mu\text{A}$
	Input HIGH Current (I/O pins) <sup>(5)</sup>			—	—	$\pm 1$	
$I_{IL}$	Input LOW Current (Input pins) <sup>(5)</sup>		$V_I = \text{GND}$	—	—	$\pm 1$	
	Input LOW Current (I/O pins) <sup>(5)</sup>			—	—	$\pm 1$	
$I_{OZH}$	High Impedance Output Current	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZL}$	(3-State Output pins) <sup>(5)</sup>		$V_O = 0.5\text{V}$	—	—	$\pm 1$	
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}$ , $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}$ , $V_O = \text{GND}$ <sup>(3)</sup>		-80	-140	-250	mA
$V_H$	Input Hysteresis	—		—	100	—	mV
$I_{CCL}$ $I_{CCH}$ $I_{CCZ}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND or } V_{CC}$		—	5	500	$\mu\text{A}$

**OUTPUT DRIVE CHARACTERISTICS**

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$I_O$	Output Drive Current	$V_{CC} = \text{Max.}$ , $V_O = 2.5\text{V}$ <sup>(3)</sup>		-50	—	-180	mA
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -3\text{mA}$	2.5	3.5	—	V
			$I_{OH} = -15\text{mA}$	2.4	3.5	—	
			$I_{OH} = -32\text{mA}$ <sup>(4)</sup>	2	3	—	
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 64\text{mA}$	—	0.2	0.55	V
$I_{OFF}$	Input/Output Power Off Leakage <sup>(5)</sup>	$V_{CC} = 0\text{V}$ , $V_{IN}$ or $V_O \leq 4.5\text{V}$		—	—	$\pm 1$	$\mu\text{A}$

## NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $+25^\circ\text{C}$  ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. This test limit for this parameter is  $\pm 5\mu\text{A}$  at  $T_A = -55^\circ\text{C}$ .

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	V <sub>CC</sub> = Max. V <sub>IN</sub> = 3.4V <sup>(3)</sup>	—	0.5	1.5	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>(4)</sup>	V <sub>CC</sub> = Max., Outputs Open OEAB = $\overline{OEBA}$ = V <sub>CC</sub> or GND One Input Toggling 50% Duty Cycle	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND	—	75	120
$I_C$	Total Power Supply Current <sup>(6)</sup>	V <sub>CC</sub> = Max., Outputs Open f <sub>CP</sub> = 10MHz (CLKAB) 50% Duty Cycle OEAB = $\overline{OEBA}$ = V <sub>CC</sub> LEAB = GND One Bit Toggling f <sub>i</sub> = 5MHz 50% Duty Cycle	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND	—	0.8	1.7
		V <sub>CC</sub> = Max., Outputs Open f <sub>CP</sub> = 10MHz (CLKAB) 50% Duty Cycle OEAB = $\overline{OEBA}$ = V <sub>CC</sub> LEAB = GND Eighteen Bits Toggling f <sub>i</sub> = 2.5MHz 50% Duty Cycle	V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	—	1.3	3.2
		V <sub>CC</sub> = Max., Outputs Open f <sub>CP</sub> = 10MHz (CLKAB) 50% Duty Cycle OEAB = $\overline{OEBA}$ = V <sub>CC</sub> LEAB = GND Eighteen Bits Toggling f <sub>i</sub> = 2.5MHz 50% Duty Cycle	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND	—	3.8	6.5 <sup>(5)</sup>
		V <sub>CC</sub> = Max., Outputs Open f <sub>CP</sub> = 10MHz (CLKAB) 50% Duty Cycle OEAB = $\overline{OEBA}$ = V <sub>CC</sub> LEAB = GND Eighteen Bits Toggling f <sub>i</sub> = 2.5MHz 50% Duty Cycle	V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	—	8.5	20.8 <sup>(5)</sup>

### NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient.

3. Per TTL driven input (V<sub>IN</sub> = 3.4V). All other inputs at V<sub>CC</sub> or GND.

4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.

5. Values for these conditions are examples of the  $I_C$  formula. These limits are guaranteed but not tested.

6.  $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$$I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$$

$I_{CC}$  = Quiescent Current (I<sub>CC1</sub>, I<sub>CC2</sub> and I<sub>CC3</sub>)

$\Delta I_{CC}$  = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)

D<sub>H</sub> = Duty Cycle for TTL Inputs High

N<sub>T</sub> = Number of TTL Inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)

N<sub>CP</sub> = Number of Clock Inputs at f<sub>CP</sub>

f<sub>i</sub> = Input Frequency

N<sub>i</sub> = Number of Inputs at f<sub>i</sub>

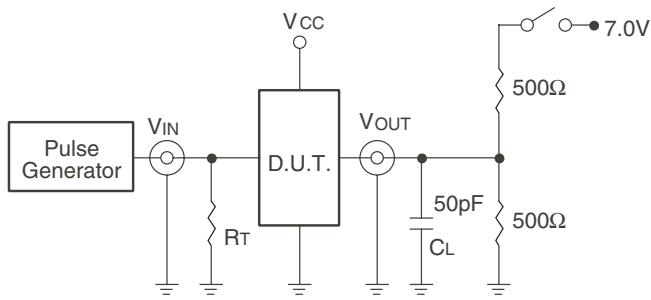
## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition <sup>(1)</sup>	FCT16501AT		FCT16501CT		Unit
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
f <sub>MAX</sub>	CLKAB or CLKBA frequency <sup>(3)</sup>	CL = 50pF RL = 500Ω	—	150	—	150	MHz
t <sub>PLH</sub>	Propagation Delay Ax to Bx or Bx to Ax		1.5	5.1	1.5	4.3	ns
t <sub>PLH</sub>	Propagation Delay LEBA to Ax, LEAB to Bx		1.5	5.6	1.5	4.4	ns
t <sub>PLH</sub>	Propagation Delay CLKBA to Ax, CLKAB to Bx		1.5	5.6	1.5	4.4	ns
t <sub>PZH</sub>	Output Enable Time OEBA to Ax, OEAB to Bx		1.5	6	1.5	4.8	ns
t <sub>PHZ</sub>	Output Disable Time OEBA to Ax, OEAB to Bx		1.5	5.6	1.5	5.2	ns
t <sub>su</sub>	Set-up Time, HIGH or LOW Ax to CLKAB, Bx to CLKBA		3	—	2.4	—	ns
t <sub>h</sub>	Hold Time, HIGH or LOW Ax to CLKAB, Bx to CLKBA		0	—	0	—	ns
t <sub>su</sub>	Set-up Time HIGH or LOW Ax to LEAB, Bx to LEBA	Clock LOW Clock HIGH	3	—	2	—	ns
t <sub>h</sub>	Hold Time, HIGH or LOW Ax to LEAB, Bx to LEBA		1.5	—	1.5	—	ns
t <sub>w</sub>	LEAB or LEBA Pulse Width HIGH <sup>(3)</sup>		1.5	—	0.5	—	ns
t <sub>w</sub>	CLKAB or CLKBA Pulse Width HIGH or LOW <sup>(3)</sup>		3	—	3	—	ns
t <sub>SK(0)</sub>	Output Skew <sup>(4)</sup>		—	0.5	—	0.5	ns

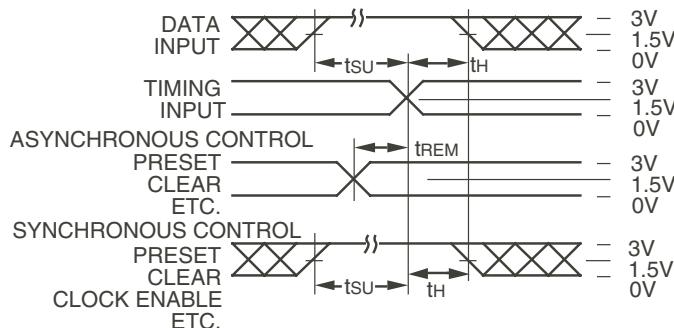
NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

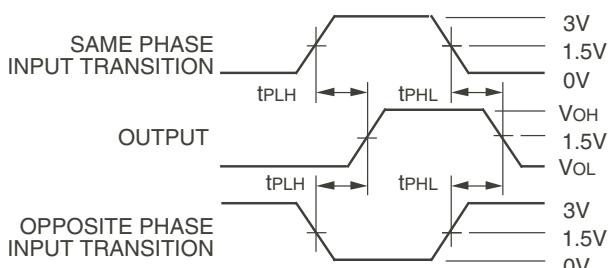
## TEST CIRCUITS AND WAVEFORMS



*Test Circuits for All Outputs*



*Set-up, Hold, and Release Times*



*Propagation Delay*

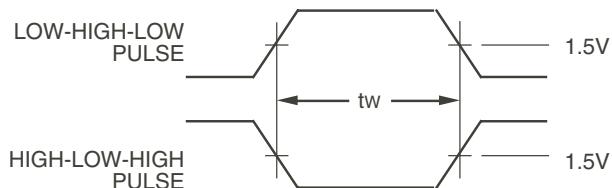
## SWITCH POSITION

Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

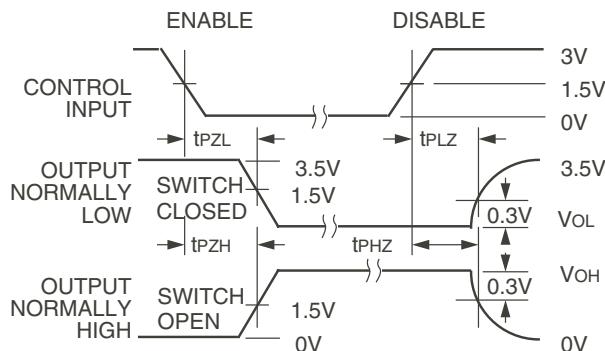
### DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

R<sub>T</sub> = Termination resistance: should be equal to Z<sub>out</sub> of the Pulse Generator.



*Pulse Width*

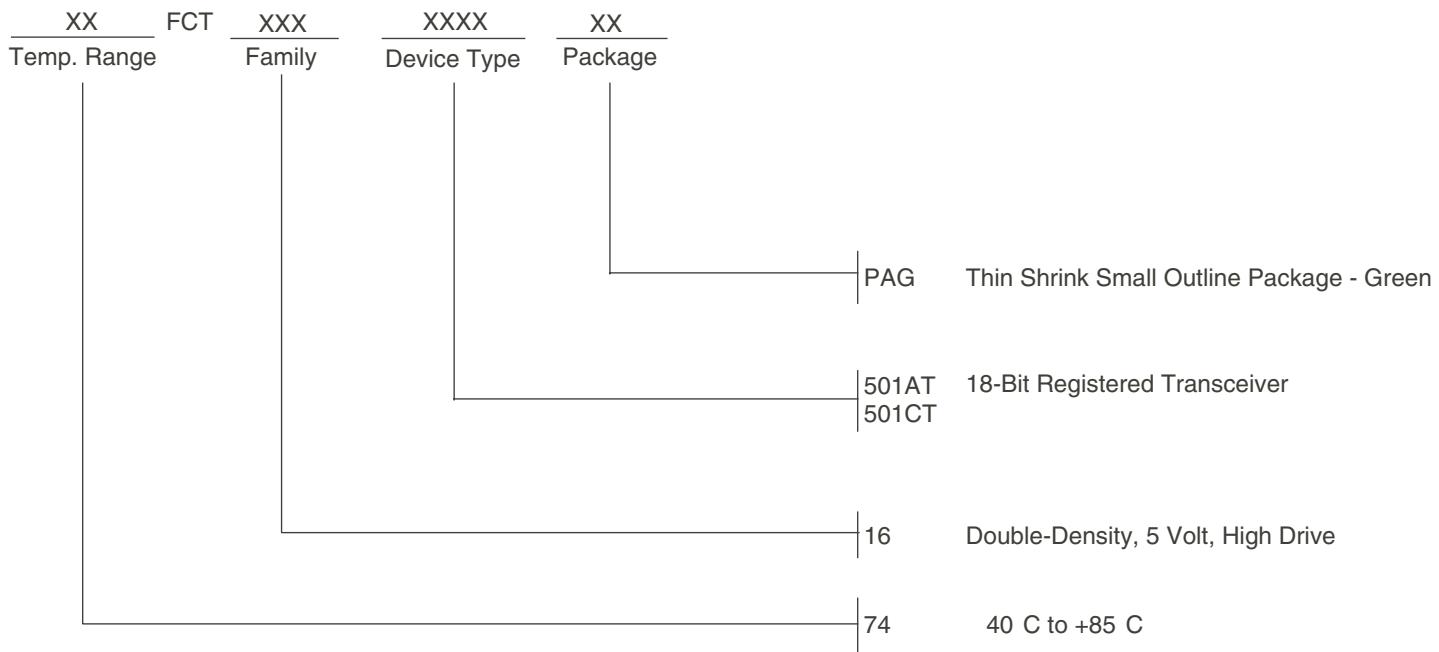


*Enable and Disable Times*

### NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_f \leq 2.5\text{ns}$ ;  $t_r \leq 2.5\text{ns}$ .

## ORDERING INFORMATION



## Datasheet Document History

09/28/09 Pg. 7      Updated the ordering information by removing the "IDT" notation and non RoHS part.

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