

FEATURES:

- Pin-out compatible with standard '244 Logic products
- 5Ω A/B bi-directional switch
- Isolation under power-off conditions
- Over-voltage tolerant
- Latch-up performance exceeds 100mA
- $V_{CC} = 2.3V - 3.6V$, Normal Range
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model ($C = 200pF$, $R = 0$)
- Available in QSOP and TSSOP packages

DESCRIPTION:

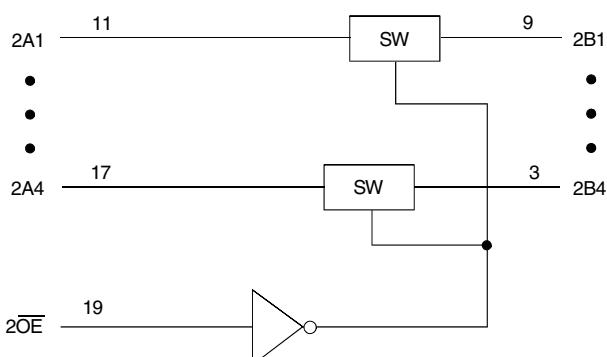
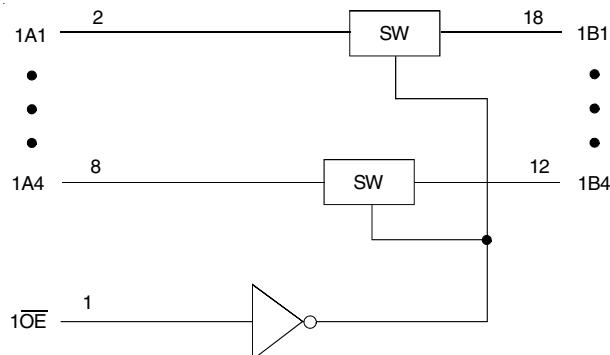
The octal bus switch has standard 244 pinouts. The CBLV3244 is designed for asynchronous communication between data buses. Sets of four switches are controlled by one output Enable (\overline{OE}). When \overline{OE} is low, the set of four bus switches is on and port A is connected to port B. When \overline{OE} is high, the set of four bus switches is off and a high impedance exists between port A and port B.

To ensure the high-impedance state during power up or power down, both \overline{OE} s should be tied to V_{CC} through a pullup resistor.

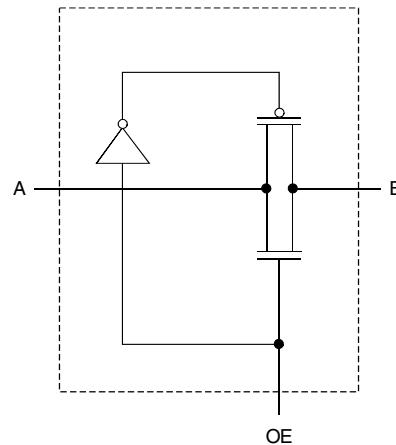
APPLICATIONS:

- 3.3V High Speed Bus Switching and Bus Isolation

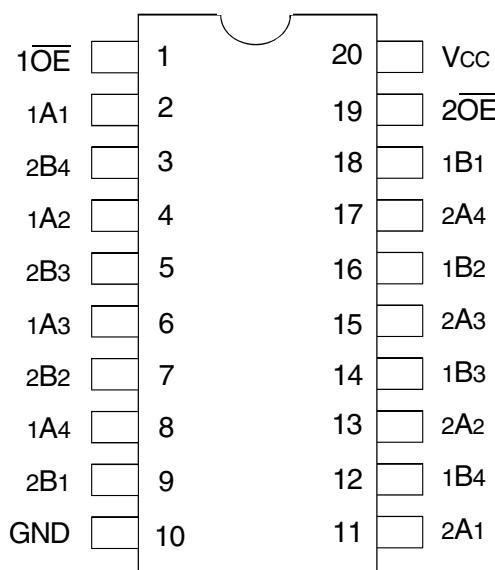
FUNCTIONAL BLOCK DIAGRAM



SIMPLIFIED SCHEMATIC, EACH SWITCH



PIN CONFIGURATION



TOP VIEW

Package Type	Package Code	Order Code
TSSOP	PGG20	PGG
QSOP	PCG20	QG

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
Vcc	Supply Voltage Range	-0.5 to +4.6	V
VI	Input Voltage Range	-0.5 to +4.6	V
	Continuous Channel Current	128	mA
IIK	Input Clamp Current, VI<0	-50	mA
TSTG	Storage Temperature	-65 to +150	°C

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PIN DESCRIPTION

Pin Names	Description
xOE	Output Enable (Active LOW)
Ax	Port A Inputs or Outputs
Bx	Port B Inputs or Outputs

FUNCTION TABLE⁽¹⁾

Input		1A, 1B I/Os	2A, 2B I/Os
1OE	2OE		
H	H	Disconnect	Disconnect
L	H	1A Port = 1B Port	Disconnect
H	L	Disconnect	2A Port = 2B Port
L	L	1A Port = 1B Port	2A Port = 2B Port

NOTE:

1. H = HIGH Voltage Level
L = LOW Voltage Level

OPERATING CHARACTERISTICS, TA = 25°C⁽¹⁾

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
Vcc	Supply Voltage		2.3	3.6	V
VIH	High-Level Control Input Voltage	Vcc = 2.3V to 2.7V	1.7	—	V
		Vcc = 2.7V to 3.6V	2	—	
VIL	Low-Level Control Input Voltage	Vcc = 2.3V to 2.7V	—	0.7	V
		Vcc = 2.7V to 3.6V	—	0.8	
TA	Operating Free-Air Temperature		-40	85	°C

NOTE:

1. All unused control inputs of the device must be held at Vcc or GND to ensure proper device operation.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Conditions: TA = -40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
VIK	Control Inputs, Data Inputs	VCC = 3V, I _I = -18mA		—	—	-1.2	V
I _I	Control Inputs	VCC = 3.6V, VI = VCC or GND		—	—	±1	µA
I _{OZ}	Data I/O	VCC = 3.6V, VO = 0 or 3.6V, switch disabled		—	—	5	µA
I _{OFF}		VCC = 0, VI or VO = 0 to 3.6V		—	—	50	µA
I _{CC}		VCC = 3.6V, IO = 0, VI = VCC or GND		—	—	10	µA
ΔI _{CC} ⁽¹⁾	Control Inputs	VCC = 3.6V, one input at 3V, other inputs at VCC or GND		—	—	300	µA
C _I	Control Inputs	VI = 3V or 0		—	4	—	pF
C _{O(OFF)}		VO = 3V or 0, OE = VCC		—	6	—	pF
R _{ON} ⁽²⁾	V _{CC} = 2.3V Typ. at V _{CC} = 2.5V	VI = 0	I _O = 64mA	—	5	8	Ω
			I _O = 24mA	—	5	8	
		VI = 1.7V	I _O = 15mA	—	27	40	
	V _{CC} = 3V	VI = 0	I _O = 64mA	—	5	7	
			I _O = 24mA	—	5	7	
		VI = 2.4V	I _O = 15mA	—	10	15	

NOTES:

1. The increase in supply current is attributable to each current that is at the specified voltage level rather than VCC or GND.
2. This is measured by the voltage drop between the A and B terminals at the indicated current through the switch.

SWITCHING CHARACTERISTICS

Symbol	Parameter	V _{CC} = 2.5V ± 0.2V		V _{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	
t _{PD} ⁽¹⁾	Propagation Delay A to B or B to A	—	0.15	—	0.25	ns
t _{EN}	Output Enable Time OE to A or B	1	4.5	1	4	ns
t _{DIS}	Output Disable Time OE to A or B	1	4.5	1	5	ns

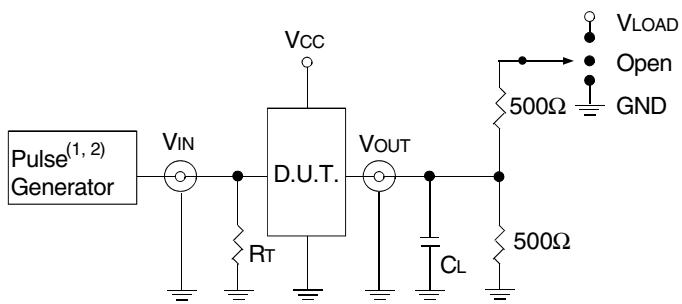
NOTE:

1. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance driven by an ideal voltage source (zero output impedance).

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)} = 3.3V \pm 0.3V$	$V_{CC}^{(2)} = 2.5V \pm 0.2V$	Unit
V_{LOAD}	6	$2 \times V_{CC}$	V
V_{IH}	3	V_{CC}	V
V_T	1.5	$V_{CC} / 2$	V
V_{LZ}	300	150	mV
V_{HZ}	300	150	mV
C_L	50	30	pF



Test Circuits for All Outputs

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

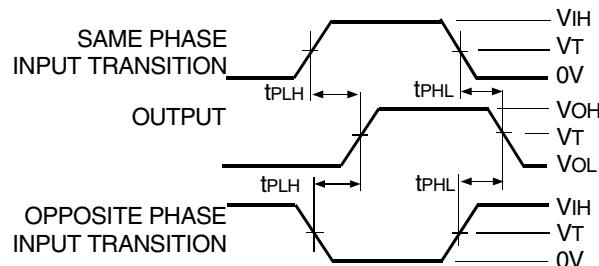
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

NOTES:

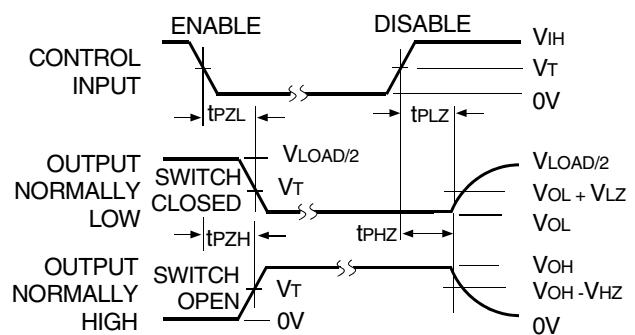
1. Pulse Generator for All Pulses: Rate $\leq 10MHz$; $t_f \leq 2.5ns$; $t_r \leq 2.5ns$.
2. Pulse Generator for All Pulses: Rate $\leq 10MHz$; $t_f \leq 2ns$; $t_r \leq 2.5ns$.

SWITCH POSITION

Test	Switch
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND
t_{PD}	Open

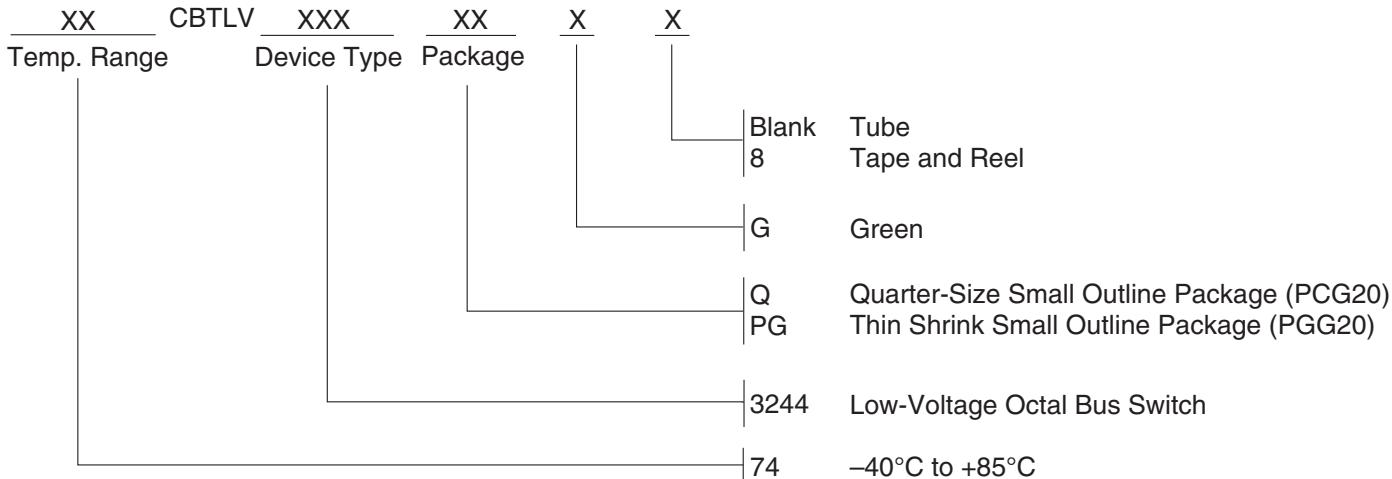


Propagation Delay



Enable and Disable Times

ORDERING INFORMATION



Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
	74CBTLV3244PGG	PGG20	TSSOP	I
	74CBTLV3244PGG8	PGG20	TSSOP	I
	74CBTLV3244QG	PCG20	QSOP	I
	74CBTLV3244QG8	PCG20	QSOP	I

Datasheet Document History

12/18/2014 Pg. 5 Updated the ordering information by removing the "IDT" notation, non RoHS part and by adding Tape and Reel information.

05/31/2019 Pg. 2,5 Added table under pin configuration diagram with detailed package information and orderable part information table. Updated the ordering information diagram in clearer detail.

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