

FEATURES:

- Pin-out compatible with standard '244 Logic products
- 5Ω A/B bi-directional switch
- Isolation under power-off conditions
- Over-voltage tolerant
- Latch-up performance exceeds 100mA
- $V_{CC} = 2.3V - 3.6V$, Normal Range
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- Available in QSOP and TSSOP packages

APPLICATIONS:

- 3.3V High Speed Bus Switching and Bus Isolation

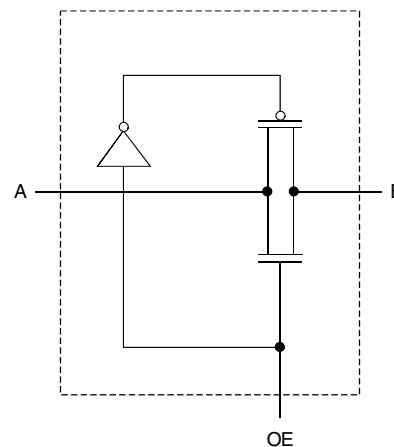
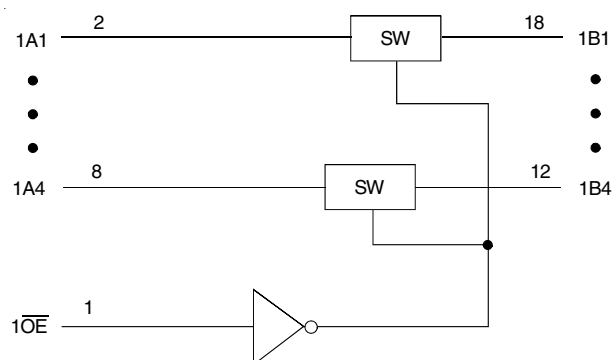
DESCRIPTION:

The octal bus switch has standard 244 pinouts. The CBTLV3244 is designed for asynchronous communication between data buses. Sets of four switches are controlled by one output Enable (\overline{OE}). When \overline{OE} is low, the set of four bus switches is on and port A is connected to port B. When \overline{OE} is high, the set of four bus switches is off and a high impedance exists between port A and port B.

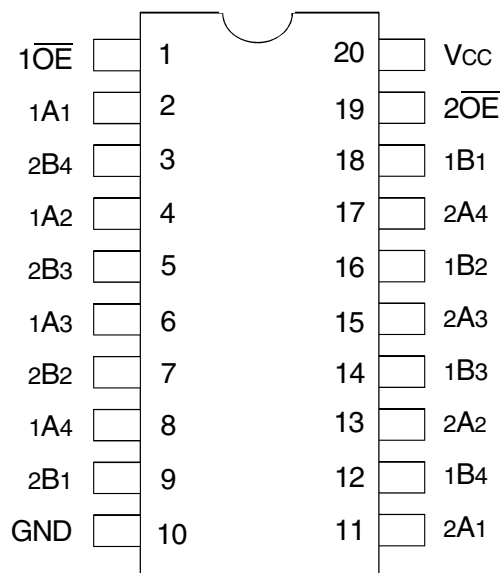
To ensure the high-impedance state during power up or power down, both \overline{OE} s should be tied to V_{CC} through a pullup resistor.

FUNCTIONAL BLOCK DIAGRAM

SIMPLIFIED SCHEMATIC, EACH SWITCH



PIN CONFIGURATION



TOP VIEW

Package Type	Package Code	Order Code
TSSOP	PGG20	PGG
QSOP	PCG20	QG

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{CC}	Supply Voltage Range	-0.5 to +4.6	V
V _I	Input Voltage Range	-0.5 to +4.6	V
	Continuous Channel Current	128	mA
I _{IK}	Input Clamp Current, V _{I/O} < 0	-50	mA
T _{STG}	Storage Temperature	-65 to +150	°C

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PIN DESCRIPTION

Pin Names	Description
xOE	Output Enable (Active LOW)
A x	Port A Inputs or Outputs
B x	Port B Inputs or Outputs

FUNCTION TABLE⁽¹⁾

Input		1A, 1B I/Os	2A, 2B I/Os
1OE	2OE		
H	H	Disconnect	Disconnect
L	H	1A Port = 1B Port	Disconnect
H	L	Disconnect	2A Port = 2B Port
L	L	1A Port = 1B Port	2A Port = 2B Port

NOTE:

1. H = HIGH Voltage Level
L = LOW Voltage Level

OPERATING CHARACTERISTICS, T_A = 25°C⁽¹⁾

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V _{CC}	Supply Voltage		2.3	3.6	V
V _{IH}	High-Level Control Input Voltage	V _{CC} = 2.3V to 2.7V	1.7	—	V
		V _{CC} = 2.7V to 3.6V	2	—	
V _{IL}	Low-Level Control Input Voltage	V _{CC} = 2.3V to 2.7V	—	0.7	V
		V _{CC} = 2.7V to 3.6V	—	0.8	
T _A	Operating Free-Air Temperature		-40	85	°C

NOTE:

1. All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Conditions: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{IK}	Control Inputs, Data Inputs	$V_{CC} = 3\text{V}$, $I_I = -18\text{mA}$		—	—	-1.2	V
I_I	Control Inputs	$V_{CC} = 3.6\text{V}$, $V_I = V_{CC}$ or GND		—	—	± 1	μA
I_{OZ}	Data I/O	$V_{CC} = 3.6\text{V}$, $V_O = 0$ or 3.6V , switch disabled		—	—	5	μA
I_{OFF}		$V_{CC} = 0$, V_I or $V_O = 0$ to 3.6V		—	—	50	μA
I_{CC}		$V_{CC} = 3.6\text{V}$, $I_O = 0$, $V_I = V_{CC}$ or GND		—	—	10	μA
$\Delta I_{CC}^{(1)}$	Control Inputs	$V_{CC} = 3.6\text{V}$, one input at 3V , other inputs at V_{CC} or GND		—	—	300	μA
C_I	Control Inputs	$V_I = 3\text{V}$ or 0		—	4	—	pF
$C_{IO(OFF)}$		$V_O = 3\text{V}$ or 0 , $\overline{OE} = V_{CC}$		—	6	—	pF
$R_{ON}^{(2)}$	$V_{CC} = 2.3\text{V}$ Typ. at $V_{CC} = 2.5\text{V}$	$V_I = 0$	$I_O = 64\text{mA}$	—	5	8	Ω
			$I_O = 24\text{mA}$	—	5	8	
	$V_{CC} = 3\text{V}$	$V_I = 1.7\text{V}$	$I_O = 15\text{mA}$	—	27	40	
			$I_O = 64\text{mA}$	—	5	7	
			$I_O = 24\text{mA}$	—	5	7	
			$I_O = 15\text{mA}$	—	10	15	

NOTES:

- The increase in supply current is attributable to each current that is at the specified voltage level rather than V_{CC} or GND.
- This is measured by the voltage drop between the A and B terminals at the indicated current through the switch.

SWITCHING CHARACTERISTICS

Symbol	Parameter	$V_{CC} = 2.5\text{V} \pm 0.2\text{V}$		$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$		Unit
		Min.	Max.	Min.	Max.	
$t_{PD}^{(1)}$	Propagation Delay A to B or B to A	—	0.15	—	0.25	ns
t_{EN}	Output Enable Time \overline{OE} to A or B	1	4.5	1	4	ns
t_{DIS}	Output Disable Time \overline{OE} to A or B	1	4.5	1	5	ns

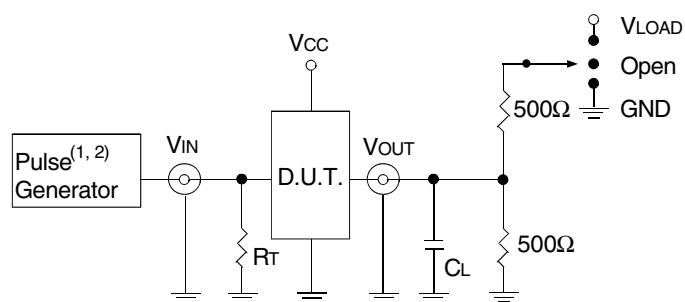
NOTE:

- The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance driven by an ideal voltage source (zero output impedance).

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)} = 3.3V \pm 0.3V$	$V_{CC}^{(2)} = 2.5V \pm 0.2V$	Unit
V_{LOAD}	6	$2 \times V_{CC}$	V
V_{IH}	3	V_{CC}	V
V_T	1.5	$V_{CC} / 2$	V
V_{LZ}	300	150	mV
V_{HZ}	300	150	mV
C_L	50	30	pF



Test Circuits for All Outputs

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

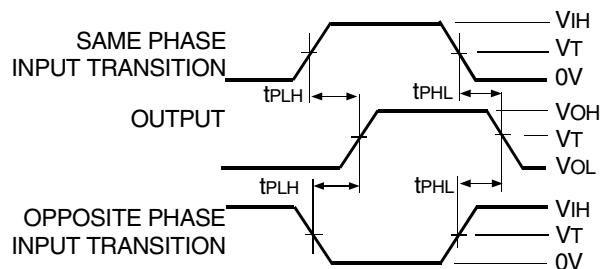
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

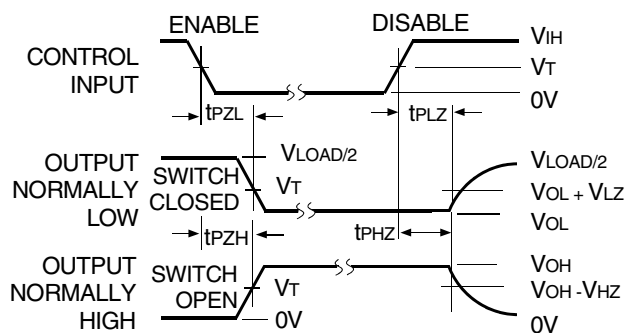
1. Pulse Generator for All Pulses: Rate $\leq 10MHz$; $t_r \leq 2.5ns$; $t_f \leq 2.5ns$.
2. Pulse Generator for All Pulses: Rate $\leq 10MHz$; $t_r \leq 2ns$; $t_f \leq 2.5ns$.

SWITCH POSITION

Test	Switch
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND
t_{PD}	Open

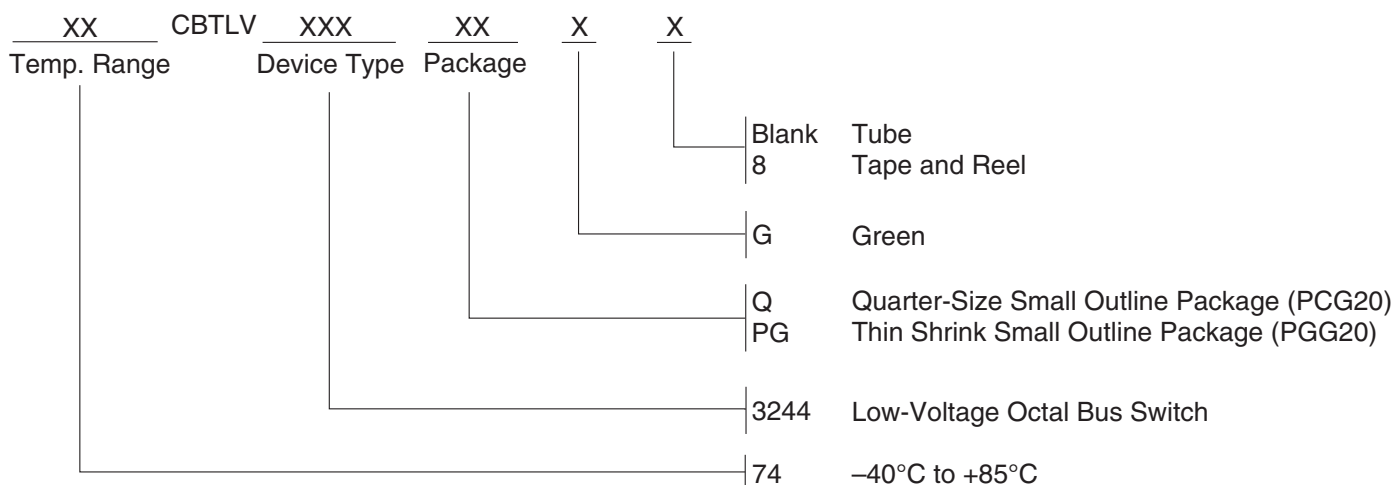


Propagation Delay



Enable and Disable Times

ORDERING INFORMATION



Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
	74CBTLV3244PGG	PGG20	TSSOP	I
	74CBTLV3244PGG8	PGG20	TSSOP	I
	74CBTLV3244QG	PCG20	QSOP	I
	74CBTLV3244QG8	PCG20	QSOP	I

Datasheet Document History

12/18/2014	Pg. 5	Updated the ordering information by removing the "IDT" notation, non RoHS part and by adding Tape and Reel information.
05/31/2019	Pg. 2,5	Added table under pin configuration diagram with detailed package information and orderable part information table. Updated the ordering information diagram in clearer detail.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.