

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SR(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to $3.6V$, Extended Range
- $V_{CC} = 2.5V \pm 0.2V$
- CMOS power levels (0.4 μ W typ. static)
- Rail-to-Rail output swing for increased noise margin
- Available in TSVOP package

DRIVE FEATURES:

- Balanced Output Drivers: $\pm 12mA$
- Low switching noise

APPLICATIONS:

- SDRAM Modules
- PC Motherboards
- Workstations

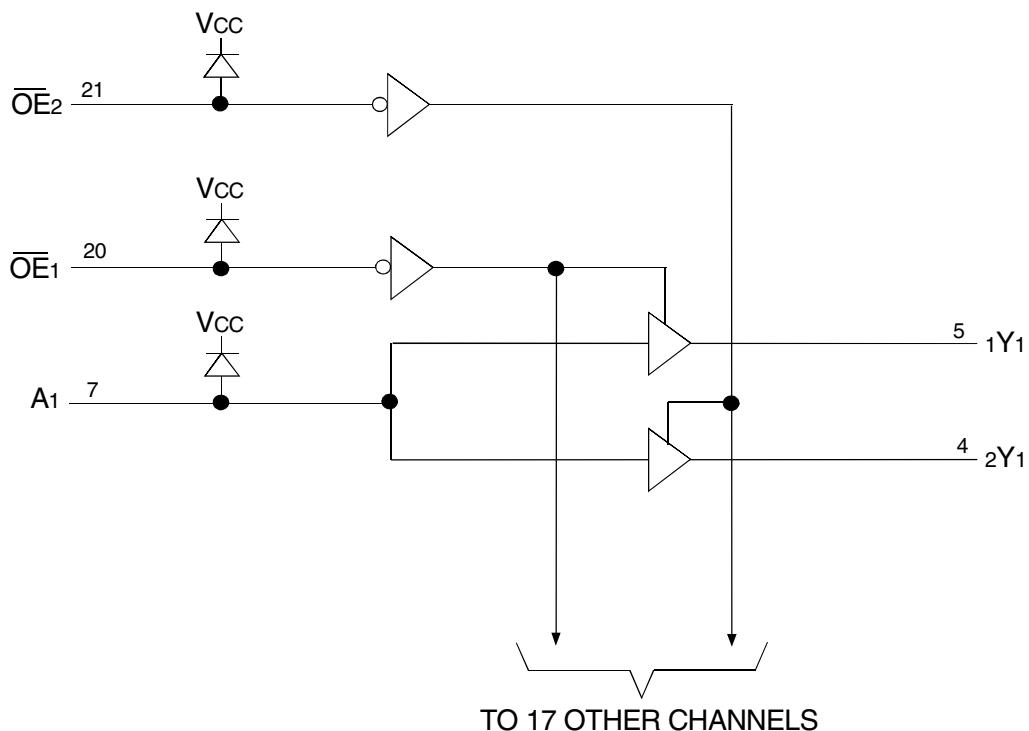
DESCRIPTION:

This 1-bit to 2-bit address driver is built using advanced dual metal CMOS technology. Diodes to V_{CC} have been added on the inputs to clamp overshoot.

The ALVCHS162830 has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been designed to drive $\pm 12mA$ at the designated threshold levels.

The ALVCHS162830 has "bus-hold" which retains the inputs' last state whenever the input bus goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

| | | | |
|------|----|----|------|
| 2Y2 | 1 | 80 | 1Y3 |
| 1Y2 | 2 | 79 | 2Y3 |
| GND | 3 | 78 | GND |
| 2Y1 | 4 | 77 | 1Y4 |
| 1Y1 | 5 | 76 | 2Y4 |
| Vcc | 6 | 75 | Vcc |
| A1 | 7 | 74 | 1Y5 |
| A2 | 8 | 73 | 2Y5 |
| GND | 9 | 72 | GND |
| A3 | 10 | 71 | 1Y6 |
| A4 | 11 | 70 | 2Y6 |
| GND | 12 | 69 | GND |
| A5 | 13 | 68 | 1Y7 |
| A6 | 14 | 67 | 2Y7 |
| Vcc | 15 | 66 | Vcc |
| A7 | 16 | 65 | 1Y8 |
| A8 | 17 | 64 | 2Y8 |
| GND | 18 | 63 | GND |
| A9 | 19 | 62 | 1Y9 |
| OE1 | 20 | 61 | 2Y9 |
| OE2 | 21 | 60 | 1Y10 |
| A10 | 22 | 59 | 2Y10 |
| GND | 23 | 58 | GND |
| A11 | 24 | 57 | 1Y11 |
| A12 | 25 | 56 | 2Y11 |
| Vcc | 26 | 55 | Vcc |
| A13 | 27 | 54 | 1Y12 |
| A14 | 28 | 53 | 2Y12 |
| GND | 29 | 52 | GND |
| A15 | 30 | 51 | 1Y13 |
| A16 | 31 | 50 | 2Y13 |
| GND | 32 | 49 | GND |
| A17 | 33 | 48 | 1Y14 |
| A18 | 34 | 47 | 2Y14 |
| Vcc | 35 | 46 | Vcc |
| 2Y18 | 36 | 45 | 1Y15 |
| 1Y18 | 37 | 44 | 2Y15 |
| GND | 38 | 43 | GND |
| 2Y17 | 39 | 42 | 1Y16 |
| 1Y17 | 40 | 41 | 2Y16 |

TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Description | Max | Unit |
|----------------------|--|-----------------|------|
| VTERM ⁽²⁾ | Terminal Voltage with Respect to GND | -0.5 to +4.6 | V |
| VTERM ⁽³⁾ | Terminal Voltage with Respect to GND | -0.5 to Vcc+0.5 | V |
| TSTG | Storage Temperature | -65 to +150 | °C |
| I _{OUT} | DC Output Current | -50 to +50 | mA |
| I _{IK} | Continuous Clamp Current, V _I < 0 or V _I > V _{cc} | ±50 | mA |
| I _{OK} | Continuous Clamp Current, V _O < 0 | -50 | mA |
| I _{CC} | Continuous Current through each V _{cc} or GND | ±100 | mA |
| I _{SS} | | | |

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{cc} terminals.
3. All terminals except V_{cc}.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Typ. | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 5 | 7 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | 7 | 9 | pF |
| C _{OUT} | I/O Port Capacitance | V _{IN} = 0V | 7 | 9 | pF |

NOTE:

1. As applicable to the device type.

PIN DESCRIPTION

| Pin Names | Description |
|------------------|---|
| OE _{Ex} | 3-State Output Enable Inputs (Active LOW) |
| A _x | Data Inputs ⁽¹⁾ |
| xY _x | 3-State Outputs |

NOTE:

1. These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLE⁽¹⁾

| Inputs | | | Outputs | |
|-----------------|-----------------|----------------|-----------------|-----------------|
| OE ₁ | OE ₂ | A _x | 1Y _x | 2Y _x |
| L | H | H | H | Z |
| L | H | L | L | Z |
| H | L | H | Z | H |
| H | L | L | Z | L |
| L | L | H | H | H |
| L | L | L | L | L |
| H | H | X | Z | Z |

NOTE:

1. H = HIGH Voltage Level
- L = LOW Voltage Level
- X = Don't Care
- Z = High Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

| Symbol | Parameter | Test Conditions | | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|--|--|---|----------------------------------|------|---------------------|----------|---------------|
| V _{IH} | Input HIGH Voltage Level | V _{CC} = 2.3V to 2.7V | | 1.7 | — | — | V |
| | | V _{CC} = 2.7V to 3.6V | | 2 | — | — | |
| V _{IL} | Input LOW Voltage Level | V _{CC} = 2.3V to 2.7V | | — | — | 0.7 | V |
| | | V _{CC} = 2.7V to 3.6V | | — | — | 0.8 | |
| I _{IH} | Input HIGH Current | V _{CC} = 3.6V | V _I = V _{CC} | — | — | ± 5 | μA |
| I _{IL} | Input LOW Current | V _{CC} = 3.6V | V _I = GND | — | — | ± 5 | μA |
| I _{OZH} | High Impedance Output Current (3-State Output pins) | V _{CC} = 3.6V | V _O = V _{CC} | — | — | ± 10 | μA |
| | | | V _O = GND | — | — | ± 10 | |
| V _{IK} | Clamp Diode Voltage | V _{CC} = 2.3V, I _{IN} = -18mA | | — | -0.7 | -1.2 | V |
| V _H | Input Hysteresis | V _{CC} = 3.3V | | — | 100 | — | mV |
| I _{CCL} I _{CCH} I _{CZZ} | Quiescent Power Supply Current | V _{CC} = 3.6V V _{IN} = GND or V _{CC} | | — | 0.1 | 40 | μA |
| ΔI_{CC} | Quiescent Power Supply Current Variation | One input at V _{CC} - 0.6V, other inputs at V _{CC} or GND | | — | — | 750 | μA |

NOTE:

1. Typical values are at V_{CC} = 3.3V, $+25^\circ\text{C}$ ambient.

BUS-HOLD CHARACTERISTICS

| Symbol | Parameter ⁽¹⁾ | Test Conditions | | Min. | Typ. ⁽²⁾ | Max. | Unit |
|-------------------|----------------------------------|------------------------|----------------------------|------|---------------------|-----------|---------------|
| I _{BHH} | Bus-Hold Input Sustain Current | V _{CC} = 3V | V _I = 2V | -75 | — | — | μA |
| | | | V _I = 0.8V | 75 | — | — | |
| I _{BHH} | Bus-Hold Input Sustain Current | V _{CC} = 2.3V | V _I = 1.7V | -45 | — | — | μA |
| | | | V _I = 0.7V | 45 | — | — | |
| I _{BHHO} | Bus-Hold Input Overdrive Current | V _{CC} = 3.6V | V _I = 0 to 3.6V | — | — | ± 500 | μA |
| | | | | | | | |

NOTES:

1. Pins with Bus-Hold are identified in the pin description.

2. Typical values are at V_{CC} = 3.3V, $+25^\circ\text{C}$ ambient.

OUTPUT DRIVE CHARACTERISTICS

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Max. | Unit |
|--------|---------------------|--------------------------------|---------------|-----------|------|------|
| VOH | Output HIGH Voltage | VCC = 2.3V to 3.6V | IOH = - 0.1mA | VCC - 0.2 | — | V |
| | | VCC = 2.3V | IOH = - 4mA | 1.9 | — | |
| | | VCC = 2.7V | IOH = - 6mA | 1.7 | — | |
| | | | IOH = - 4mA | 2.2 | — | |
| | | VCC = 3V | IOH = - 8mA | 2 | — | |
| | | | IOH = - 6mA | 2.4 | — | |
| VOL | Output LOW Voltage | VCC = 2.3V to 3.6V | IOL = 0.1mA | — | 0.2 | V |
| | | VCC = 2.3V | IOL = 4mA | — | 0.4 | |
| | | | IOL = 6mA | — | 0.55 | |
| | | VCC = 2.7V | IOL = 4mA | — | 0.4 | |
| | | | IOL = 8mA | — | 0.6 | |
| | | VCC = 3V | IOL = 6mA | — | 0.55 | |
| | | | IOL = 12mA | — | 0.8 | |

NOTE:

1. VIH and Vil must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate Vcc range.
TA = - 40°C to + 85°C.

OPERATING CHARACTERISTICS, TA = 25°C

| Symbol | Parameter | Test Conditions | Vcc = 2.5V ± 0.2V | Vcc = 3.3V ± 0.3V | Unit |
|--------|---|---------------------|-------------------|-------------------|------|
| | | | Typical | Typical | |
| CPD | Power Dissipation Capacitance per Driver Outputs enabled | CL = 0pF, f = 10Mhz | 49 | 53 | pF |
| | Power Dissipation Capacitance per Driver Outputs disabled | | 6 | 7.5 | |

SWITCHING CHARACTERISTICS⁽¹⁾

| Symbol | Parameter | Vcc = 2.5V ± 0.2V | | Vcc = 2.7V | | Vcc = 3.3V ± 0.3V | | Unit |
|--------|-----------------------------------|-------------------|------|------------|------|-------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| tPLH | Propagation Delay Ax to xYx | 1.2 | 3.8 | — | 4 | 1.7 | 3.5 | ns |
| tPHL | — | — | — | — | — | — | — | — |
| tPZH | Output Enable Time OEx to xYx | 1 | 5.7 | — | 5.7 | 1 | 4.8 | ns |
| tPZL | — | — | — | — | — | — | — | — |
| tPHZ | Output Disable Time OEx to xYx | 1 | 4.9 | — | 5.4 | 1.7 | 5.2 | ns |
| tPLZ | — | — | — | — | — | — | — | — |
| tSK(0) | Output Skew ⁽²⁾ | — | — | — | — | — | 500 | ps |

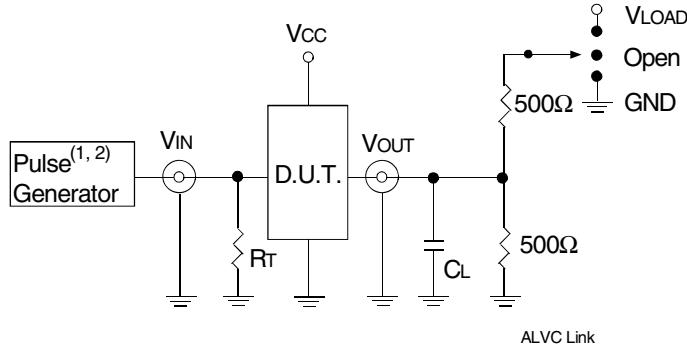
NOTES:

1. See TEST CIRCUITS AND WAVEFORMS. TA = - 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

| Symbol | $V_{CC}^{(1)} = 3.3V \pm 0.3V$ | $V_{CC}^{(1)} = 2.7V$ | $V_{CC}^{(2)} = 2.5V \pm 0.2V$ | Unit |
|------------|--------------------------------|-----------------------|--------------------------------|------|
| V_{LOAD} | 6 | 6 | $2 \times V_{CC}$ | V |
| V_{IH} | 2.7 | 2.7 | V_{CC} | V |
| V_T | 1.5 | 1.5 | $V_{CC} / 2$ | V |
| V_{LZ} | 300 | 300 | 150 | mV |
| V_{HZ} | 300 | 300 | 150 | mV |
| C_L | 50 | 50 | 30 | pF |



Test Circuit for All Outputs

DEFINITIONS:

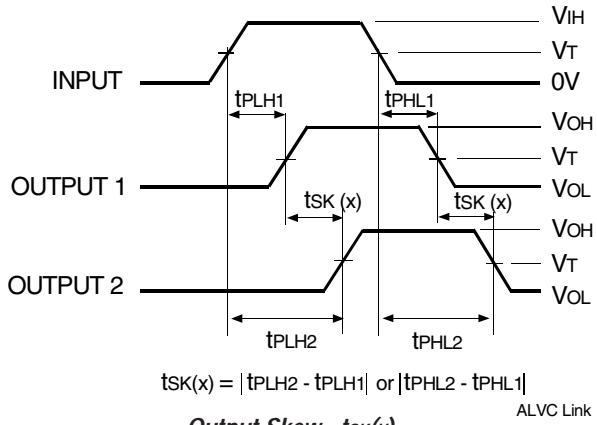
C_L = Load capacitance: includes jig and probe capacitance.R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; t_f $\leq 2.5\text{ns}$; t_r $\leq 2.5\text{ns}$.
2. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; t_f $\leq 2\text{ns}$; t_r $\leq 2\text{ns}$.

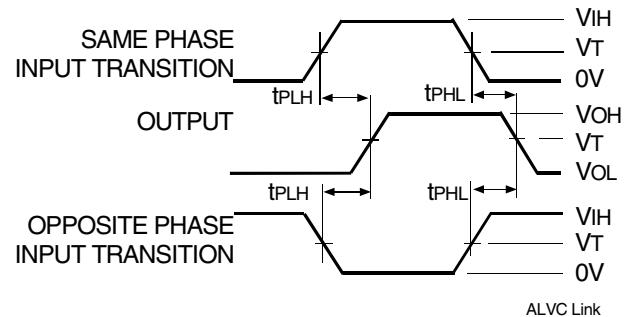
SWITCH POSITION

| Test | Switch |
|-----------------|------------|
| Open Drain | |
| Disable Low | V_{LOAD} |
| Enable Low | |
| Disable High | GND |
| Enable High | |
| All Other Tests | Open |

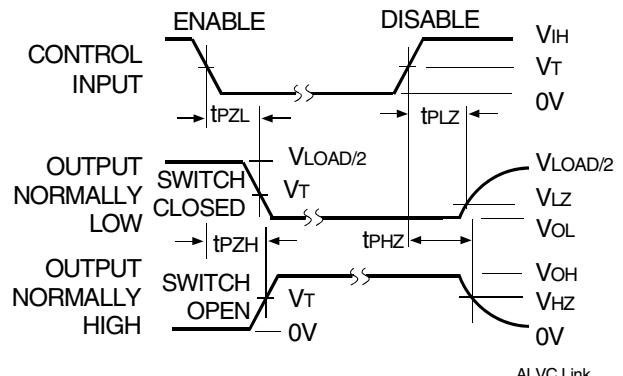
Output Skew - $tsk(x)$

NOTES:

1. For t_{sk(o)} OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{sk(b)} OUTPUT1 and OUTPUT2 are in the same bank.



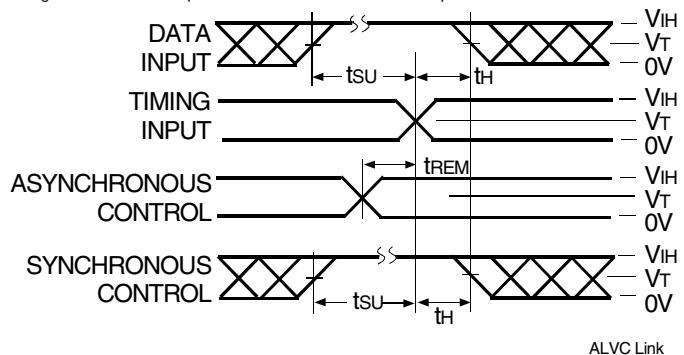
Propagation Delay



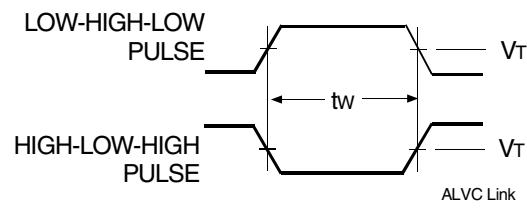
Enable and Disable Times

NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



Set-up, Hold, and Release Times



Pulse Width

ORDERING INFORMATION

| IDT | XX | ALVC | X | XXX | XXX | XX |
|-----|-------------|------|----------|--------|-------------|--|
| | Temp. Range | | Bus-Hold | Family | Device Type | Package |
| | | | | | | DF Thin Very Small Outline Package |
| | | | | | | DFG TVSOP - Green |
| | | | | | 830 | 1-Bit to 2-Bit Address Driver with 3-State Outputs |
| | | | | | S162 | Double-Density with Resistors and Clamps to Vcc, $\pm 12\text{mA}$ |
| | | | | | H | Bus-Hold |
| | | | | | 74 | -40°C to $+85^\circ\text{C}$ |

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